

MT3250

N-Channel Power MOSFET 50V, 120A, 4.8mΩ



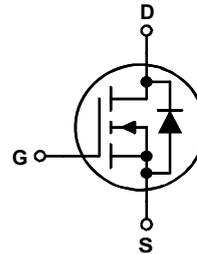
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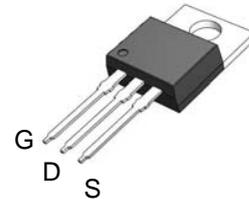
Features

- $R_{DS(on)} = 4.8m\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 60A$
- High performance trench technology for extremely low $R_{DS(on)}$
- High power and current handling capability
- RoHS compliant

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



TO-220FB-3L

Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		50	V
V_{GSS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ C$, Silicon Limited)	120*	A
		- Continuous ($T_C = 100^\circ C$, Silicon Limited)	90*	
		- Continuous ($T_C = 25^\circ C$, Package Limited)	35	
I_{DM}	Drain Current	- Pulsed (Note 1)	480	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	570	mJ
P_D	Power Dissipation	($T_C = 25^\circ C$)	206	W
		- Derate above $25^\circ C$	2.04	$W/^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +125	$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		150	$^\circ C$

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 100A.

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.79	$^\circ C/W$
$R_{\theta CS}$	Thermal Resistance, Case to Sink (Typ.)	0.8	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	69.5	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package			
MT3250	MT3250	TO-220	N/A	N/A	50units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μ	50			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32V V _{GS} = 0V	--	--	1	μA
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20V	--	--	±100	nA
On Characteristics						
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.8	1.2	1.4	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 60A	--	4.8	5.5	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance		--	2810	--	pF
C _{oss}	Output Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	--	580	--	pF
C _{rss}	Reverse Transfer Capacitance		--	270	--	pF
R _G	Gate Resistance	V _{GS} = 0.5V, f = 1MHz	--	1.1	--	Ω
Q _{g(tot)}	Total Gate Charge at 10V	V _{GS} = 0V to 10V	--	345	--	nC
Q _{g(2)}	Threshold Gate Charge	V _{GS} = 0V to 2V	--	32.5	--	nC
Q _{gs}	Gate to Source Gate Charge		--	49	--	nC
Q _{gs2}	Gate Charge Threshold to Plateau		--	16.5	--	nC
Q _{gd}	Gate to Drain "Miller" Charge		--	74	--	nC
Switching Characteristics (V_{GS} = 10V)						
t _{ON}	Turn-On Time		--	175	360	ns
t _{d(on)}	Turn-On Delay Time		--	43	95	ns
t _r	Rise Time	V _{DD} = 20V, I _D = 80A V _{GS} = 10V, R _{GEN} = 7Ω	--	130	275	ns
t _{d(off)}	Turn-Off Delay Time		--	435	875	ns
t _f	Fall Time		--	290	590	ns
t _{OFF}	Turn-Off Time		--	730	1470	ns
Drain-Source Diode Characteristics and Maximum Ratings						
V _{SD}	Source to Drain Diode Voltage	I _{SD} = 80A	--	0.8	1.30	V
		I _{SD} = 40A	--	--	1.0	V
t _{rr}	Reverse Recovery Time	I _{SD} = 75A, dI _{SD} /dt = 100A/μs	--	59	--	ns
Q _{RR}	Reverse Recovery Charge	I _{SD} = 75A, dI _{SD} /dt = 100A/μs	--	77	--	nC

NOTES:

1: Pulse width limited by maximum junction temperature.

2: Starting T_J = 25°C, L = 1mH, I_{AS} = 58A, V_{DD} = 36V, V_{GS} = 10V.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

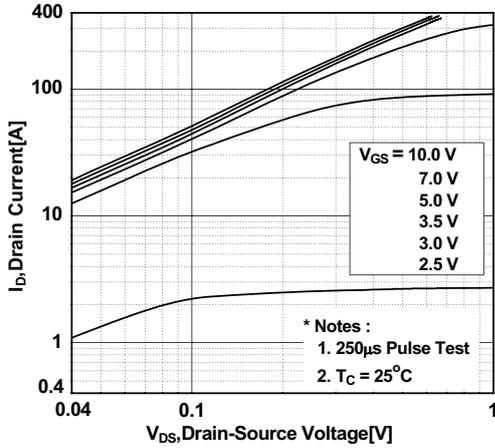


Figure 2. Transfer Characteristics

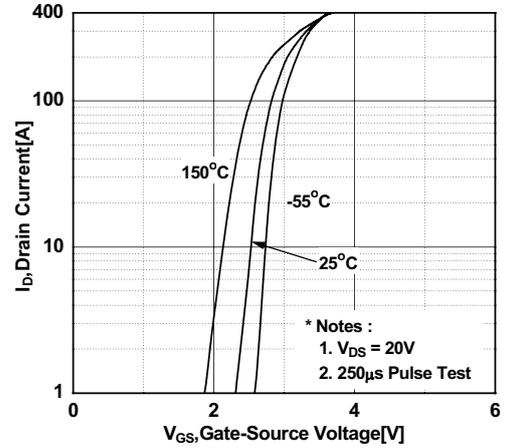


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

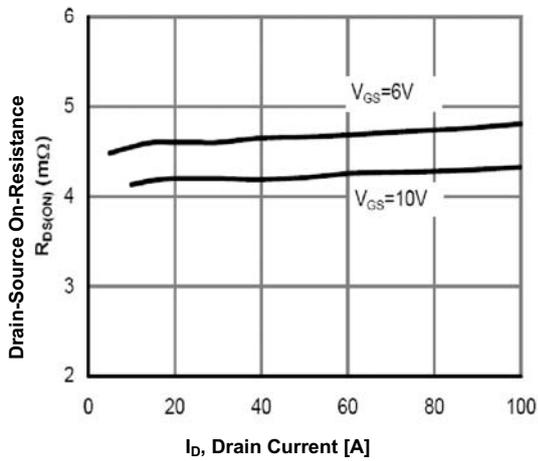


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

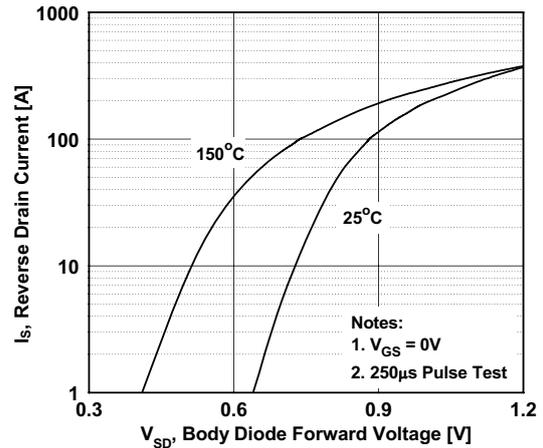


Figure 5. Capacitance Characteristics

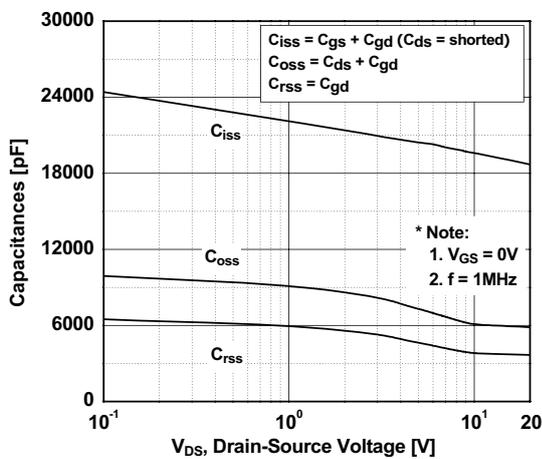
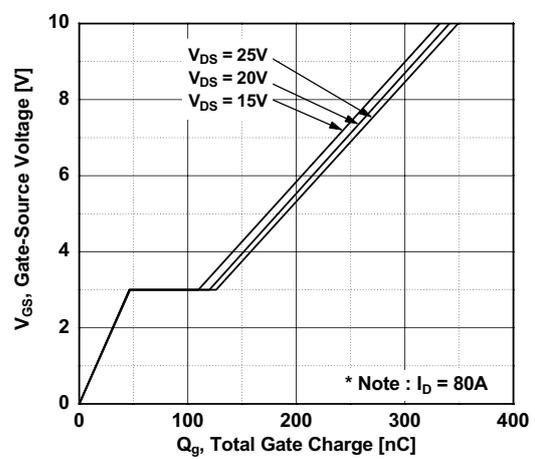


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

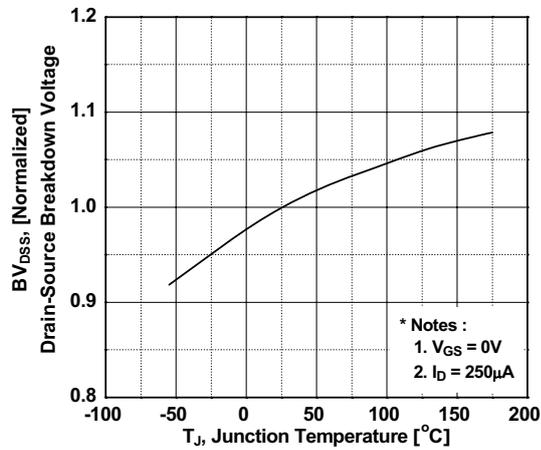


Figure 8. On-Resistance Variation vs. Temperature

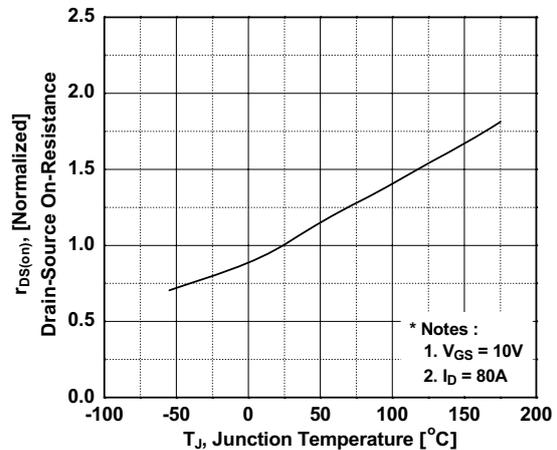


Figure 9. Unclamped Inductive Switching Capability

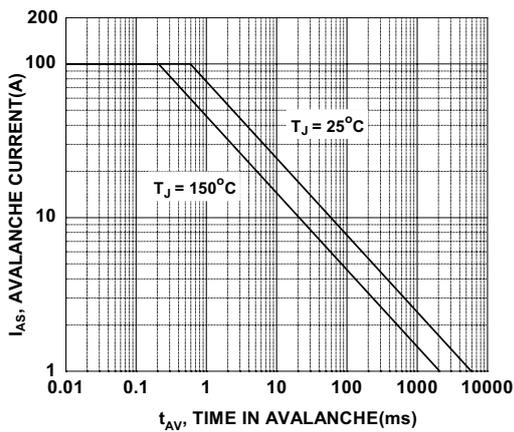


Figure 10. Safe Operating Area

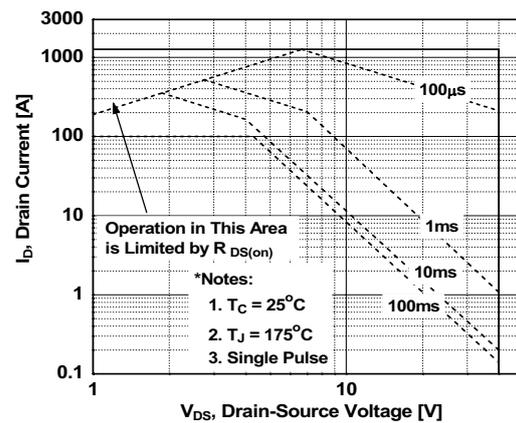
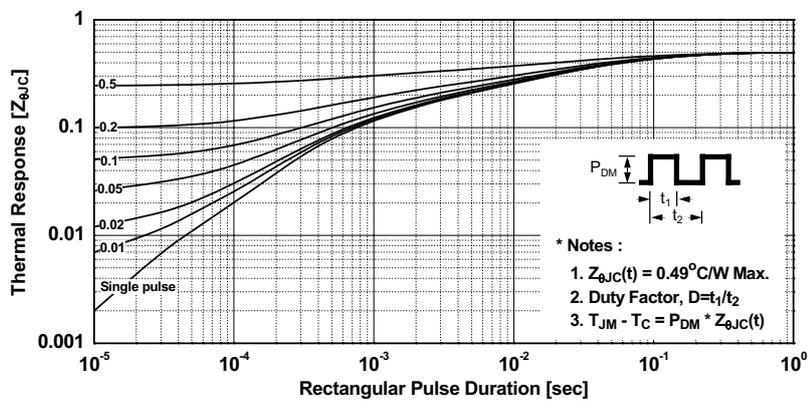
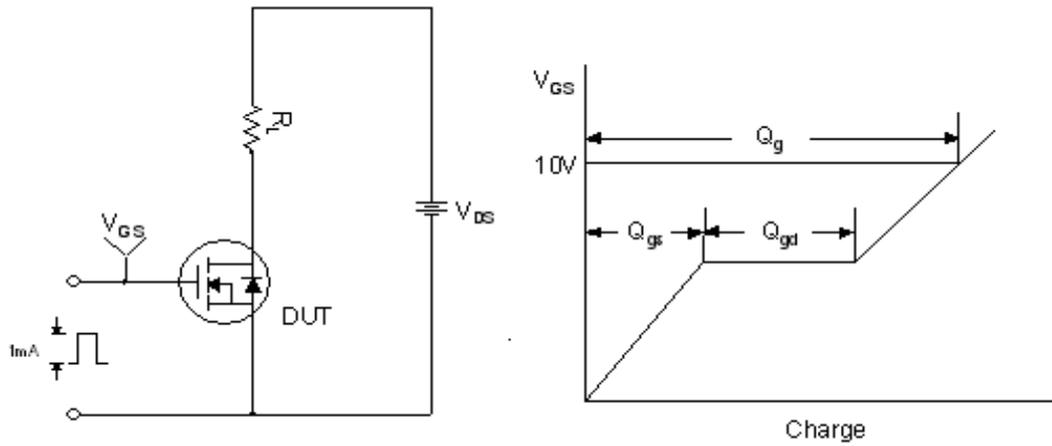


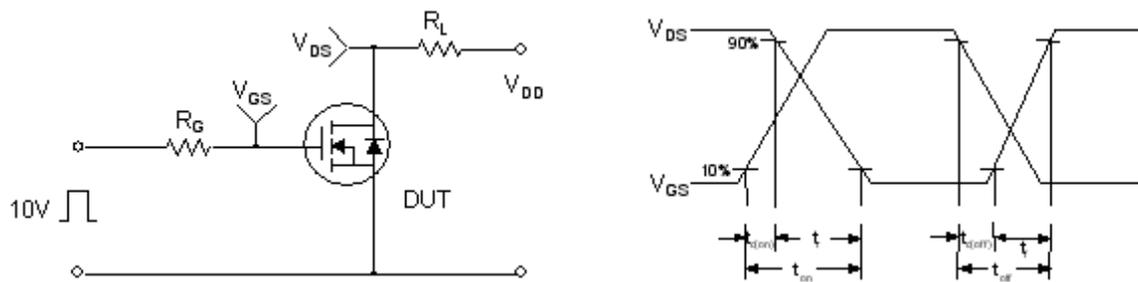
Figure 11. Transient Thermal Response Curve



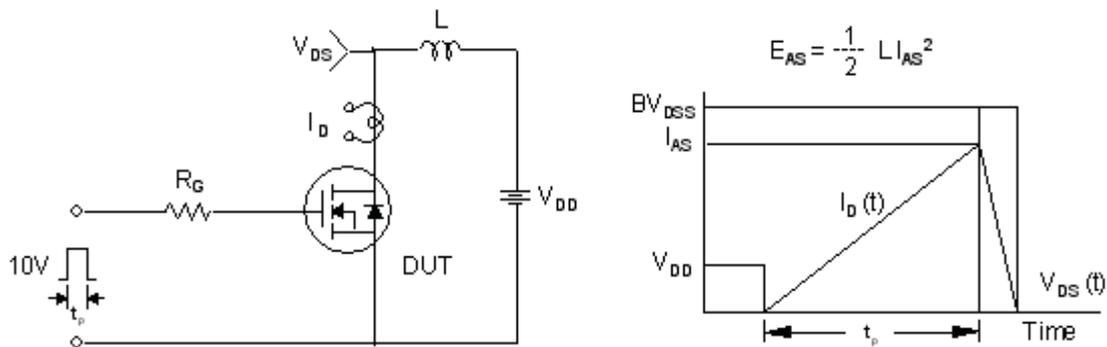
Gate Charge Test Circuit & Waveform



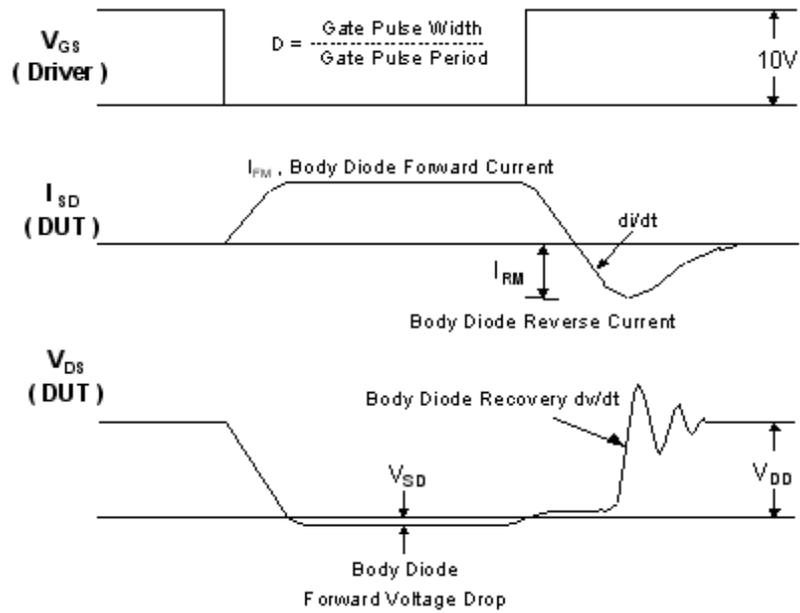
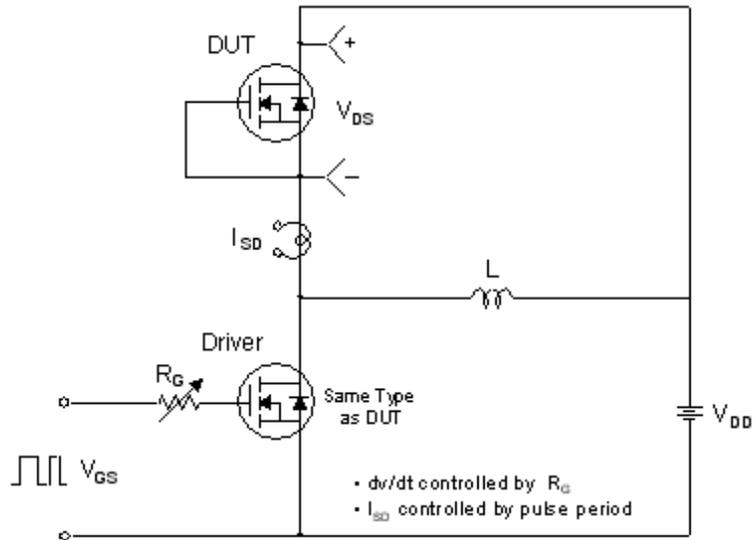
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

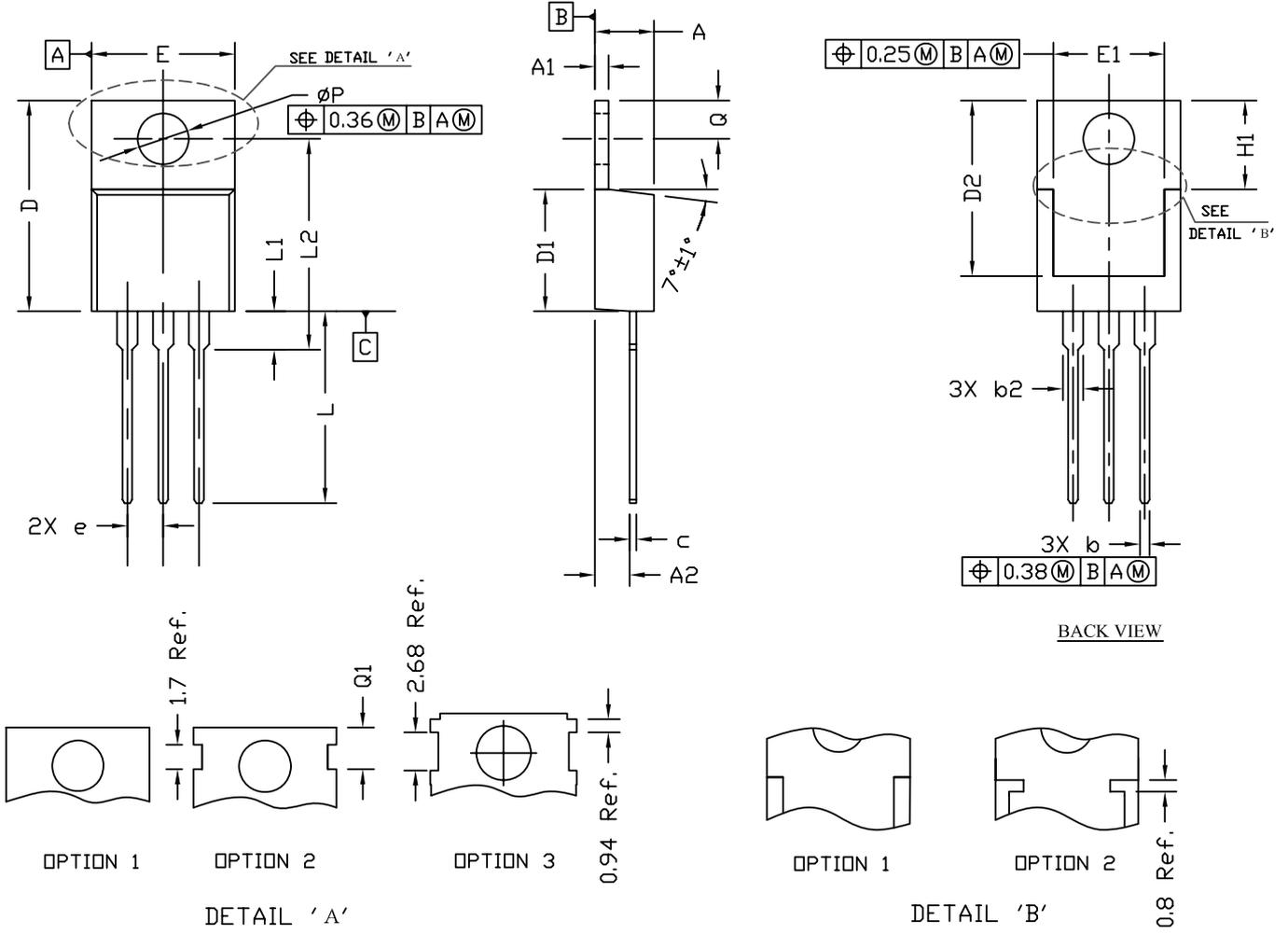


Peak Diode Recovery dv/dt Test Circuit & Waveforms

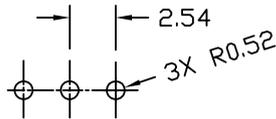


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TO220 PACKAGE OUTLINE



RECOMMENDATION OF HOLE PATTERN



UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.45	4.72	0.169	0.175	0.186
A1	1.15	1.27	1.40	0.045	0.050	0.055
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.69	0.81	0.95	0.027	0.032	0.037
b2	1.17	1.37	1.45	0.046	0.050	0.068
c	0.36	0.38	0.60	0.014	0.015	0.024
D	14.50	15.44	15.80	0.571	0.608	0.622
D1	8.59	9.14	9.65	0.338	0.360	0.380
D2	11.43	11.73	12.48	0.450	0.462	0.491
e	2.54 BSC			0.100 BSC.		
E	9.66	10.03	10.54	0.380	0.395	0.415
E1	6.22	---	---	0.245	---	---
H1	6.10	6.30	6.50	0.240	0.248	0.256
L	12.27	12.82	14.27	0.483	0.505	0.562
L1	2.47	---	3.90	0.097	---	0.154
L2	---	---	16.70	---	---	0.657
Q	2.59	2.74	2.89	0.102	0.108	0.114
ϕP	3.50	3.84	3.89	0.138	0.151	0.153
Q1	2.70	---	2.90	0.106	---	0.114

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