# MT3225

## N-Channel Low Qg® MOSFET

30V,150A,2.3mΩ

## General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional swiching PWM controllers It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

## Features

- $R_{DS(ON)}$ = 2.3mΩ , $V_{GS}$ = 10V, $I_D$ = 40A
- $R_{DS(ON)}$ =3.3mΩ , $V_{GS}$ = 4.5V, $I_D$ = 40A
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low gate charge
- High power and current handling capability

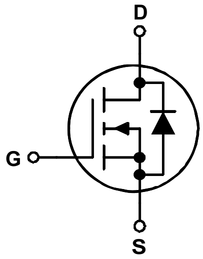
## Applications

- DC/DC converters

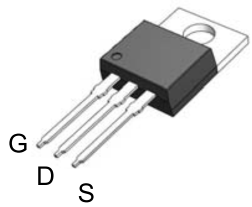
MT Semiconductor®

http://www.mtsemi.com

## Simplified Schematic




**MARKING DIAGRAM**
**& PIN ASSIGNMENT**




TO-220FB-3L

## Absolute Maximum Ratings ($T_A$ = 25℃ unless otherwise noted)

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| V | Drain to Source Voltage | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current<br>Continuous ($T_C$ = 25°C, $V_{GS}$ = 10V) (Note 1) | 150 | A |
| | Continuous ($T_C$ = 25°C, $V_{GS}$ = 4.5V) (Note 1) | 90 | A |
| | Continuous ($T_{amb}$ = 25°C, $V_{GS}$ = 10V, with $R_{\theta JA}$ = 62°C/W) | 16 | A |
| | Pulsed | Figure 4 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 2) | 115 | mJ |
| $P_D$ | Power dissipation | 120 | W |
| | Derate above 25°C | 0.73 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -55 to 150 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case TO-220 | 1.04 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient TO-220 ( Note 3) | 62 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| MT3224 | MT3224 | TO-220FB-3L | Tube | N/A | 50 units |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $B_{VDSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250µA, $V_{GS}$ = 0V | 30 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24V, $V_{GS}$ = 0V | - | - | 1 | µA |
| | | $T_C$ = 150°C | - | - | 250 | µA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(TH)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250µA | - | 2.0 | 3.0 | V |
| $R_{DS(ON)}$ | Drain to Source On Resistance | $I_D$ = 75A, $V_{GS}$ = 10V | - | 2.3 | 3.0 | mΩ |
| | | $I_D$ = 75A, $V_{GS}$ = 4.5V | - | 3.3 | 4.0 | mΩ |
| **Dynamic Characteristics** | | | | | | |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 15V, $V_{GS}$ = 0V, f = 1MHz | - | 4500 | - | pF |
| $C_{OSS}$ | Output Capacitance | | - | 460 | - | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | - | 195 | - | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 0.5V, f = 1MHz | - | 1.9 | - | Ω |
| $Q_{g(TOT)}$ | Total Gate Charge at 10V | $V_{GS}$ = 0V to 10V; $V_{DD}$ = 15V, $I_D$ = 40A, $I_g$ = 1.0mA | - | 56 | 72 | nC |
| $Q_{g(5)}$ | Total Gate Charge at 5V | $V_{GS}$ = 0V to 5V | - | 28 | 38 | nC |
| $Q_{g(TH)}$ | Threshold Gate Charge | $V_{GS}$ = 0V to 1V | - | 3.0 | 4.0 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 7.8 | - | nC |
| $Q_{gs2}$ | Gate Charge Threshold to Plateau | | - | 6.0 | - | nC |
| $Q_{gd}$ | Gate to Drain Miller Charge | | - | 10.3 | - | nC |
| **Switching Characteristics** ($V_{GS}$ = 10V) | | | | | | |
| $t_{ON}$ | Turn-On Time | $V_{DD}$ = 15V, $I_D$ = 40A, $V_{GS}$ = 4.5V, $R_{GS}$ = 4.7Ω | - | - | 100 | ns |
| $t_{d(ON)}$ | Turn-On Delay Time | | - | 10 | - | ns |
| $t_r$ | Rise Time | | - | 110 | - | ns |
| $t_{d(OFF)}$ | Turn-Off Delay Time | | - | 44 | - | ns |
| $t_f$ | Fall Time | | - | 31 | - | ns |
| $t_{OFF}$ | Turn-Off Time | | - | - | 112 | ns |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Voltage | $I_{SD}$ = 40A | - | 0.75 | 1.25 | V |
| | | $I_{SD}$ = 20A | - | - | 1.0 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$ = 40A, $dI_{SD}/dt$ = 100A/µs | - | - | 26 | ns |
| $Q_{RR}$ | Reverse Recovered Charge | $I_{SD}$ = 40A, $dI_{SD}/dt$ = 100A/µs | - | - | 70 | nC |

**Notes:**
**1:** Package current limitation is 80A.
**2:** Starting $T_J$ = 25°C, L = 51uH, $I_{AS}$ = 64A, $V_{DD}$ = 27V, $V_{GS}$ = 10V.
**3:** Pulse width = 100s.

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

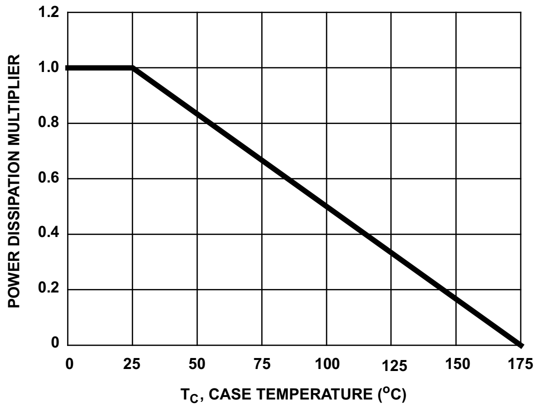



**Figure 1. Normalized Power Dissipation vs Case Temperature**

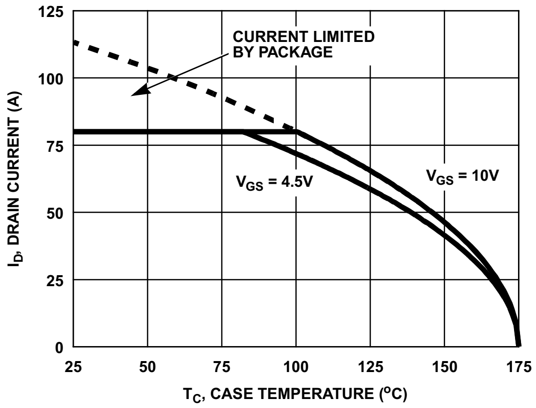



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

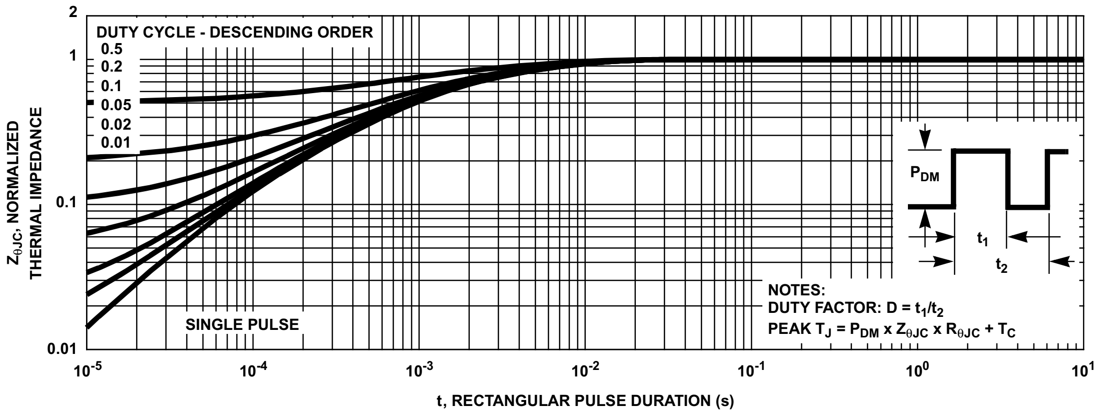



**Figure 3. Normalized Maximum Transient Thermal Impedance**

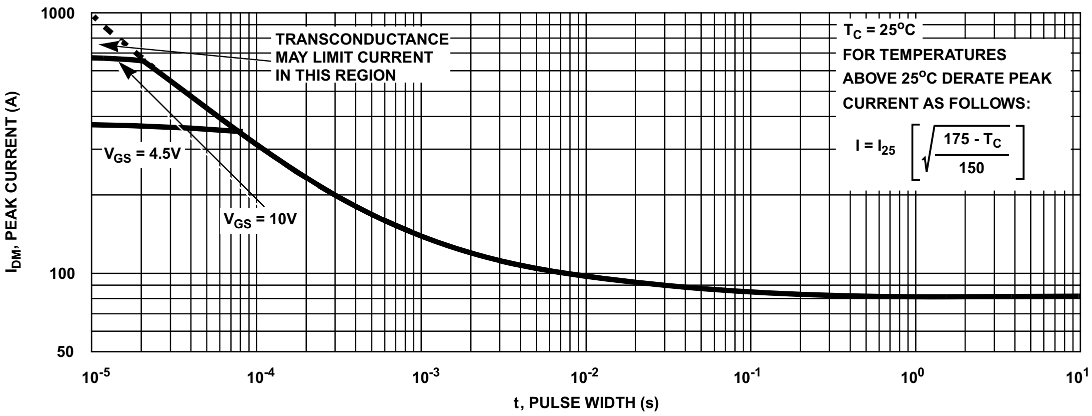



**Figure 4. Peak Current Capability**

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

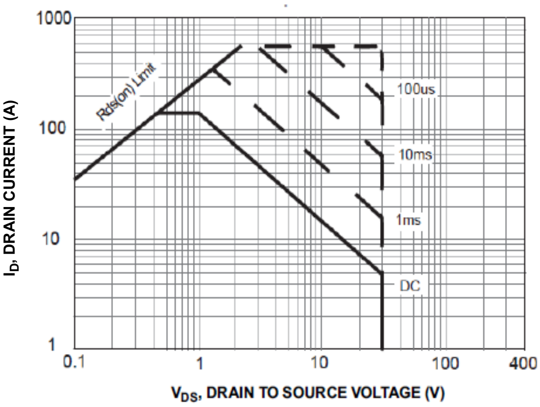
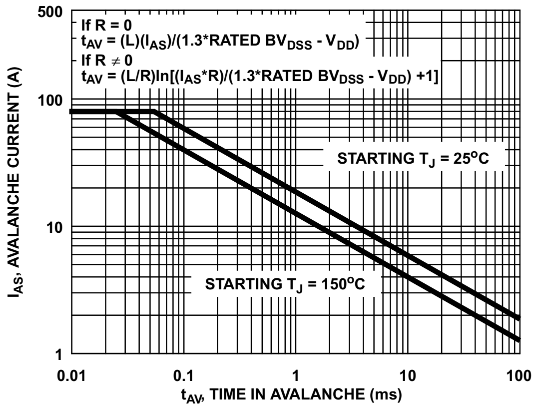



Figure 5. Forward Bias Safe Operating Area




NOTE Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

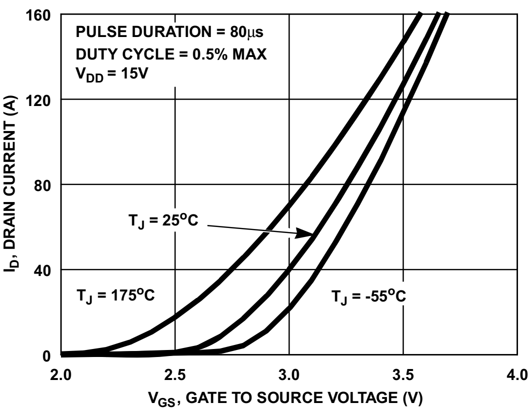



Figure 7. Transfer Characteristics

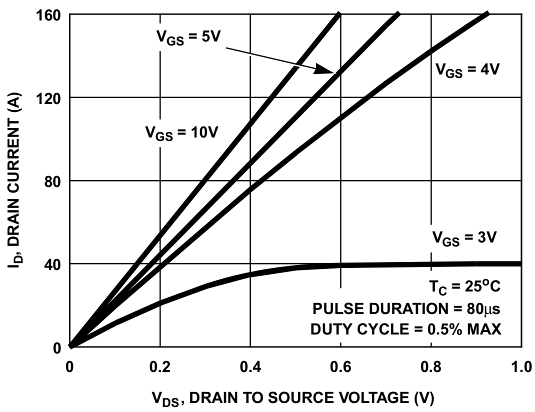



Figure 8. Saturation Characteristics

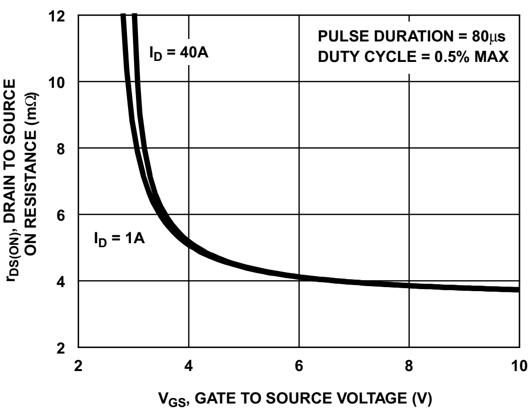



Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

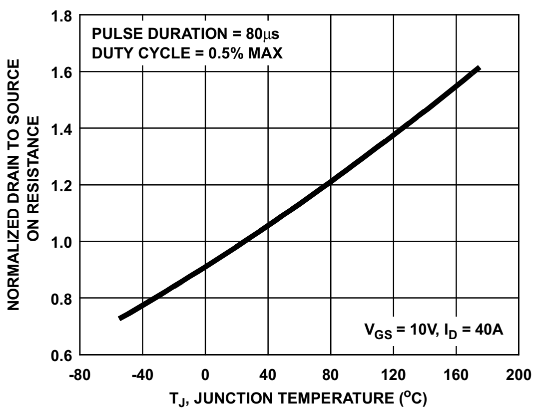



Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

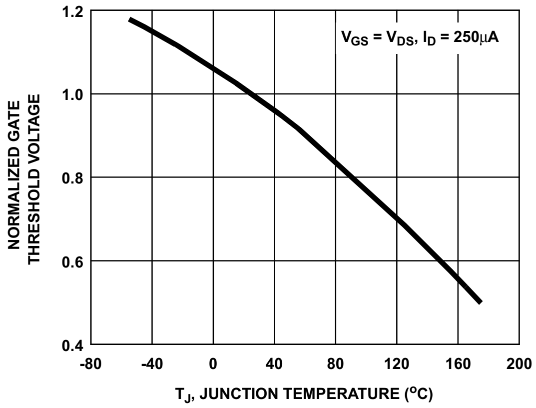



**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**

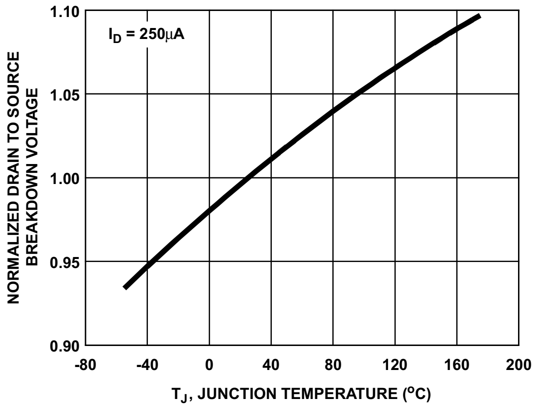



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**

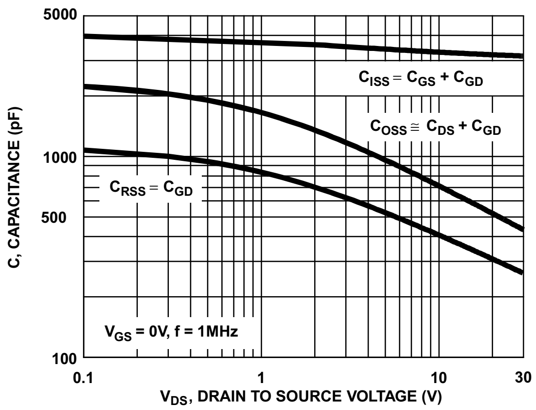



**Figure 13. Capacitance vs Drain to Source Voltage**

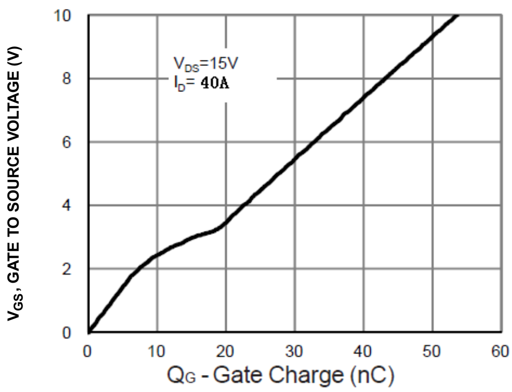



**Figure 14. Gate Charge Waveforms for Constant Gate Current**

## Test Circuits and Waveforms

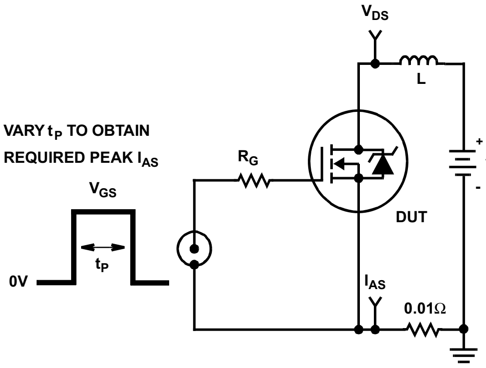



Figure 15. Unclamped Energy Test Circuit

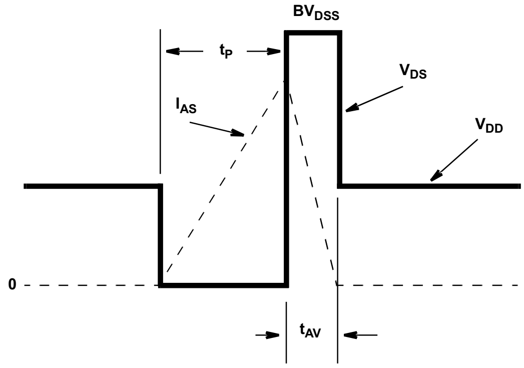



Figure 16. Unclamped Energy Waveforms

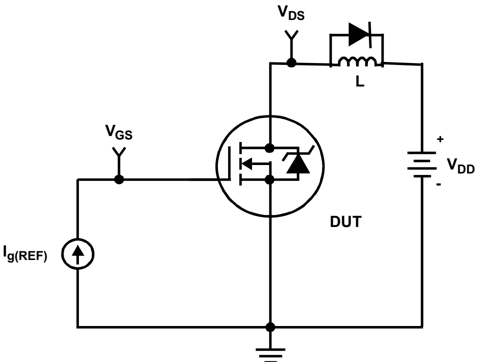



Figure 17. Gate Charge Test Circuit

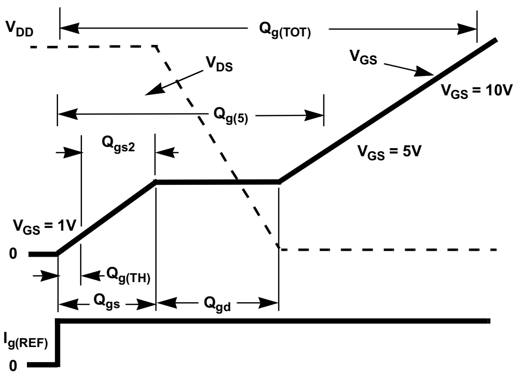



Figure 18. Gate Charge Waveforms

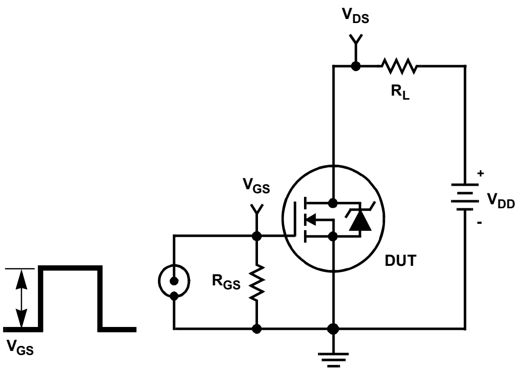



Figure 19. Switching Time Test Circuit

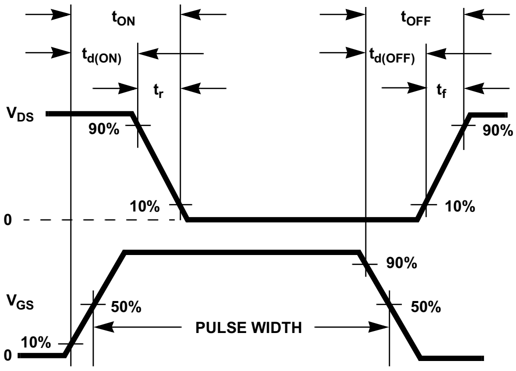
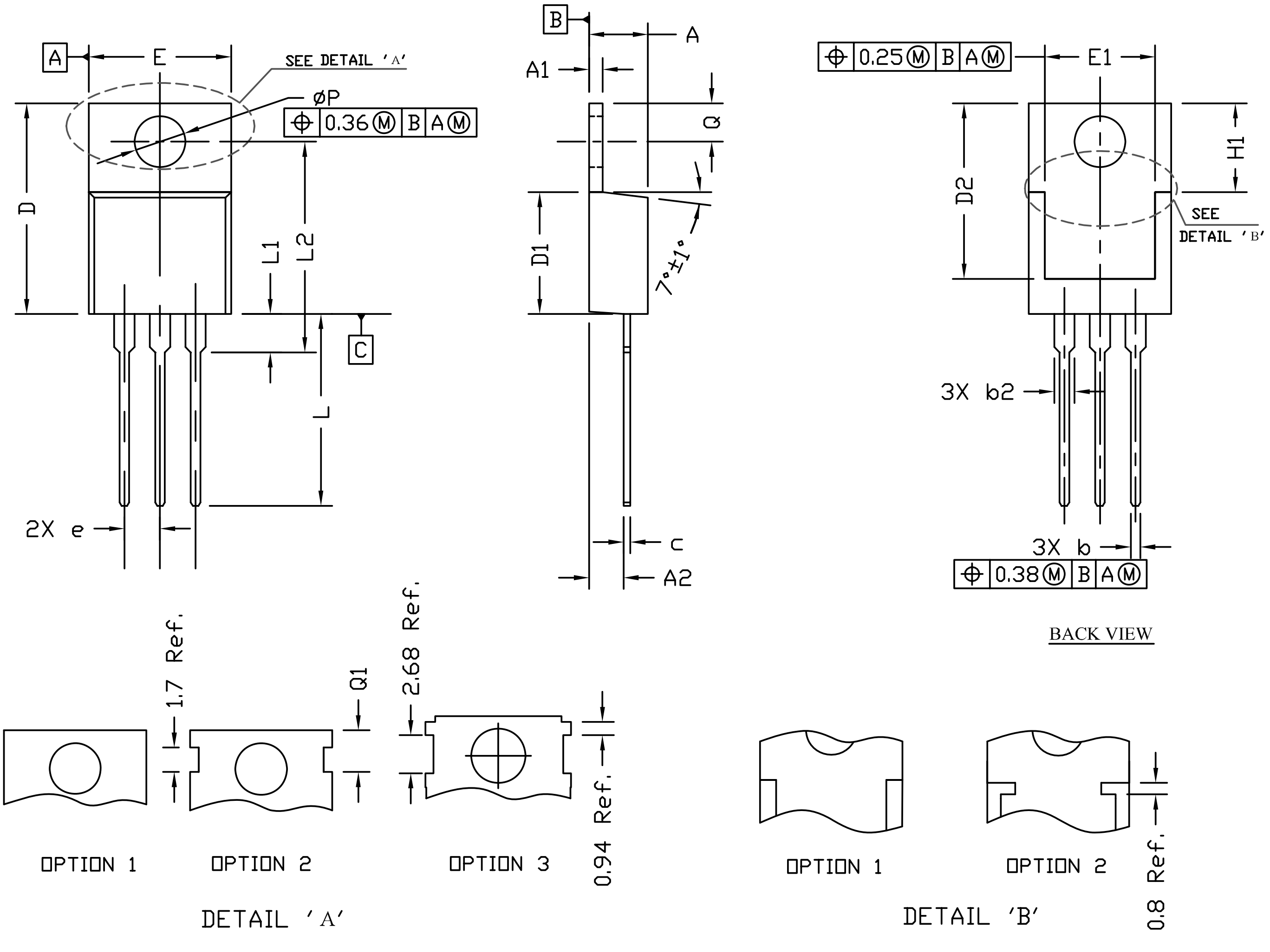


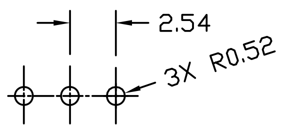

Figure 20. Switching Time Waveforms

| Document No. | PO-00015 |
|---|---|
| Version | L |

# TO220 PACKAGE OUTLINE




## RECOMMENDATION OF HOLE PATTERN




UNIT: mm

| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 4.30 | 4.45 | 4.72 | 0.169 | 0.175 | 0.186 |
| A1 | 1.15 | 1.27 | 1.40 | 0.045 | 0.050 | 0.055 |
| A2 | 2.20 | 2.67 | 2.90 | 0.087 | 0.105 | 0.114 |
| b | 0.69 | 0.81 | 0.95 | 0.027 | 0.032 | 0.037 |
| b2 | 1.17 | 1.37 | 1.45 | 0.046 | 0.050 | 0.068 |
| c | 0.36 | 0.38 | 0.60 | 0.014 | 0.015 | 0.024 |
| D | 14.50 | 15.44 | 15.80 | 0.571 | 0.608 | 0.622 |
| D1 | 8.59 | 9.14 | 9.65 | 0.338 | 0.360 | 0.380 |
| D2 | 11.43 | 11.73 | 12.48 | 0.450 | 0.462 | 0.491 |
| e | 2.54 BSC | | | 0.100 BSC. | | |
| E | 9.66 | 10.03 | 10.54 | 0.380 | 0.395 | 0.415 |
| E1 | 6.22 | --- | --- | 0.245 | --- | --- |
| H1 | 6.10 | 6.30 | 6.50 | 0.240 | 0.248 | 0.256 |
| L | 12.27 | 12.82 | 14.27 | 0.483 | 0.505 | 0.562 |
| L1 | 2.47 | --- | 3.90 | 0.097 | --- | 0.154 |
| L2 | --- | --- | 16.70 | --- | --- | 0.657 |
| Q | 2.59 | 2.74 | 2.89 | 0.102 | 0.108 | 0.114 |
| ØP | 3.50 | 3.84 | 3.89 | 0.138 | 0.151 | 0.153 |
| Q1 | 2.70 | --- | 2.90 | 0.106 | --- | 0.114 |

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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### Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.