

MT3114

N-Channel Power MOSFET

100V, 140A, 5.6mΩ

Features

- $R_{DS(on)} = 5.6m\Omega$ / $V_{GS} = 10V$, $I_D = 75A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extr emely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

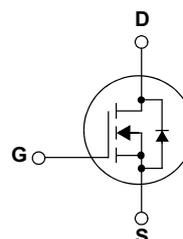
- DC-DC primary bridge
- DC-DC Synchronous rectification
- Hot swap



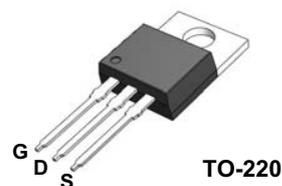
MT Semiconductor®

<http://www.mtsemi.com>

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units	
V_{DSS}	Drain to Source Voltage	100	V	
V_{GSS}	Gate to Source Voltage	± 20	V	
I_D	Drain Curren - Continuous (Silicon Limited) $T_C = 25^\circ C$	140	A	
	- Continuous(Package Limited) $T_C = 25^\circ C$	120		
	- Continuous $T_C = 25^\circ C$ (Note 1a)	97	A	
	- Pulsed	550		
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	980	mJ	
P_D	Power Dissipation	- $T_C = 25^\circ C$ (Note 1a)	330	W
		- $T_A = 25^\circ C$ (Note 1b)	2.2	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ C$	

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	0.45	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	62	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT3114	MT3114	TO-220	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.064	-	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 75\text{A}$	-	5.6	7.0	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{V}, I_D = 75\text{A}$	-	160	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	7670	-	pF
C_{oss}	Output Capacitance		-	540	-	pF
C_{rss}	Reverse Transfer Capacitance		-	210	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 80\text{V}, I_D = 75\text{A}$ $V_{GS} = 10\text{V}$	-	170	-	nC
Q_{gs}	Gate to Source Gate Charge		-	24	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	25	-	nC

Switching Characteristics

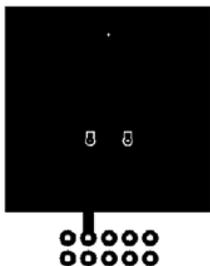
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}, I_D = 75\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 4.7\Omega$	-	22	54	ns
t_r	Turn-On Rise Time		-	54	118	ns
$t_{d(off)}$	Turn-Off Delay Time		-	37	84	ns
t_f	Turn-Off Fall Time		-	11	32	ns

Drain-Source Diode Characteristics

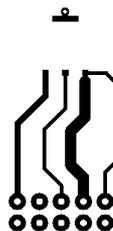
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 75\text{A}$ (Note 2)	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 75\text{A}, V_{DD} = 80\text{V}$	-	72	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt = 100\text{A}/\mu\text{s}$	-	129	-	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 40 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b) 62.5 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.
3. Starting $T_J = 25^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 36.3\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ V}$.

Typical Performance Characteristics

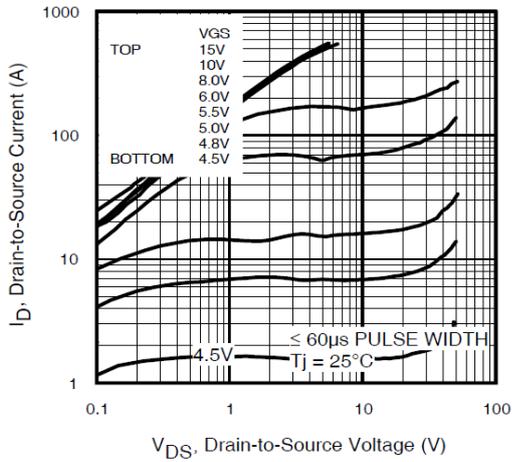


Fig 1. Typical Output Characteristics

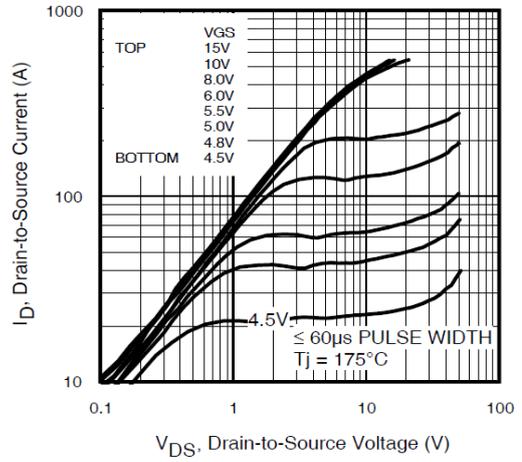


Fig 2. Typical Output Characteristics

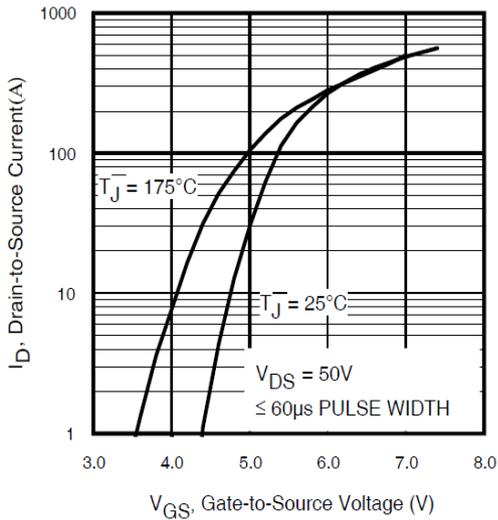


Fig 3. Typical Transfer Characteristics

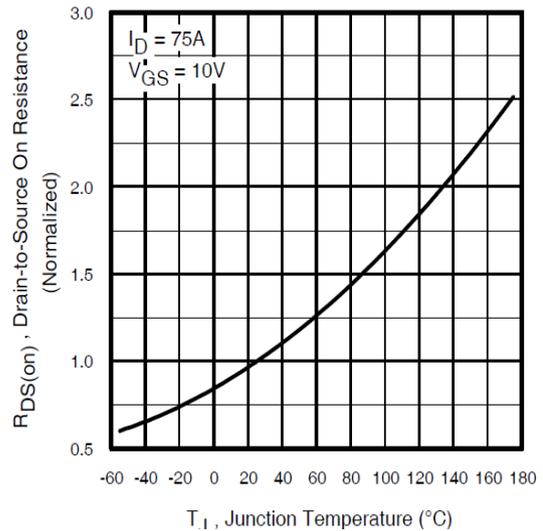


Fig 4. Normalized On-Resistance vs. Temperature

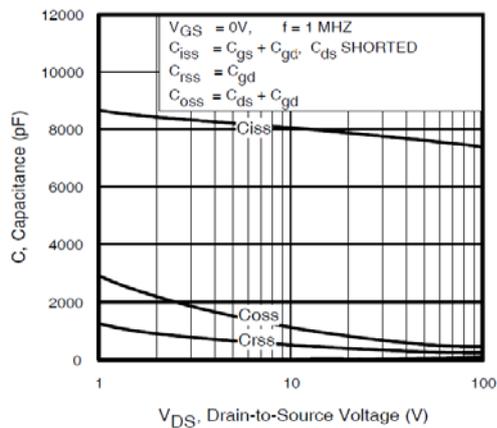


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

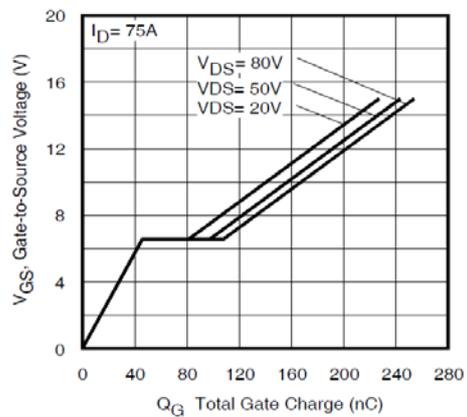


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

Typical Performance Characteristics

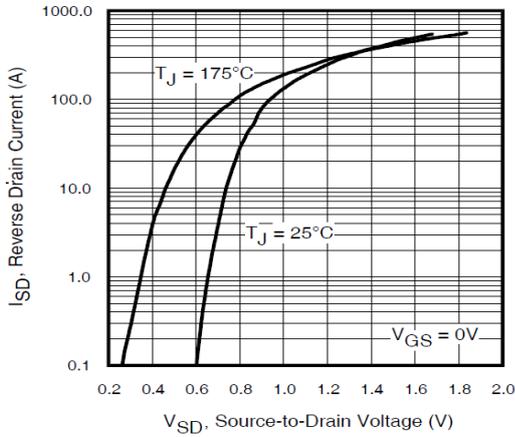


Fig 7. Typical Source-Drain Diode Forward Voltage

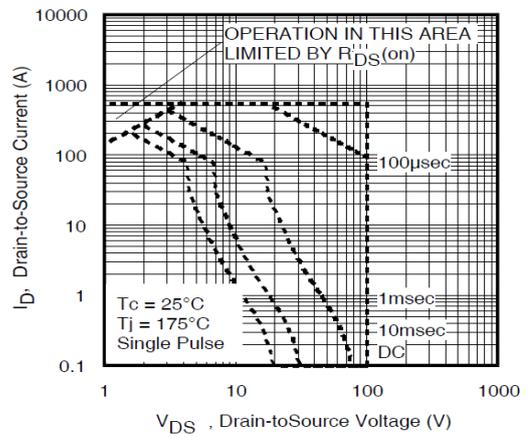


Fig 8. Maximum Safe Operating Area

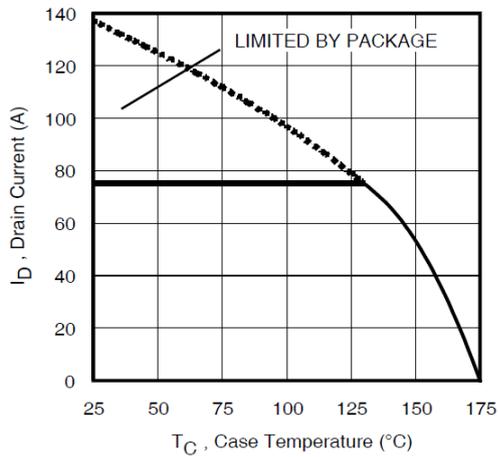


Fig 9. Maximum Drain Current vs. Case Temperature

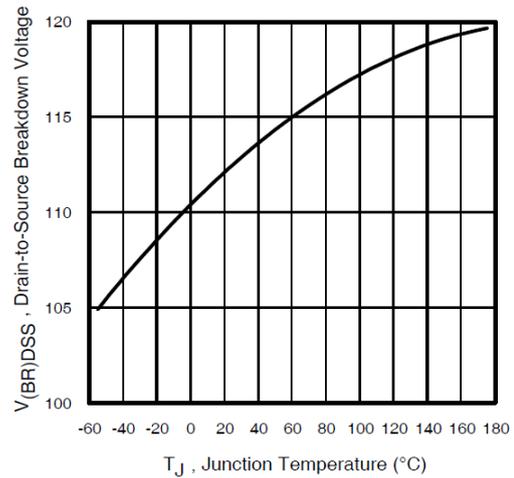


Fig 10. Drain-to-Source Breakdown Voltage

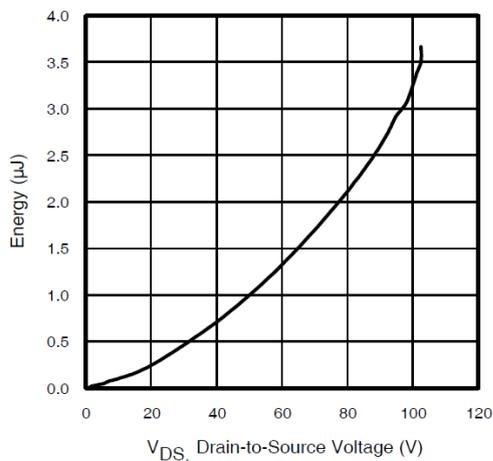


Fig 11. Typical C_{OSS} Stored Energy

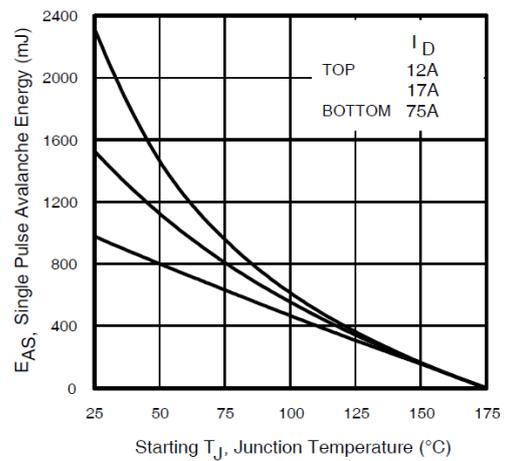


Fig 12. Maximum Avalanche Energy Vs. DrainCurrent

Typical Performance Characteristics

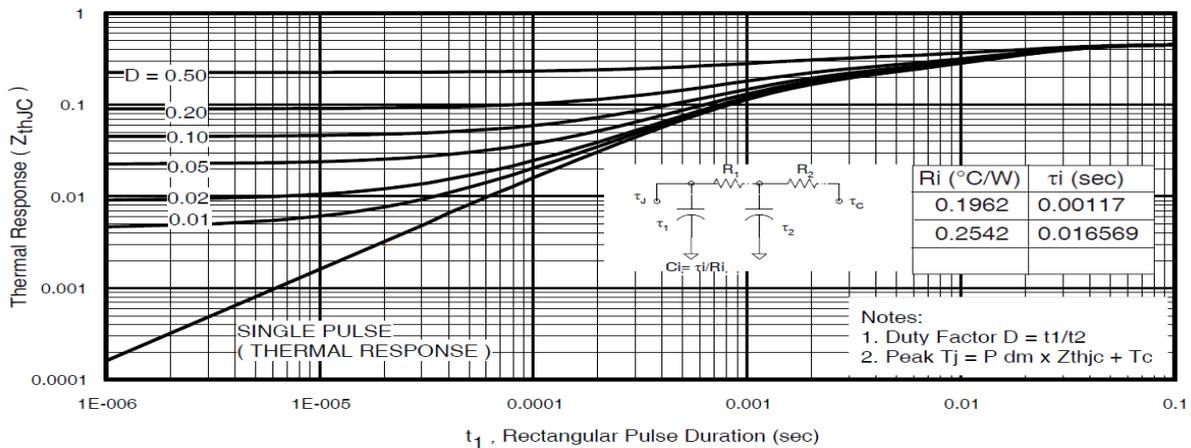


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

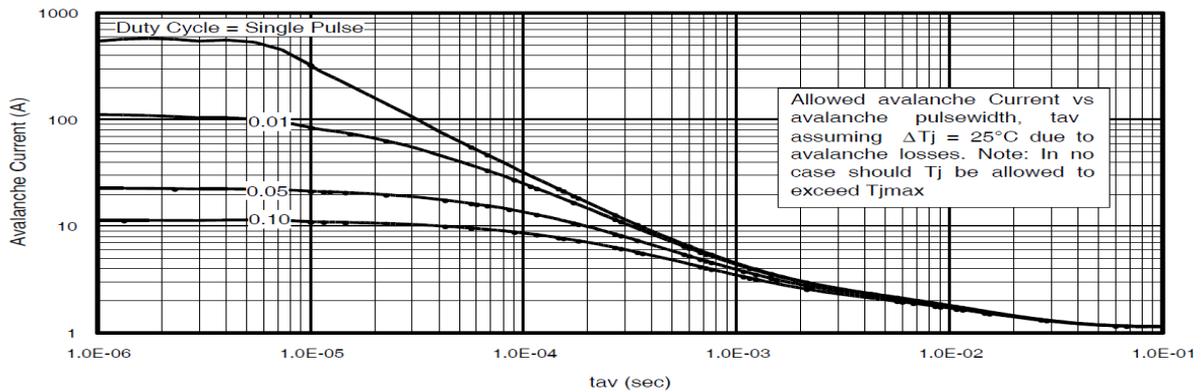


Fig 14. Typical Avalanche Current vs. Pulsewidth

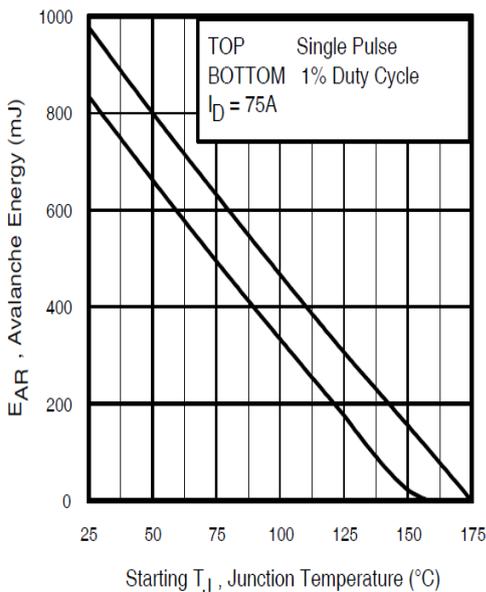


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 14, 15:
 (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. PD(ave) = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. Iav = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 14, 15).
 tav = Average time in avalanche.
 D = Duty cycle in avalanche = tav · f
 ZthJC(D, tav) = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

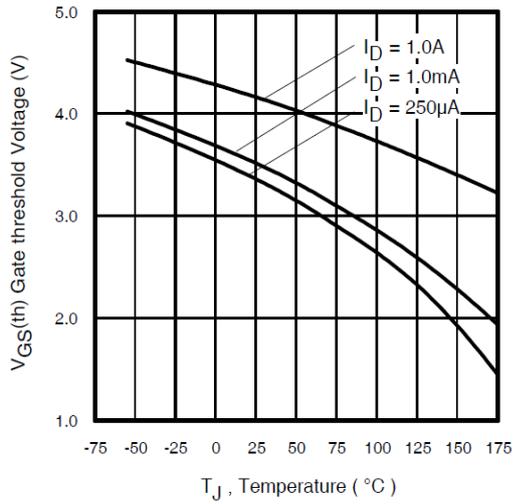


Fig 16. Threshold Voltage Vs. Temperature

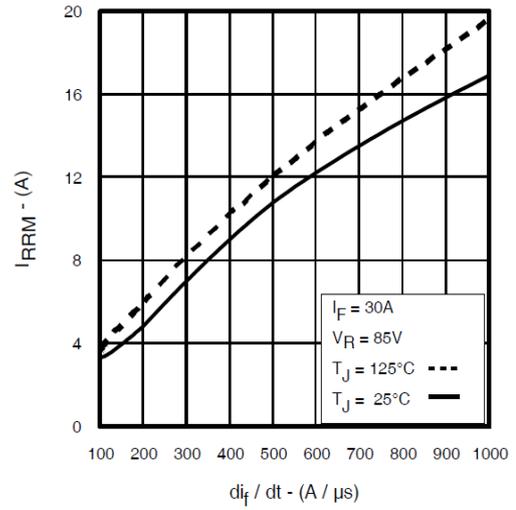


Fig. 17 - Typical Recovery Current vs. di/dt

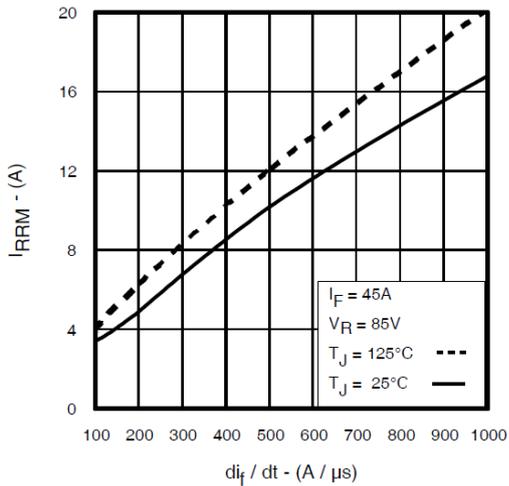


Fig. 18 - Typical Recovery Current vs. di/dt

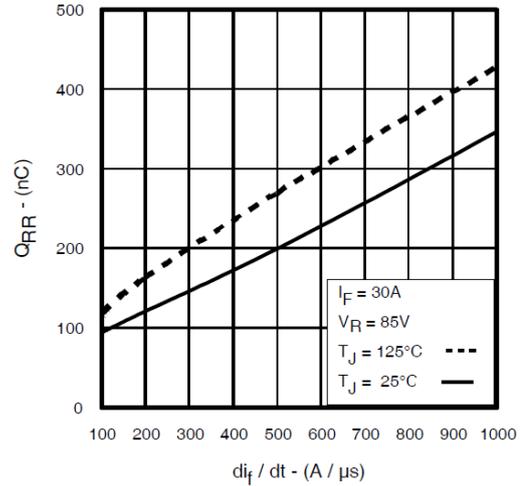


Fig. 19 - Typical Stored Charge vs. di/dt

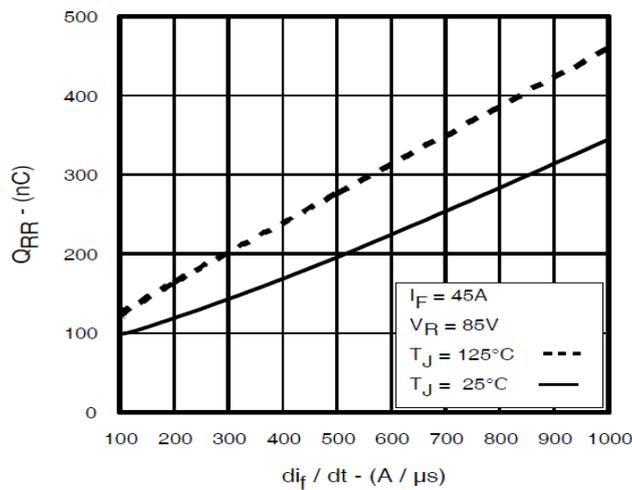
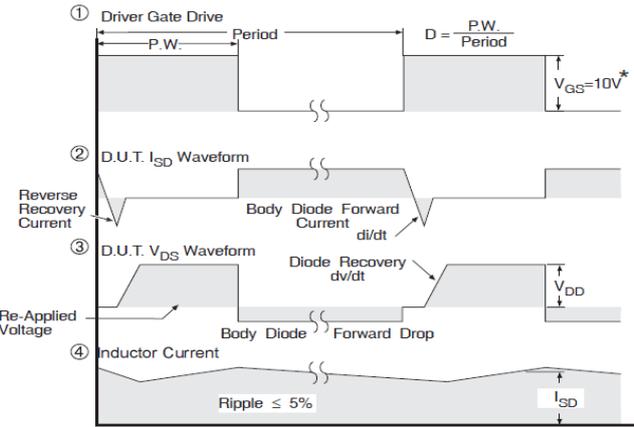
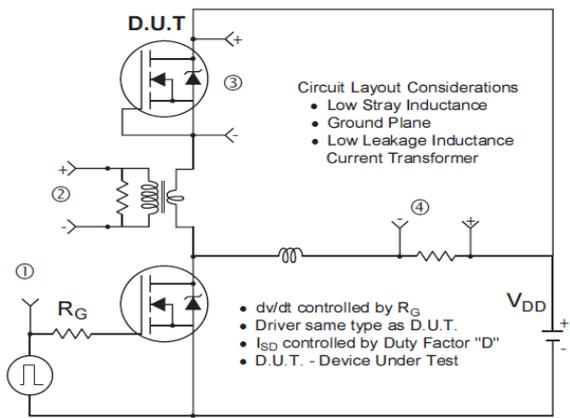


Fig. 20 - Typical Stored Charge vs. di/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel

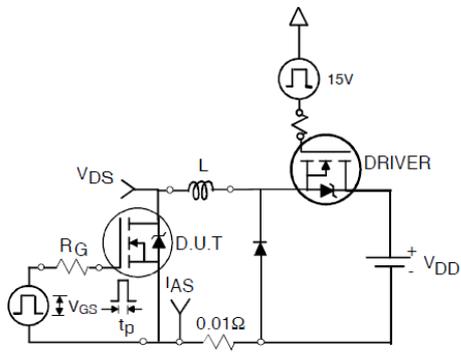


Fig 22a. Unclamped Inductive Test Circuit

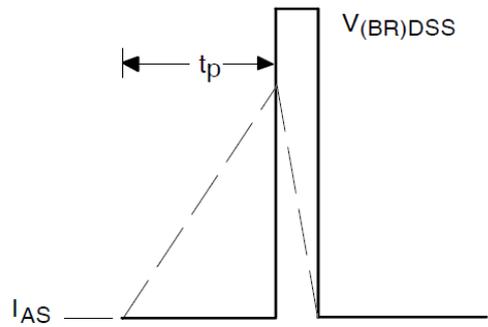


Fig 22b. Unclamped Inductive Waveforms

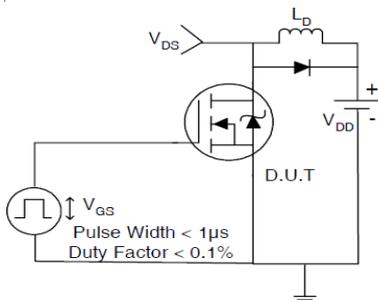


Fig 23a. Switching Time Test Circuit

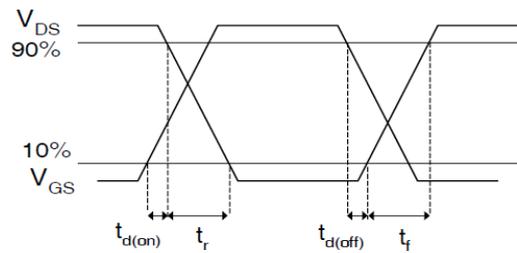


Fig 23b. Switching Time Waveforms

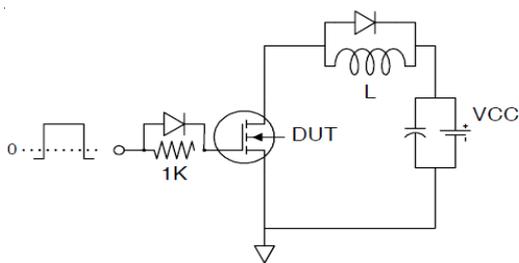


Fig 24a. Gate Charge Test Circuit

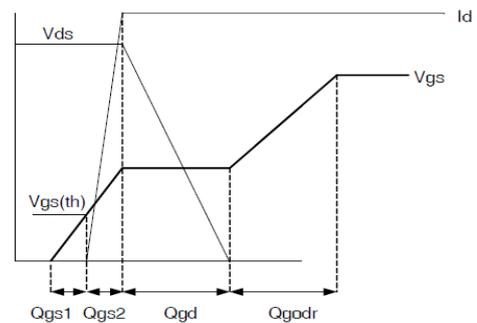


Fig 24b. Gate Charge Waveform

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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.