MT1530 UPSTREAM AMPLIFIER
ADVANCE DATA SHEET

1 APPLICATIONS

- Cable modems
- Telephony over cable
- Set-top box CATV

2 FEATURES

- Lowest power consumption upstream amplifier available
- Maximum output level of 64 dBmV
- Low power-up/down transients of 4 mV_{p-p} typical at 59 dBmV output
- Best in class second harmonic distortion
- Ultra low third harmonic distortion
- Single +5V supply
- 63-dB Gain range
- Gain programmable in 1-dB steps
- Low transmit output noise floor: 131 nV / √Hz
- Low transmit-disable output noise: 810 pV / √Hz
- Two power-down modes
- DOCSIS and EuroDOCSIS compatible

3 OVERVIEW

The Microtune 1530 (MT1530) is a low-cost programmable-gain power amplifier IC for use in CATV upstream applications. Specifically, the MT1530 is optimized for the DOCSIS upstream standard.

The device operates at a frequency range from 5 MHz to 65 MHz, and can output 64 dBmV through a 4:1 impedance-ratio transformer. Second harmonic distortion is typically less than -70 dBc, and third harmonic distortion is typically less than -55 dBc at a 59 dBmV output level. A 3-wire digital serial bus controls the variable gain, with gain control available in 1-dB steps and a nominal 63-dB gain range.

The MT1530 may be disabled via an external control pin. The transmit-disable mode not only minimizes output noise by shutting off the output stage, but also maintains its output impedance at nominal levels. Output glitch transients are nominally less than 4 mV at maximum gain settings during transmit enable/disable switching.

Operating from a single +5V supply, the amplifier's typical current draw at maximum gain, or minimum attenuation, is 102 mA. Additionally, internal circuitry reduces the amplifier's power consumption depending on gain setting. Transmit-disable mode power supply current is reduced to a nominal of 14 mA. A shutdown mode further reduces current to a nominal of 130 µA.

The MT1530 is available in a 20-pin SSOP package for the extended industrial temperature range of -40°C to +85°C.

4 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 1 may cause permanent damage to the device. These are stress ratings only; functional operation of the device under conditions other than those listed in the operational sections of this document is not recommended or implied. Exposure to any of the absolute-maximum rating conditions for extended periods of time may affect reliability.

Table 1 Stress Ratings

PARAMETER	MIN	MAX	UNIT
V_{CC} (V_{CC1}, V_{CC2})	-0.7	6	V
V_{OUT+}, V_{OUT-}	-0.7	7.5	V
Input voltage levels (all inputs), VCM	–0.7	V_{CC} + 0.7	V
Junction temperature		+150	°C
Storage temperature range	-55	+150	°C
Lead temperature (soldering, 10 seconds)		+300	°C

5 DC ELECTRICAL CHARACTERISTICS

The DC electrical characteristics listed in Table 2 are valid for the following conditions unless otherwise noted. Typical parameters are at T_A = +25°C.

- V_{CC} = +4.75V to +5.25V
- TXEN = high
- D7 = 1
- T_A = -40°C to +85°C

Table 2 DC Electrical Characteristics

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage		V_{CC}	4.75		5.25	V
Supply current, transmit mode	Gain code = 52 to 63	I_{CC}		102	129	mA
	Gain code = 46 to 51			59	75	
	Gain code = 45 to 0			37	47	
Supply current, transmit-disable mode (TXEN = low)		I_{CC}		14	19	mA
Supply current, shutdown mode (D7 = 0 or $\overline{SHDN}$ = 0)		I_{CC}		131	164	µA
Input high voltage		V_{IH}	2.0			V
Input low voltage		V_{IL}			0.8	V
Input high current		I_{IH}		0		µA
Input low current		I_{IL}		0		µA

6 AC ELECTRICAL CHARACTERISTICS

The AC electrical characteristics listed in Table 3 are valid for the following conditions unless otherwise noted. Typical parameters are at T_A = +25°C.

- V_{CC} = +4.75V to +5.25V
- TXEN = $\overline{\text{SHDN}}$ = high
- D7 = 1
- V_{IN} = 33 dBmV differential
- Output impedance = 75Ω through a 4:1 impedance transformer
- T_A = -40°C to +85°C

Table 3 AC Electrical Characteristics of the MT1530

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Voltage gain	A_V	F_{IN} = 5 MHz to 42 MHz	Gain control word = 0	-33.6	-32.4	-31.1	dB
			Gain control word = 63	28.1	30.8	32.1	dB
Gain rolloff		V_{OUT} = 59 dBmV, F_{IN} = 42 MHz[1]			-0.25	-0.5	dB
		V_{OUT} = 59 dBmV, F_{IN} = 65 MHz[1]			-0.9	-1.5	dB
1 dB Compression point	P_{1dB}	A_V = 29 dB, 42 MHz[1]		65	67		dBmV
Output step size		F_{IN} = 5 MHz to 42 MHz		0.7	1	1.3	dB
Transmit mode noise		A_V = 26 dB[1]			131	150	nV / √Hz
		A_V = -26 dB[1]			8.5	10.1	nV / √Hz
Transmit-disable mode noise		TXEN = low, A_V = 26 dB, F_{IN} = 5 MHz to 65 MHz			810		pV / √Hz
Isolation in transmit-disable mode		TXEN = low, gain control word = 63, F_{IN} = 65 MHz			69		dB
TXEN Transient duration		TXEN rise/fall time < 0.1µs			1.5		µs
TXEN Transient step size		Gain setting = 63[2]			4	16	mVp-p
		Gain setting = 51 or lower[2]			2	8	mVp-p
Input impedance	Z_{IN}	F_{IN} = 5 MHz to 65 MHz, single-ended[2]		1.35	1.85		kΩ
Output impedance	Z_{OUT}				75		Ω
Output return loss	R_L	F_{IN} = 5 MHz to 65 MHz[1]		10.7	15		dB
Third-order output intercept	OIP3	Input tones at 65 MHz and 66 MHz, V_{IN} = 28 dBmV/tone, V_{OUT} = 53 dBmV/tone[2]		80	84		dBmV
2nd Harmonic distortion	HD2	F_{IN} = 33 MHz, V_{OUT} = +59 dBmV			-72	-66	dBc
		F_{IN} = 65 MHz, V_{OUT} = +59 dBmV			-70	-64	dBc
3rd Harmonic distortion	HD3	F_{IN} = 22 MHz, V_{OUT} = +59 dBmV			-59	-55	dBc
		F_{IN} = 65 MHz, V_{OUT} = +59 dBmV			-55	-51	dBc

1 Referenced to 10 MHz.
2 Guaranteed by design.

7 TYPICAL PERFORMANCE

The following data is representative of a part measured in a typical application circuit.

- 4:1 impedance ratio balun on the output
- Z_{load} = 75Ω, Vcc = 5V
- T_A = 25°C

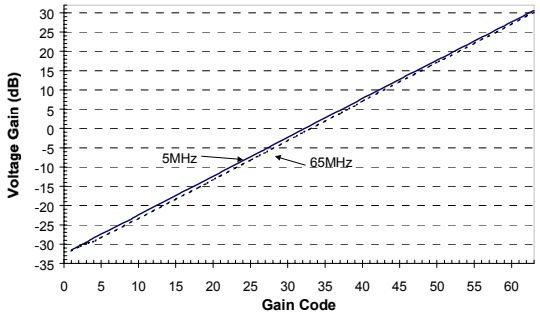


Figure 1 Voltage Gain vs. Gain Code

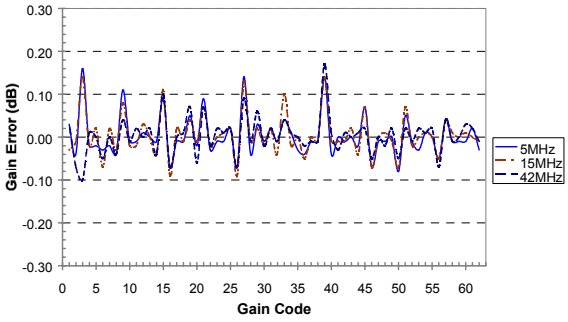


Figure 2 Differential Gain Linearity vs. Gain Code

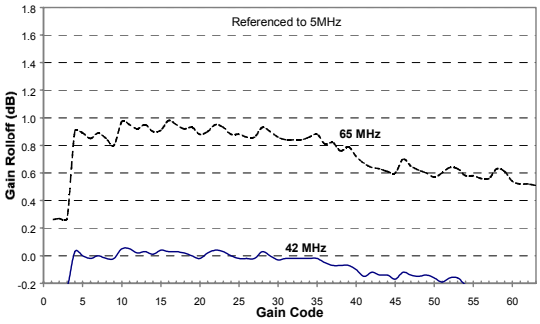


Figure 3 Gain Rolloff vs. Gain Code

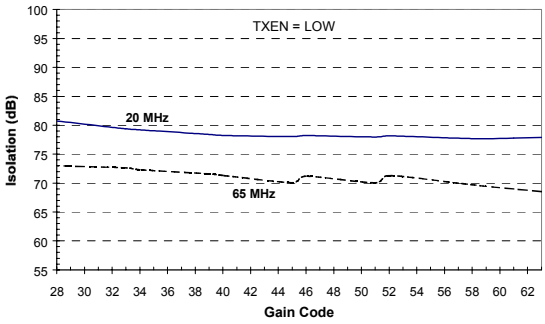


Figure 4 Input-Output Isolation vs. Gain Code

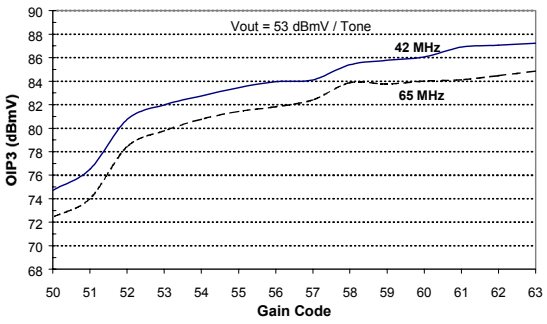


Figure 5 Third-Order Output Intercept vs. Gain Control

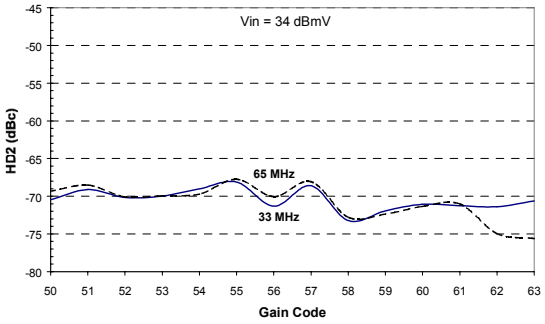


Figure 6 Second-Order Harmonic Distortion vs. Gain Code

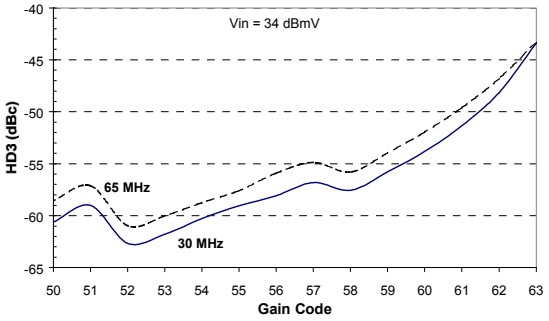


Figure 7 Third-Order Harmonic Distortion vs. Gain Code

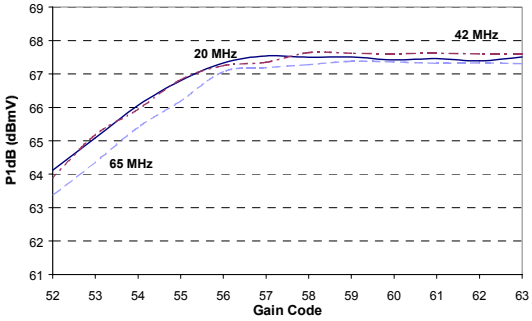


Figure 8 Output 1 dB Compression Point vs. Gain and Frequency

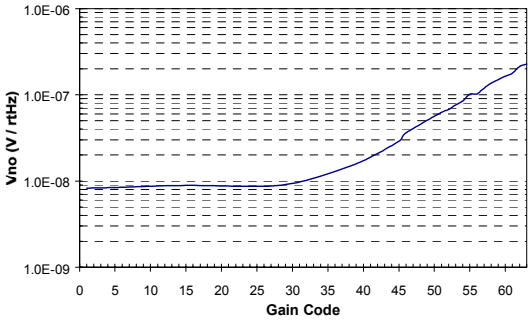


Figure 9 Output Noise vs. Gain Code

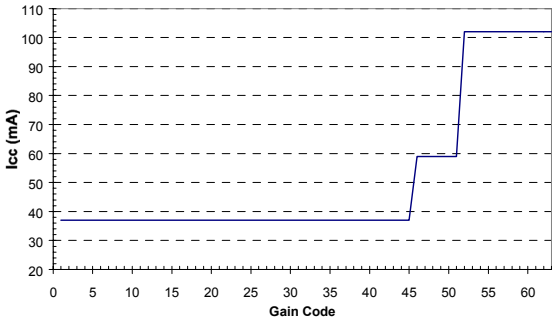


Figure 10 Power Supply Current vs. Gain Code

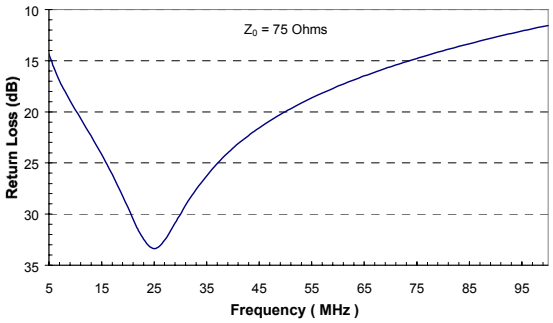


Figure 11 Output Return Loss vs. Frequency

8 DETAILED DESCRIPTION

This section describes the MT1530 functional blocks shown in Figure 12.

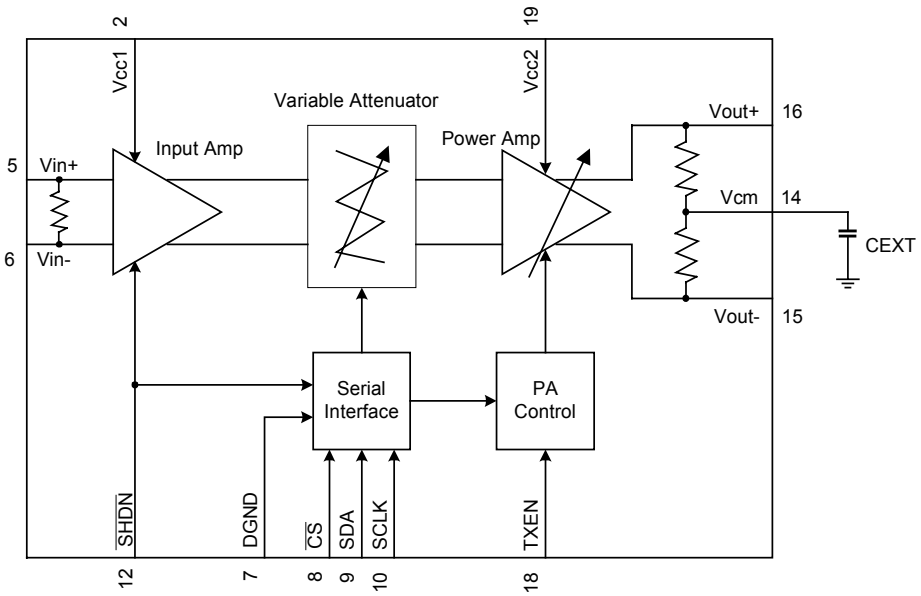


Figure 12 MT1530 Amplifier Block Diagram

8.1 FUNCTIONAL MODES

The MT1530 amplifier has three functional modes controlled through the serial interface or external pins: transmit mode, transmit-disable mode, and shutdown mode.

8.1.1 TRANSMIT MODE

Transmit mode is the normal active mode of the MT1530. The TXEN and $\overline{\text{SHDN}}$ pins must be held high in this mode.

8.1.2 TRANSMIT-DISABLE MODE

Transmit-disable mode is typically used between bursts in TDMA systems. This mode shuts off the power amplifier while keeping the input amplifier and variable attenuator powered up. Taking TXEN low while keeping $\overline{\text{SHDN}}$ high and D7 = 1 (see Table 5) activates this mode.

8.1.3 SHUTDOWN MODE

Shutdown mode minimizes current consumption while maintaining the programmed gain state stored in the latch of the serial interface. All analog functions are disabled in this mode and current consumption is reduced to 131 µA (typical). Shutdown mode is enabled when either D7 = 0 or $\overline{\text{SHDN}}$ is set low. This mode overrides the TXEN input pin, but TXEN should be held low to minimize glitching when exiting this mode.

8.2 IC ARCHITECTURE

The MT1530's signal path consists of an input amplifier, a variable attenuator, and a power amplifier as shown in Figure 12. The input amplifier is a fixed-gain, low-noise, differential amplifier with a nominal input impedance of 1.85 kΩ. The variable attenuator is capable of a 51-dB attenuation range in 1-dB steps. The output power amplifier has 12 dB of gain range in 6 dB steps.

8.2.1 INPUT AMPLIFIER

The input amplifier (IA) is a fully differential, low-noise amplifier with no gain adjustment. Its bias may be disabled either by the external $\overline{\text{SHDN}}$ pin, or D7 of the serial control register.

For best second-order performance, the IA should be driven differentially. However, the device may be driven in a single-ended mode, with the other unused input bypassed to ground with a 10 nF capacitor. The IA's inputs are self-biasing and must be AC coupled.

8.2.2 VARIABLE ATTENUATOR

The variable attenuator (VA) provides up to 51 dB attenuation of the input signal in nominal 1-dB increments. The architecture is fully differential to minimize glitching and even-order harmonics. This attenuator acts together with the output power amplifier to achieve a nominal 63 dB of gain range, as described in section 8.2.3.

8.2.3 OUTPUT POWER AMPLIFIER

The output power amplifier (PA) is a fully differential amplifier capable of driving +64 dBmV into a 75Ω load. An off-chip transformer must be used to convert from a differential to a single-ended output. The PA's output impedance is nominally 300Ω, which is transformed to 75Ω by the 4:1 impedance ratio transformer. This impedance is maintained when the amplifier is powered down by setting TXEN = low. The amplifier's outputs are powered by +5V connected to the center tap of the transformer's secondary.

The differential nature of the PA provides superior second-order harmonic performance. Additionally, any single-ended transients on the amplifier's outputs that are generated during transmit enable/disable switching are cancelled by this architecture.

In addition to providing output power, the PA also plays a role in the gain-programmability of the IC. The output amplifier has attenuation settings of 0, 6, and 12 dB. Higher attenuations reduce output power and noise. The programmed gain control code automatically sets the PA's attenuation. Gain control codes of 52 through 63 set the PA's attenuation to 0 dB, putting the PA at maximum power. Gain control codes of 46 to 51 set the PA's attenuation to 6 dB, lowering its power by half. Gain control codes of less than 46 set the PA's attenuation to 12 dB, lowering its power to one quarter of the maximum value. Transmit-disable and shutdown modes turn off power to the PA for maximum isolation and minimum output noise.

8.2.4 PA CONTROL

The PA Control (PAC) both adjusts the output amp's gain, and manages power-up and power-down transients. The PAC uses internal timing circuits to control the ramp-up and ramp-down of the PA's bias block. This orderly ramp keeps the PA's output glitch to very low levels.

The PAC begins a bias ramp-down on the falling edge of TXEN. A rising TXEN produces a bias ramp-up. Note that for a minimum glitch on the output, the rest of the IC must already be powered up by having disabled shutdown mode.

8.3 SERIAL INTERFACE

The serial interface (SI) programs the gain of the MT1530 using an 8-bit control word. The SI uses the gain control word to set the VA's and PA's gains individually using an internal decoder. It has an active-low chip-select ($\overline{CS}$) to synchronize to the incoming word. Data is clocked MSB first on the rising edge of SCLK. Data is latched on the rising edge of $\overline{CS}$. Table 4 and Table 5 show the register format. Figure 13 illustrates serial interface timing.

Table 4 Serial Interface Control Word

BIT	MNEMONIC	DESCRIPTION
7 (MSB)	D7	Software shutdown (active low)
6	D6	Unused (Don't Care)
5	D5	Gain control, Bit 5
4	D4	Gain control, Bit 4
3	D3	Gain control, Bit 3
2	D2	Gain control, Bit 2
1	D1	Gain control, Bit 1
0 (LSB)	D0	Gain control, Bit 0

Table 5 Chip State Control Bits

$\overline{\text{SHDN}}$	TXEN	D7	D6	D5	D4	D3	D2	D1	D0	GAIN STATE (DECIMAL)	STATE
0	0	X	X	X	X	X	X	X	X	X	Shutdown mode
X	0	0	X	X	X	X	X	X	X	X	Software shutdown mode
1	0	1	X	X	X	X	X	X	X	X	Transmit-disable mode
1	1	1	X	X	X	X	X	X	X	X	Transmit mode
1	1	1	X	0	0	0	0	0	0	0	Gain = -32 dB[1]
1	1	1	X	0	0	0	0	0	1	1	Gain = -31 dB[1]
1	1	1	X	1	0	0	0	0	0	32	Gain = 0 dB[1]
1	1	1	X	1	1	1	1	1	0	62	Gain = 30 dB[1]
1	1	1	X	1	1	1	1	1	1	63	Gain = 31 dB[1]

[1] Typical gain at +25°C, VCC = +5V, Fin = 20 MHz

Table 6 Timing Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
$\overline{CS}$ to SCK rise setup time	t_{SENS}	10			ns
$\overline{CS}$ to SCK rise hold time	t_{SENH}	20			ns
SDA to SCK setup time	t_{SDAS}	10			ns
SDA to SCK hold time	t_{SDAH}	20			ns
SDA pulse width high	t_{DATAH}	50			ns
SDA pulse width low	t_{DATAL}	50			ns
SCK pulse width high	t_{SCKH}	50			ns
SCK pulse width low	t_{SCKL}	50			ns

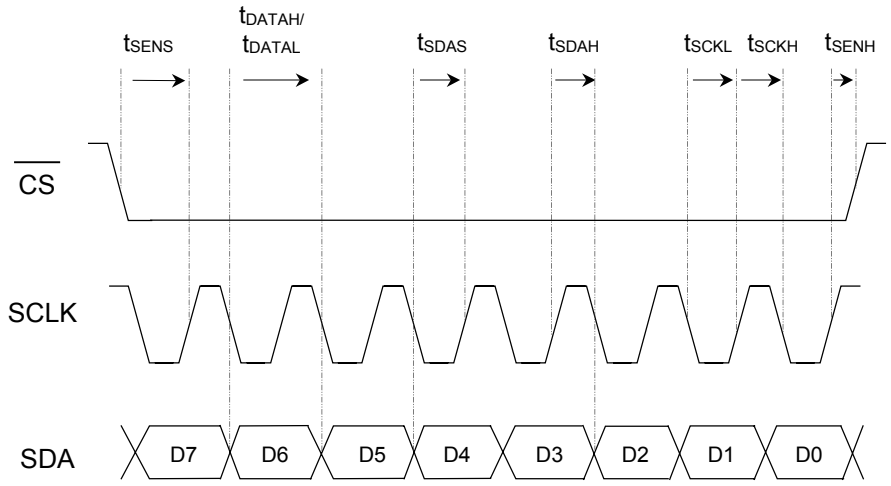


Figure 13 Serial Interface Timing Diagram

9 TERMINAL CONNECTIONS

Terminal connections for the MT1530 are described in Table 7.

Table 7 Terminal Connections

PIN	FUNCTION/ SYMBOL	DESCRIPTION
1	GND	Ground connection
2	VCC1	+5V Power supply for the input amplifier, variable attenuator, and serial interface. Bypass to GND1 with a 0.1 µF decoupling capacitor as close to the part as possible.
3	NC	No connect
4	GND1	Ground connection for the input amplifier and variable attenuator
5	VIN+	Positive input to the input amplifier
6	VIN-	Negative input to the input amplifier. Bypass with capacitor if driving amplifier single-ended.
7	DGND	Ground connection to serial interface
8	$\overline{CS}$	Chip select input to serial interface (active low)
9	SDA	Data input to serial interface (active high)
10	SCLK	Clock input to serial interface (positive-edge triggered)
11	NC	No connect
12	$\overline{SHDN}$	Shutdown mode input (active low)
13	NC	No connect
14	VCM	Output common-mode bypass. Bypass to GND2 with 0.1 µF capacitor.
15	VOUT-	PA negative output
16	VOUT+	PA positive output
17	NC	No connect
18	TXEN	PA output enable input (active high)
19	VCC2	+5V Power supply for PA bias and control circuitry. Bypass to GND2 with a 0.1 µF decoupling capacitor as close to the part as possible.
20	GND2	Ground connection for the PA

10 PIN CONFIGURATION

Top View

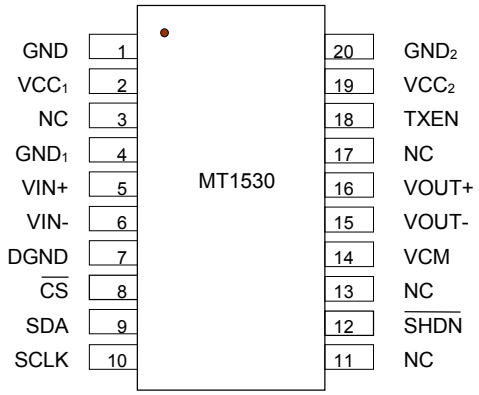
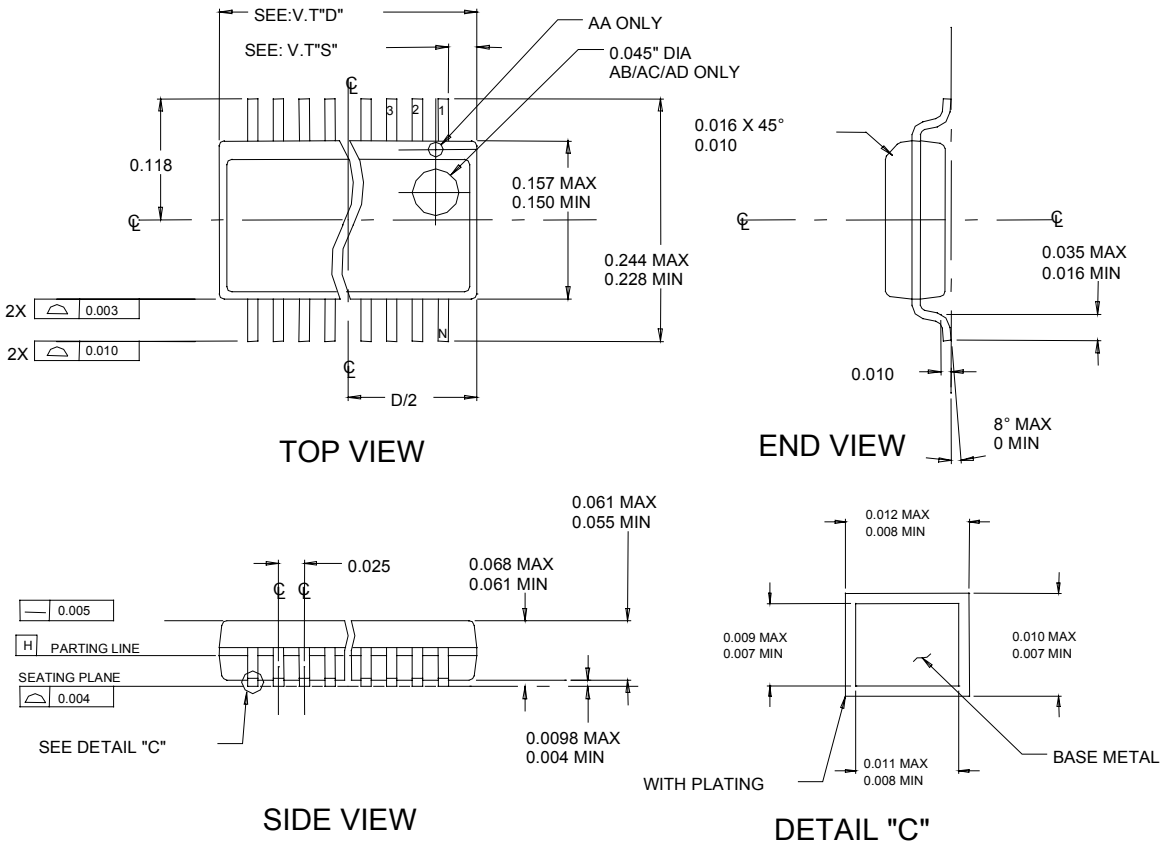


Figure 14 Pin Diagram

11 PACKAGE DRAWING



CONTROLLING DIMENSION: INCHES

VARI-ATIONS	V.T."D"			V.T."S"			N
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
AA	0.189	0.194	0.196	0.002	0.005	0.007	16
AB	0.337	0.342	0.344	0.050	0.053	0.055	20
AC	0.337	0.342	0.344	0.025	0.028	0.030	24
AD	0.386	0.391	0.393	0.025	0.028	0.030	28

THIS PACKAGE MEETS JEDEC REGISTRATION MO-137AA-AF
EXCEPT FOR THE PKG THICKNESS, DIM 0.061 MAX.

Figure 15 MT1530 Package Drawing

NOTICES

World Headquarters
Microtune, Inc.
2201 Tenth Street
Plano, TX 75074

Telephone: 972-673-1600
Fax: 972-673-1602
Email: sales@microtune.com
Website: www.microtune.com

European Headquarters
Microtune GmbH and Co. KG
Marie Curie Strasse 1
85055 Ingolstadt / Germany

Telephone: +49-841-9378-011
Fax: +49-841-9378-010
Sales Telephone: +49-841-9378-020
Sales Fax: +49-841-9378-024

Pan-Asian Headquarters
Microtune, Inc. - Hong Kong
Silvercord Tower 1, Room 503
30 Canton Road
Kowloon, Hong Kong

Telephone: +852-2378-8128
Fax: +852-2302-0756

For a detailed list of current sales representatives, visit our Web site at www.microtune.com.