

PIN Diode Shunt Switch Element

Rev. V1

Features

- Supports up to 40 W Power
- Low Insertion Loss:
 0.10 dB to 2.7 GHz
 0.25 dB to 6.0 GHz
- High Isolation:
 25 dB to 6.0 GHz
- RoHS* Compliant

Description

A broadband, high linearity, medium power shunt switch element in a 1.9 x 1.1 mm DFN package.

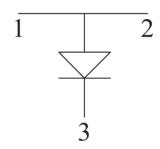
This device is designed for wireless telecommunications infrastructure and test instrument applications. It is also suited for other applications in $0.05 \sim 6$ GHz.



Part Number	Package		
MSWSH-040-30	3000 piece reel		



Pin Out / Schematic



Electrical Specifications: T_A = +25°C

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Breakdown Voltage (V _B)	I _R = 10 μA	V	500	_	_
Total Capacitance (C _T)	V _R = -50 V, 1 MHz	pF	_	0.42	_
Series Resistance (R _S)	I _F = 100 mA, 500 MHz	Ω	_	0.36	_
I-Region (W)	I-Layer	mm	_	40	_
Insertion Loss (I _L)	V _R = 10 V 2.7 GHz <6.0 GHz	dB	_	0.10 0.30	0.30 0.50
Isolation (I _{SO})	I _F = 100 mA 2.7 GHz <6.0 GHz	dB	29 24	32 36	_
Input / Output Return Loss (R _L)	V _R = 10 V 2.7 GHz <6.0 GHz	dB	18 13	22 15	_
Minority Carrier Lifetime (T _L)	I _F = 10 mA, I _R = 6 mA, @ 50%	ns	_	600	_

^{*} Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.



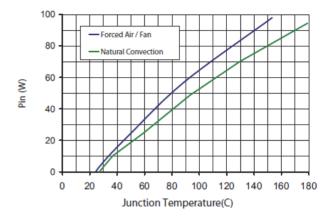
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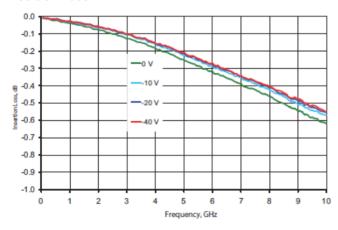
Absolute Maximum Ratings

Parameter	Absolute Maximum
Breakdown Voltage	500 V
Forward Current	500 mA
Thermal Resistance	10°C/W
Junction Temperature	+175°C
Storage Temperature	-65°C to +150°C
Assembly Temperature	+260°C Per JEDEC STD-J-20C

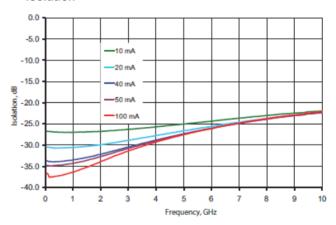
Junction Temperature vs. Power Mounted on Heatsink, +25°C, 1.3 GHz



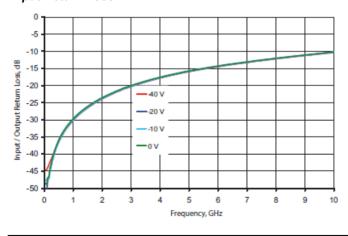
Insertion Loss



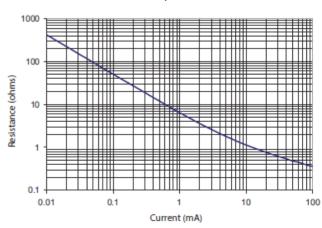
Isolation



Input Return Loss



Series Resistance vs. Bias, 500 MHz

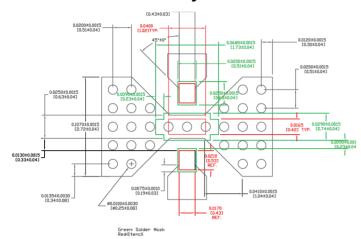




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Printed Circuit Board Layout

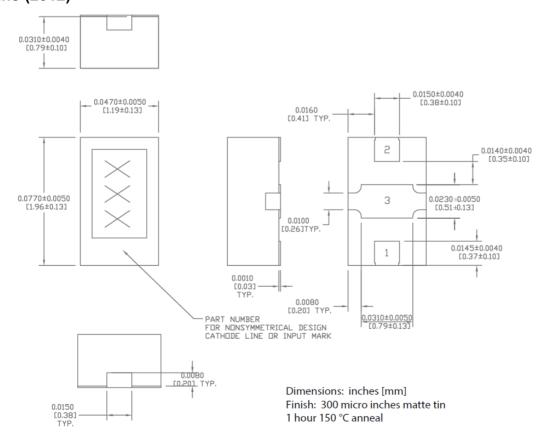


NOTE: If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

Solder mask should provide a 60 um clearance between copper pad and soldermask. Rounded pkg pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that only get 50% to 80% solder paste coverage.

Outline (2012)



MSWSH-040-30



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