July 1996

Features

- Work at 4.5V through 5.5V
- Single power voltage application
- Single chip recording & playing
- 300,000 hours nonvalatile voice storage typically, without battery backup
- 100,000 times recording typically
- 2 MHz optional external clock input if precise timing is demand
- 0 dB to 40 dB AGC is provided
- 16 ohm speaker could be driven in 75 mW
- 16 second capacity is provided at 8 KHz (20000h sample pixel)
- Up to 64 sections are provided
- No sound developing tool is needed
- 4 package types are provided : dice form, 300 mil 24L PDIP, 300 mil 24L SOG, 24L PLCC
- Two operation modes are provided : push botton mode and CPU addressing mode.
- On chip oscillator
- On chip voltage charge pump
- On chip microphone preamplifier with AGC
- On chip anti-aliasing circuit
- On chip EEPROM programming circuit
- On chip EEPROM erasing circuit
- Microphone reference pin is provided
- Audio input / output pins are provided

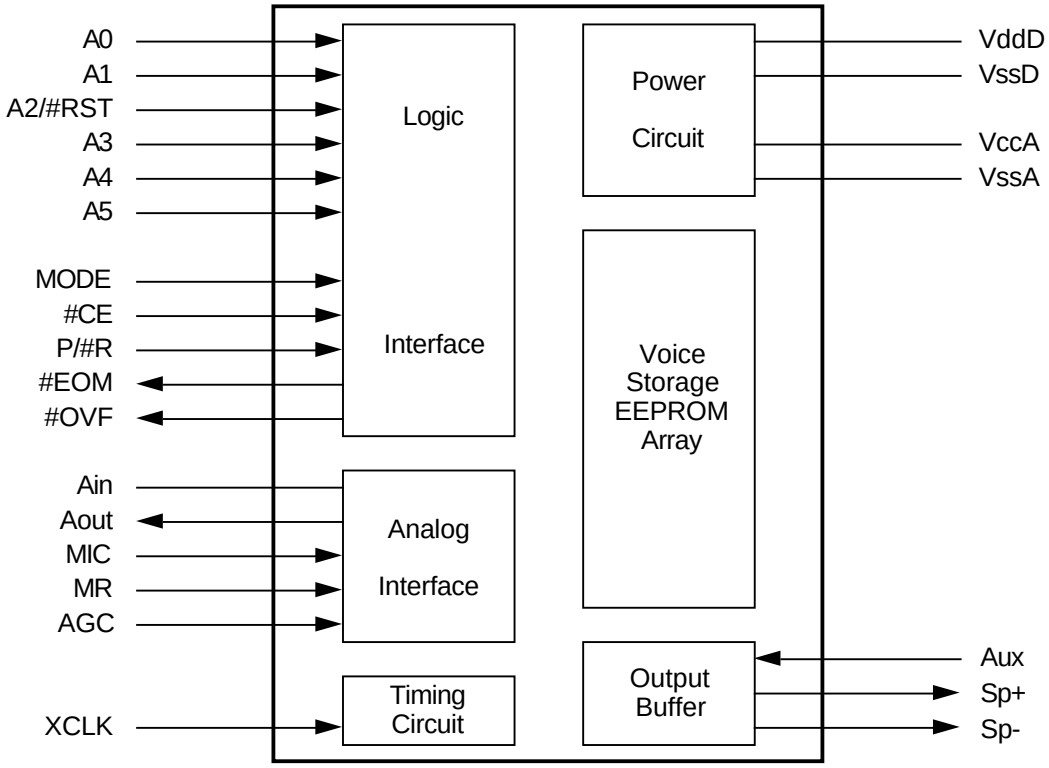
Descriptions

The MSR1161 is a single chip CMOS VLSI that can memorize analog voice data up to16 seconds at 8000 Hz sample rate. It provides high quality, single-chip record and playback solutions for messaging applications.

It has two operation modes : the push botton mode that is simple-to-use for manual operation while the CPU addressing mode allows complex messaging and addressing to be connected with microprocessor.

Voice signals are stored directly in their natural analog form into EEPROM memory. This allows natural voice reproduction in a single chip solid-state solution. Multiple chips can be cascaded to provide longer duration recorded and playback.

Block diagram



Signal Summary

Pin #	Pad #	Signal	Count	I / O	Active	Functions
		A0	1	I	H	High true address bit 0 (LSB)
		A1	1	I	H	High true address bit 1
		A2 / #RST	1	I	H/L	High true address bit 2 / restart
		A3	1	I	H	High true address bit 3
		A4	1	I	H	High true address bit 4
		A5	1	I	H	High true address bit 5
		#OVF	1	O	L	overflow flag output for whole 128K pixels
		#EOM	1	O	L	end of message flag output for each 2K pixels
		AUX	1	I		auxiliary input
		VssD	1			digital ground
		VssA	1			analog ground
		SP+	1	O		speaker output plus
		SP-	1	O		speaker output minus
		VccA	1			Vcc analog
		MIC	1	I		microphone input
		MR	1	I		microphone input reference
		Ain	1	I		analog input
		Aout	1	O		analog output
		AGC	1	I		automatic gain control input
		XCLK	1	I		external clock input
		MODE	1	I	H/L	mode selection input
		#CE	1	I	L	chip enable input
		P / #R	1	I	H/L	play / record
		VddD	1			digital Vdd

Signal Details

Input Signals

A0, A1, A2,A3, A4, A5
There are up to 64 sections provided, 2 K samples each. They are 6 bit high-true addresses to specify the section to be recorded or played among 64. A5 is MSB while A0 is the LSB.

#RST
Restart from section zero.
This pin as low when latched by #CE means the section pointer will be zero when played.

MODE
Mode selection. When this pin is connected to high(=1), the push button mode is selected. When this pin is connected to low (=0), the CPU addressing is selected.

#CE
Chip enable pin. This pulse' falling edge latches what you order this chip to execute - the address of specified section by 6 address bits, the operation by P/#R, Mode, etc. The rising edge also stops the playing (or recording) immediately. The Auxiliary input source are connected directly into mux of output buffer whenever #CE is high.

P/#R
Play or Record. Low to play and high to record.

MIC and MR
MIC means Microphone signal input. It should range within + / - 20 mV.
MR means Microphone reference. AC coupled to microphone ground to reduce noise.
This pin must be float if it is not used. It should range within 1.5 V or floating.
This signal pair is connected to microphone. There is a typical 6 K ohm resistance (R mic) in pin MIC. This R mic in serial with external C mic determines the cut off frequency of input signal. Only capacitive microphone is recommended.

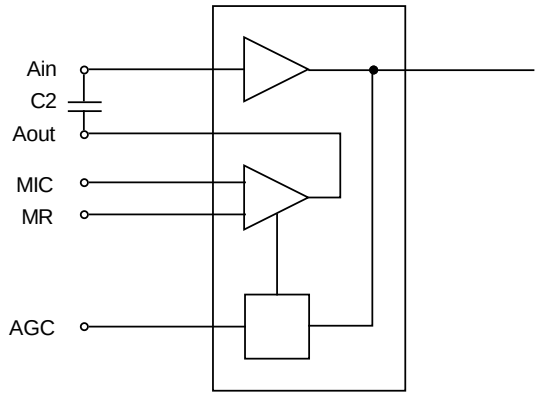
AGC
Automatic gain control. Connected to external capacitor and resistor to determine the "attack" and "release" times of the gain control. If it is tied to low, the maximal gain of pre-amplifier is achieved (19 dB). If it is tied to high, the minimal gain is achieved.
(around -3 dB). It should range within 0 through 5 V.

XCLK
External clock. This MSR1161 chip can be external clocked through this pin when more precise timing is required. 2 MHz clock in duty cycle 50% +/- 10% will play a sound at 8000 HZ sample rate. Below is the clock vs SR illustration. If this pin is tied to low, the internal clock is used. The internal clock plays 8 KHz sample rate.

6000 Hz S.R. by 1.50 MHz clock
8000 Hz S.R. by 2.00 MHz clock
10000 Hz S.R. by 2.50 MHz clock
12000 Hz S.R. by 3.00 MHz clock

AUX
Auxiliary signal input. The Auxiliary input source are connected directly into mux of output buffer whenever #CE is high and #EOM is low. This is helpful in concatenation applications. It is also the input from SP+ of next cascaded chip when at cascading application. Don't let it floating whenever it is not used. AUX can be connected to ground (VssA) when it's not used or idle.

Ain
Analog signal input pin. It also used to facilitate cascading. It should range within AC 0.5V to 2.5V at DC 1.5V. The input current should be greater than 1 mA. The greater, the better.
C2 is used to block dc voltage from Aout to Ain. The value is around 1 uF.



	C1	Attack Time
1	0.01 uF	uS
2	0.1 uF	uS
3	1.0 uF	uS
4	10 uF	uS

Output Signals

Aout
Analog signal output pre-amplified. It also used to facilitate cascading application. It should range within +/- 1000 mV.

#EOM
End of Message status output. It goes low at the end of each message section (2,048 pixels) and lasts for t EOM. It goes low as well when the device full.

#OVF
Device overflow status output. It indicates device overflow for (1) Playback or (2) Record Only or (3) Erase cycles. It goes low when the message overflows (device full) to facilitate cascading of multiple devices. Record ready for Erase Before Record cycle (only in Push button mode).
At the beginning of the Erase Before Record cycle, the chip may need to erase any existing information on the portion of the chip to be recorded. It may take up to 1 seconds. This status output pin indicates when the erase operation is complete and the chip is ready to begin recording.
This output LOW pulse also tells you that the rewind reaches the front line of voice storage.
In P3 or P6 mode, #VOF will be kept low after finishing playback until chip enter the next operation by #CE trigger.

SP+, SP-
Speaker output pins to drive 16 ohm (or 8 ohm) speaker directly, The feedback to AUX, the SP+ should be used. It should range within 0 through 3 V. Whenever the P/#R is low, this signal pair is hold at ground, VssA.

Power Signals

VssD, VddD
Ground and positive power supply of digital signals.

VssA, VccA
Ground and positive power supply of analog signals.
For mixed mode chip, the power signal is layout separately inside the chip. This is to reduce the interference. Put them as close as possible when coming out from chip to make both signal stable.

Circuit Description

Input preamplifier
This circuit block accepts the input analog signal coupled in from an external microphone (MIC). The microphone reference input pin (MR) is connected to microphone ground (or floating, if there is no microphone ground output) to reject common mode noise at the preamplifier. This circuit block includes a voltage level shifter to shift the microphone input signal (about +/- 10 mv peak-to-peak) to a positive reference level of about 1.5V, and a variable gain preamplifier to amplify this signal by -3dB to 19dB, depending on the input signal amplitude. Its output goes to the Aout pin.

Automatic gain control
This circuit block dynamically controls the variable gain of the preamplifier to compensate for the wide range of microphone input signal level. It allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time of this circuit is determined by the time constant of a 5KΩ internal resistance and an external capacitor C1 connected from the AGC input pin to VssA. The "release" time is determined by the time constant of an external resistor R1 and the same external capacitor connected in parallel between the AGC input pin and VssA.
1. If AGC is tied to low, the gain of pre-amplifier is maximum. (19dB)
2. If AGC is tied to high, the gain of pre-amplifier is minimum. (~ -3dB)

Input amplifier
This is a fixed gain amplifier stage to further amplify the input signal by about 20 ~ 21dB. For microphone inputs, the signal is AC coupled in from the Aout pin of the preamplifier stage to the Ain pin via an external capacitor C2. If the input comes from other sources, the signal may be fed, capacitively coupled, into the Ain pin directly. The output from this fixed gain amplifier goes to the antialiasing filter. For the cascaded situation, the Aout is AC coupled to the Ain of the next cascaded chip.

Anti-aliasing filter
This circuit block consists of three stages of Chebychev-type low-pass filter with a cut-off frequency of 3.4 KHz (when the sampling rate is 8 KHz) using switch-capacitor-filter technique. The filter has 3 poles, a roll-off ratio of 60dB per decade. Another one-stage Sallen-key low-pass filter is used in final stage to filter the high-frequency noise generated by switch-capacitor. The overall gain of filter is a unity. Since the resistor value in switch-capacitor can be adjusted by the switching clock frequency, the cut-off frequency tracks closely with the sampling rate governed by the internal clock oscillation frequency of external clock.

Sample and hold
This circuit samples and stores the input analog signal after passing through the filter in real time, to be transferred to the program circuit. The sampling rate is determined by an internal clock oscillator, controlled by a timing control circuit block. The nominal sampling rate is 8 KHz +/- 2.25%. If greater precision is required, The device can be clocked through the XCLK pin.

EEPROM programming circuit
The program circuit includes a charge pump to generate a high voltage; a multiplexor to select the columns of cells to be programmed; a timing-and voltage-control circuit and a comparator to precisely generate the pulses to erase and program the cells to the desired levels representing different input signal levels.

Memory array and decoder
The memory array consists of 128K EEPROM cells, tentatively organized in 1024 rows by 64 columns with two blocks (Odd and Even). Total memory size: 2x1024x64=131,072 pixels. The different rows are

decoded through a decoder driven by 6 address pins. The maximum messages is 64, and the message minimum size is 2048 pixels (0.256 second with 8 KHz sample rate frequency).

Smoothing filter
This actually uses the same circuit block as the antialiasing filter. During playback, the information read out from the memory array is smoothed out by the filter before going to the output amplifier.

Output Amplifier
The analog signal read out from the memory array, after passing through the smoothing filter, is buffered to drive the output loudspeaker. The on-chip differential speaker driver is capable of driving half watt into 16 ohm speaker. Two complementary output pins, SP+ and SP-, allow the speaker to transduce four times more output power for the same signal level than a single speaker output design. The output drivers are disabled during Standby and Record cycles.

Terms

Cascading
For the system requires more than one MSR1161 chips, several extra pins are used. The AUX is used to connected to the SP+ of the previous stage chip. Therefore, multiple of MSR1161 chips can be cascaded and only one speaker of the last chip is required. The pin #CE (Chip Enable) is used to select one of the MSR1161 chips. The selected MSR1161 chip will take the message from D/A converter and redirect it to the speaker output. For those unselected MSR1161 chips the speaker output will take the input from AUX. When the end of memory event happened in a selected chip, the #OVF pin will indicate this situation, and therefore, the system can select a new chip. The application circuit V shows double MSR1161s in cascade.

Sample Rate
MSR1161 has internal sample clock 8 KHz in precision +/- 2.5% for appropriate temperature and suitable working voltage. The other way to provide sample clock is to feed clock to XCLK pin. The sample rate is always equal to external clock frequency devided by 256. The 2 MHz clock to be applied to XCLK is recommended. Using higher sample rate may not achieve higher sound quality. Playback and record should have the same sample rate. There is no problem to apply higher sample clock for playback. However, the recording may have some error by using higher than 8 KHz.

Attack Time
Attack time is the time constant that the internal AGC circuit charges the external C1 through an internal 5k Ohm resistor. When the microphone input signal is getting large the AGC circuit starts charging the external C1. The charge time is proportional to the Attack Time. That means the smaller the Attack Time is the faster the C1 is charged. In consequent, the higher voltage of C1 charged the smaller AGC gain to amplify the microphone input signal. Therefore, for a loud signal input the AGC will reduce the signal amplitude eventually, and the Attack Time determines how fast the signal is been reduced.

Release Time
Release time is the time constant that the AGC circuit discharges the external C1 through an external resistor R1. When the microphone input sigal is getting small the AGC circuit starts discharging the external C1. The discharge time is proportional to the Release Time. That means the smaller the Release Time is the faster the C1 is discharged. In consequent, the lower voltage of C1 descharged the larger AGC gain to amplify the microphone input signal. Therefore, for a small signal input the AGC will enhance the signal amplitude eventually, and the Release Time determines how fast the signal is been enhanced.

DC Characteristics

(0℃~70 , VccA = 5.0 V ± 10%, Vdd D= 5.0 V ± 10%, VssD = 0.0 V, VssA = 0.0 V

Symbol	Parameter	Valid	Min.	Typ.	Max.	Unit	Conditions
I sb	Stand by	VddD		1	10	uA	
I op	operating	VddD			25	mA	w /o speaker
I IL	Input leakage I	logic I/Os			1	uA	
I PO	Pre-Amp source output I	Aout		100		uA	V Aout = 1.5 V
I PI	Pre-Amp sink input I	Aout		100		uA	V Ain = 1.5 V
I OVF	sink I of #VOF	#VOF				mA	R SP = 16 ohm
I EOM	sink I of #EOM	#EOM				uA	R SP = infinite
Ia PL	Playback I	VccA				mA	R SP = infinite
Ia PL	Playback I	VccA		3		mA	
Id PL	Playback I	VddD		20		uA	
Id REC	Recording I	VddD		30		mA	
Id ERA	Erasing I	VddD		30		mA	I oL = 4 mA
V iL	input low V	logic I/Os			0.8	V	
V ih	input high V	logic I/Os		2.0		V	I oh = -1.6 mA
V oL	output low V	logic I/Os			0.4	V	
V oh	output high V	logic I/Os		2.4		V	
Vpp SP	Speaker output Vpp	SP+, SP-		2.5		V	
Vpp MIC	Microphone input Vpp	MIC			20	mV	V (AGC) = 0 V
Vpp Ain	Analog input Vpp	Ain			100	mV	V (AGC) >= 3 V
Vpp AUX	Auxilary input Vpp	AUX			2.5	mV	Ain / Speaker
A PMX	Pre-Amp maximal gain			19		dB	AUX / Speaker
A PMN	Pre-Amp minimal gain			-3		dB	
A AF	Analog input fix gain			20		dB	
A PW	power Amp gain			1		dB	
R SP	Speaker load R	SP+, SP-		16		ohm	
R AGC	AGC pin input R	AGC		10		Kohm	
R MIC	Microphone input R	MIC		6		Kohm	16 ohm speaker
R Ain	Analog input Resistance	Ain		5		Kohm	
C MIC	Input C of pin MIC	MIC		0.22		uF	
C MR	Input C of pin MR	MR		0.22		uF	
P SP	Speaker output power	SP+, SP-			75	mW	

All above parameters are valid on both operation modes.

AC Characteristics

(0℃ ~70 , VccA= 5.0 V ± 10%, VddD = 5.0 V ± 10%, VssD = 0.0 V, VssA = 0.0 V)

Symbol	Description	Function	Valid pin	Min.	Typ.	Max.	Unit	Remarks
t CE	#CE hold time	Rec, Play	#CE	10			ns	
t SET	Address set up time	Rec, Play					us	
t HOLD	Address hold time	Rec, Play		6			us	
t MIC	#CE fall to MIC start	Rec			256		us	
t SPK	#CE fall to SP+ start	Play			256		us	
t CEM	#CE fall to MIC stop	Rec				8	ms	
t CES	#CE fall to SP+ stop	Play			0~256		ms	
t OSP	#OVF start to SP+ stop	Rec,			256		us	
t ESP	#EOM start to SP+ stop	Rec,					us	
t OVF	#OVF hold time	Rec, Play	#OVF		126		us	
t EOM	#EOM hold time	Rec, Play	#EOM		126		us	
t RMU	Ramp up width	Play	SP+, SP-				ms	
t RMD	Ramp down width	Play	SP+, SP-				ms	
t PUD	Power up delay	Rec, Play	VddD, VccA	1			ms	
t P	Power rise up time	Rec, Play	VddD, VccA			1	ms	
t R	Power ripple width	Rec, Play	VddD, VccA			1	ms	
t REC	Total record time	Rec			16		s	
t PLAY	Total play time	Play			16		s	
f SAMP	Sample clock frequency		(internal)		8		KHz	
f CUT	Cut-off frequency				3.4		KHz	
f XCLK	External clock frequency		XCLK		2		MHz	at node XCLK
df / f	frequency stability		SP+, SP-	-10		+10	%	[F(5V)-F(4.5V)]/F(5V)
df / f	frequency variation		SP+, SP-	-10		+10	%	lot by lot
THD	total harmonic distorsion		SP+, SP-		2		%	at 1 KHz

All above parameters are valid on both operation modes except 4 : t MIC, t SPK, t CEM, t CES.

Chip Functions

I. Chip works at mode 1, playback

Functions		Signals to decode								Location to start	When to stop
		MODE	P / #R	A0	A1	A2	A3	A4	A5		
				—	—	#RST	#END		—		
P2	play back from here	1	1	x	x	1	0	x	1	current section	#EOM
P3	play back from here	1	1	x	x	1	1	0	1	current section	#OVF
P5	play back from zero	1	1	x	x	0	0	x	1	section 0	#EOM
P6	play back from zero	1	1	x	x	0	1	x	1	section 0	#OVF

II. Chip works at mode 1, Forward and Rewind

Functions		Signals to decode								Location to start	When to stop
		MODE	P / #R	A0	A1	A2	A3	A4	A5		
				—	—	#RST	#END	RWD	—		
F1	Forward from here	1	1	x	x	1	0	0	0	current section	# EOM
F2	Forward from here	1	1	x	x	1	1	0	0	current section	# OVF
F3	Forward from zero	1	1	x	x	0	0	0	0	section 0	# EOM
F4	Forward from zero	1	1	x	x	0	1	0	0	section 0	# OVF
B1	Rewind from here	1	1	x	x	1	0	1	0	current section	# EOM
B2	Rewind from here	1	1	x	x	1	1	1	0	current section	# OVF
B3	Rewind from zero	1	1	x	x	0	0	1	0	section 0	# EOM
B4	Rewind from zero	1	1	x	x	0	1	1	0	section 0	# OVF

III. Chip works at mode 1, record/erase

Functions		Signals to decode								Location to start	When to stop
		MODE	P / #R	A0	A1	A2	A3	A4	A5		
				—	—	#RST	—	—	—		
R2	Erase from here	1	0	x	x	1	x	0	0	current section	# OVF
R3	Erase from zero	1	0	x	x	0	x	0	0	section 0	# OVF
R4	Erase from here	1	0	x	x	1	x	x	1	current section	# OVF
R5	Erase from zero	1	0	x	x	0	x	x	1	section 0	# OVF
R6	Erase Before Record from here	1	0	x	x	1	x	1	0	current section	# OVF
R6	Erase Before Record from zero	1	0	x	x	0	x	1	0	section 0	# OVF

IV. Chip works at mode 0, playback and record / erase

	Functions	Signals to decode								Location to start	When to stop
		MODE	P / #R	A0	A1	A2	A3	A4	A5		
P1	play back	0	1	A0	A1	A2	A3	A4	A5	—	next #CE
R1	record / erase	0	0	A0	A1	A2	A3	A4	A5	—	next #CE

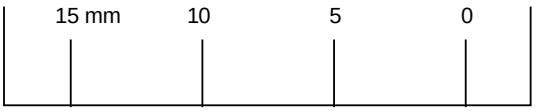
COB Board Description

A PCB marked as MS-2266 is used for MSR1161's COB board. The MS-2266 has 28 pads and only 24 of them are used for MSR1161's signal. The pads assignment is shown on below Figure.

COB Information

Silk screen & copper print

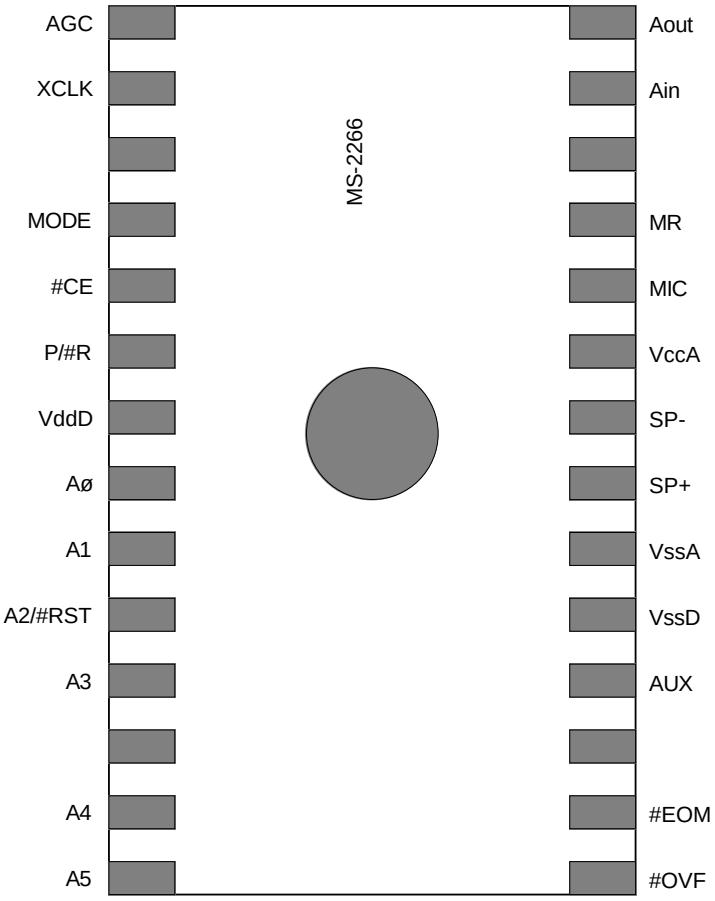
COB model number : MVI-P28



Legend

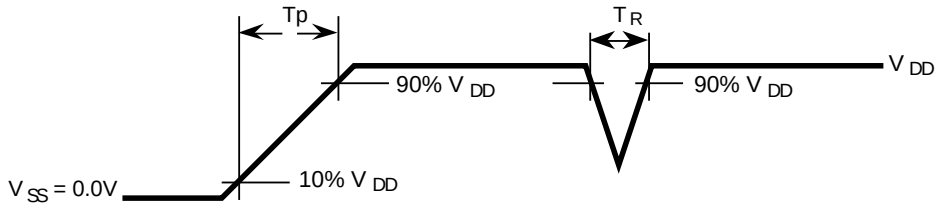
Copper pad

Chip covered

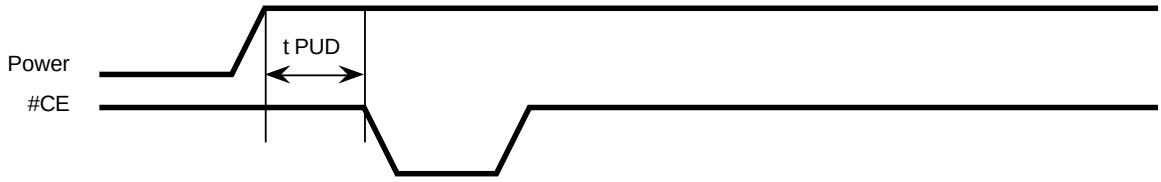


Timing Critical

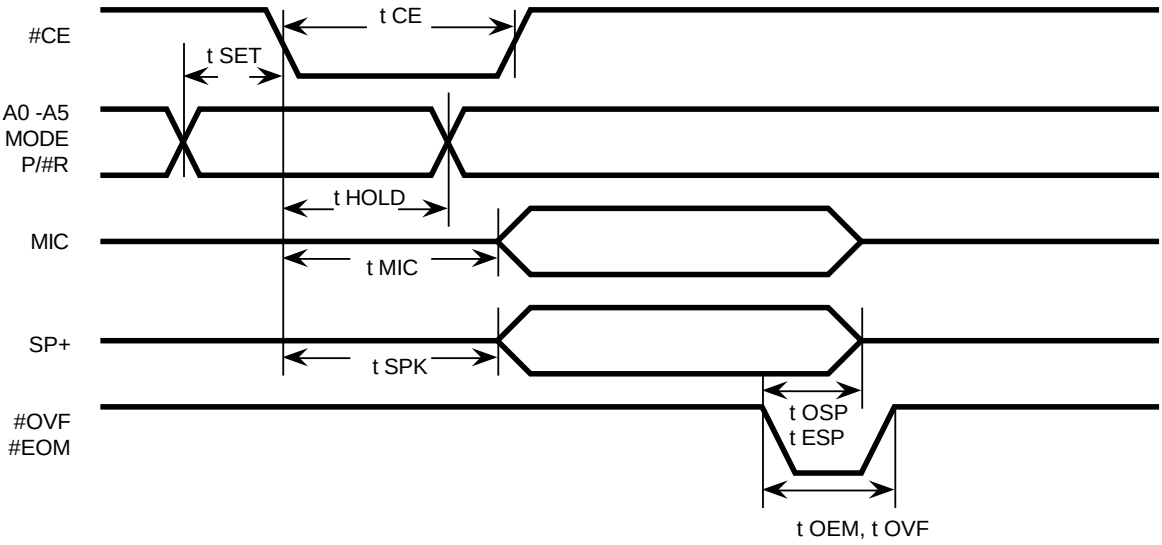
I. Acceptable Power on Signal & Ripple



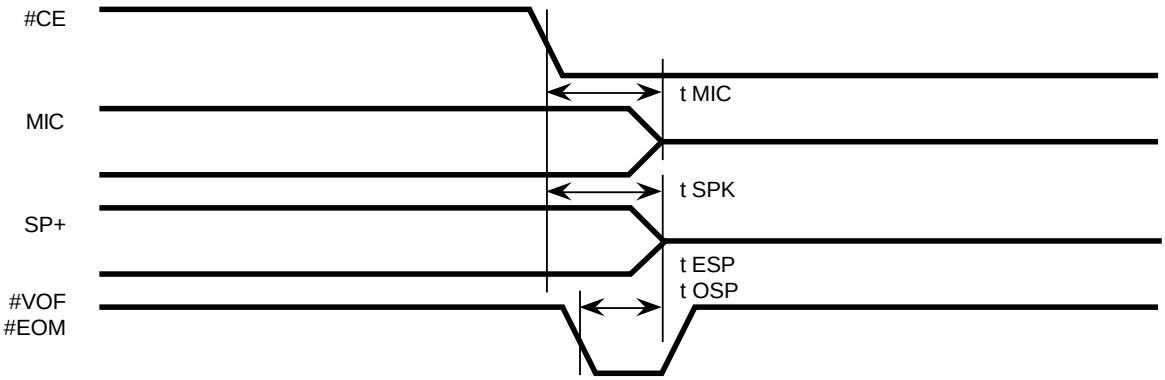
II. Power up delay



III. Start a sound record / playback



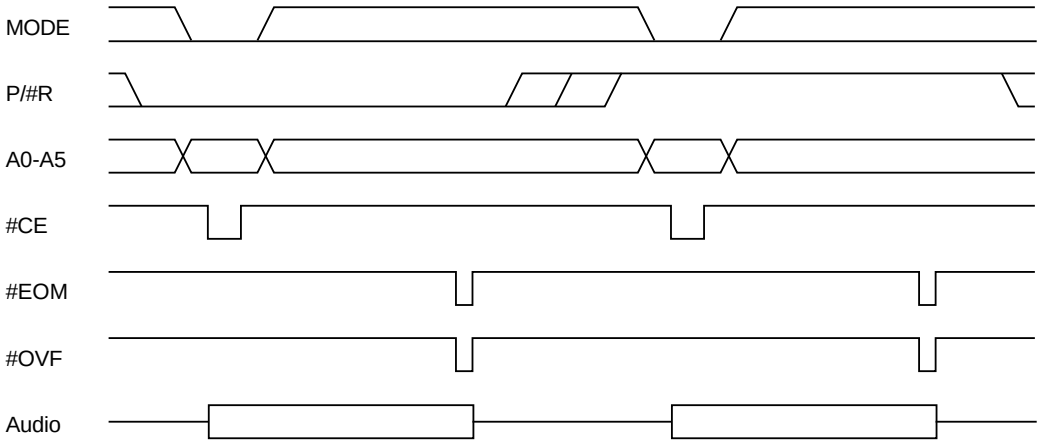
IV. To end a sound record / playback



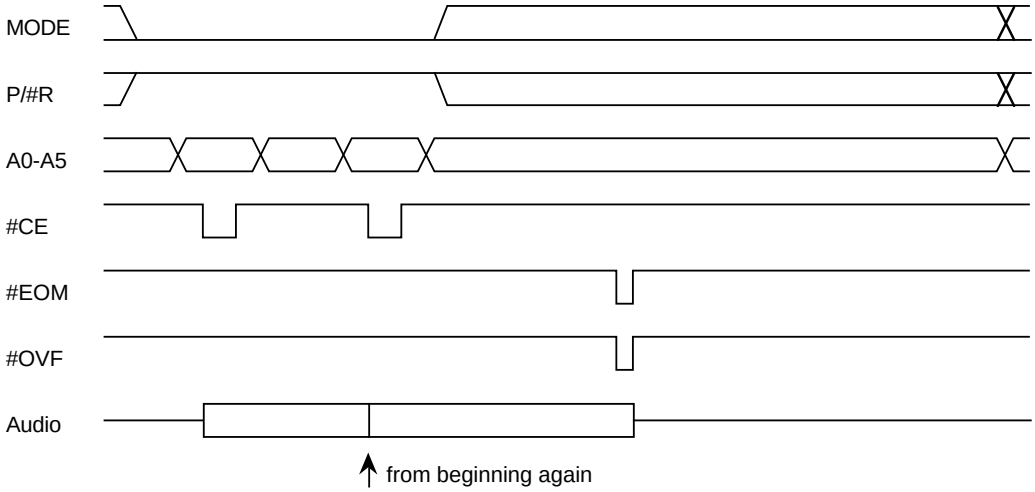
Timing Diagram

I. Mode ø Operations (CPU Addressing Mode)

I.1 Record & Playback at C.A. Mode



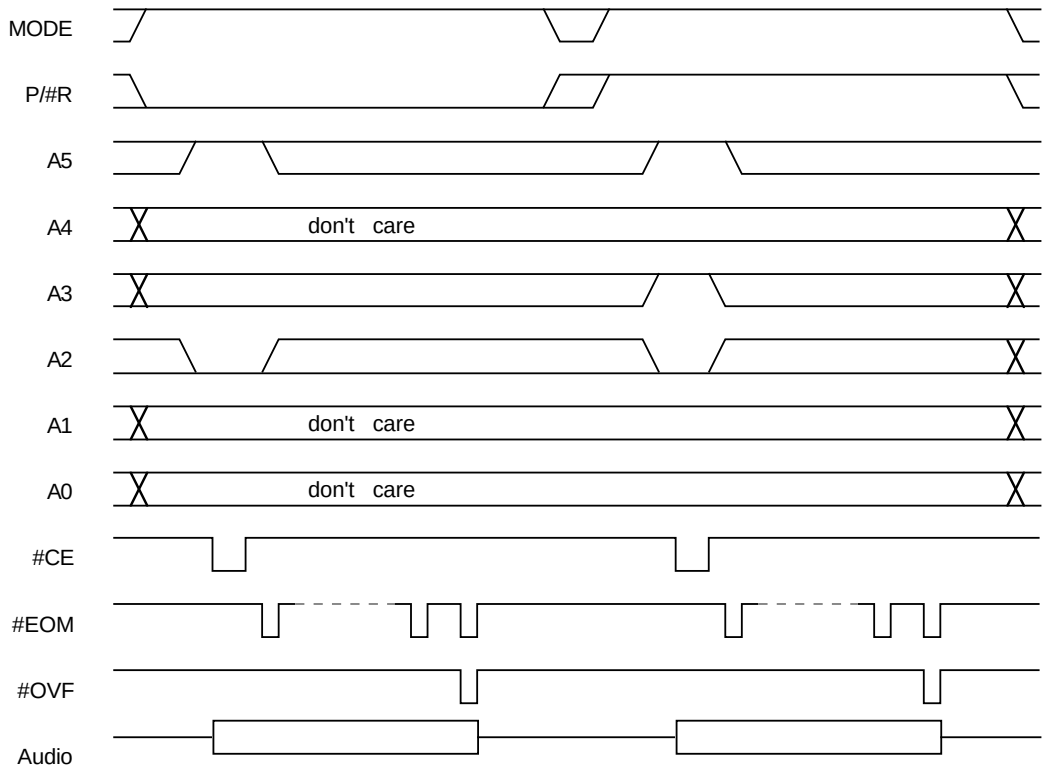
I.2 #CE to terminate a playing sound at C.A. Mode



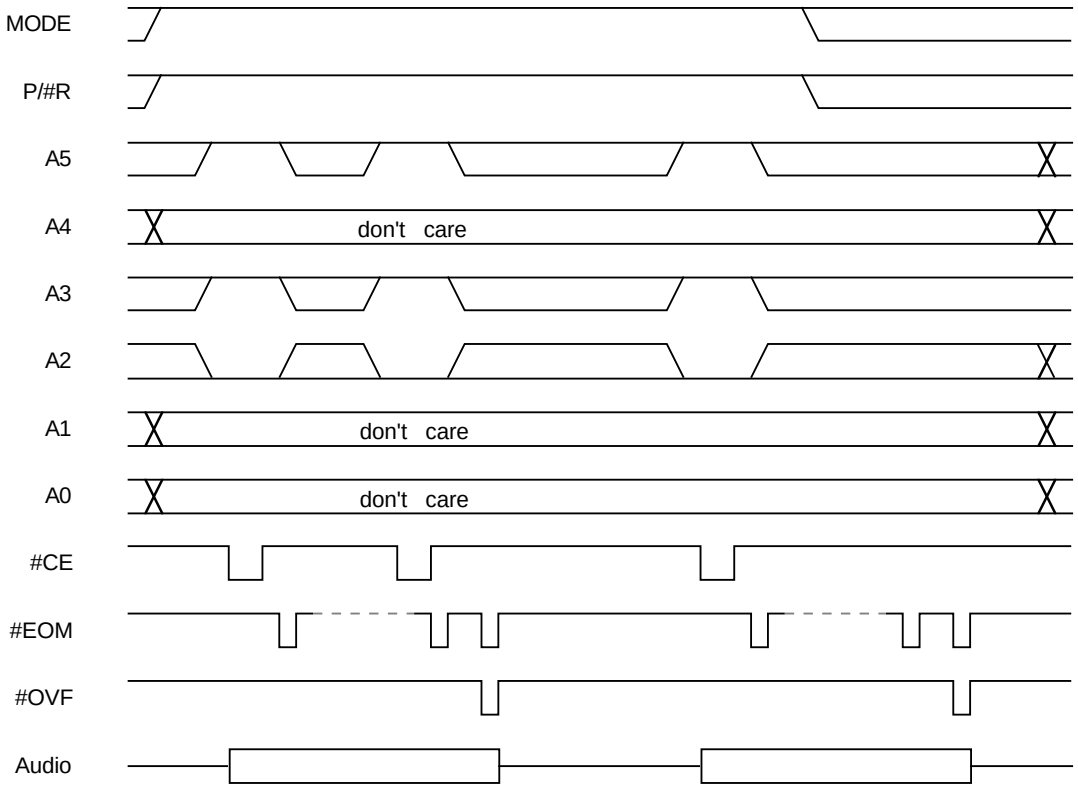
Timing Diagram

II. Mode 1 Operation (Push button mode)

II.1 Record & Playback at P.B. mode (from section 0 to #OVF)

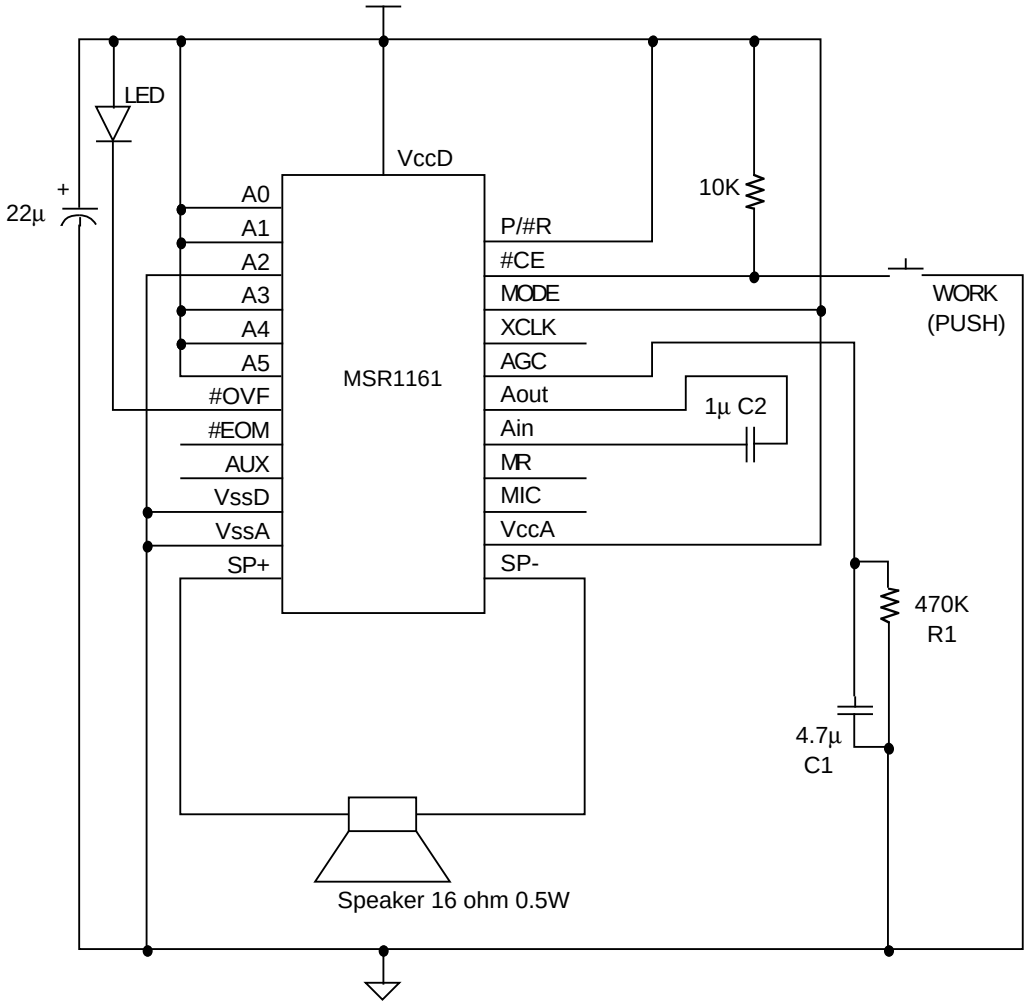


II.2 #CE cannot terminate a playing sound at P.B. mode



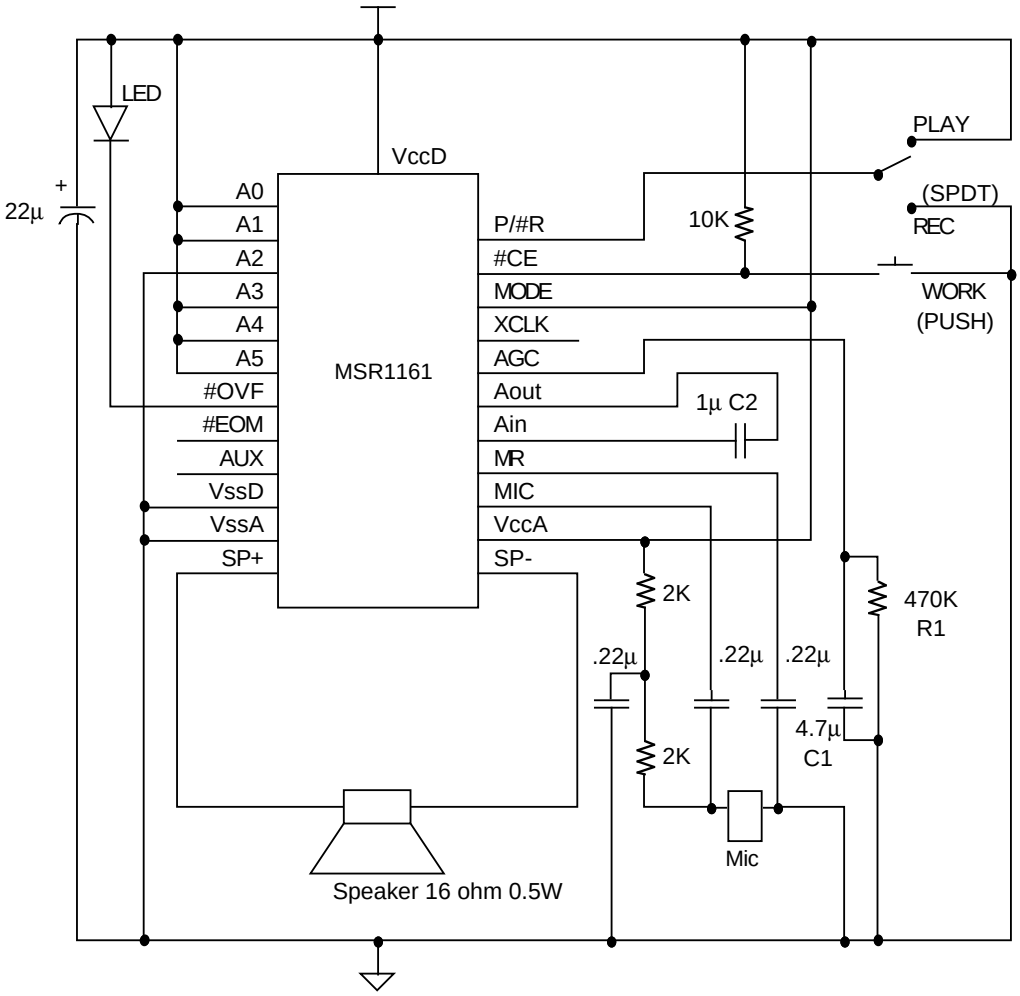
Application circuits

I. Playback only at P.B. mode



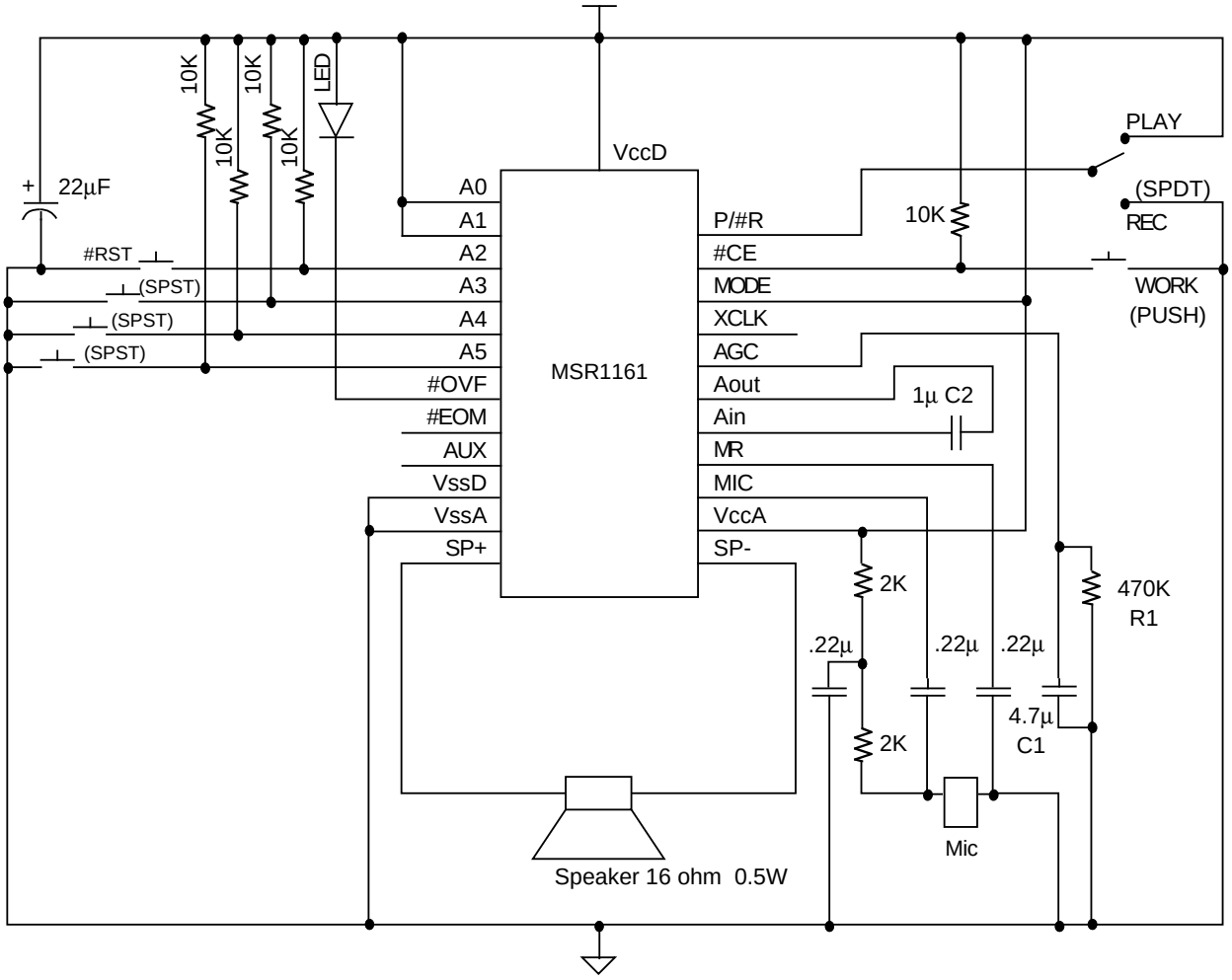
Application circuits

II. Record & Playback at P.B. mode

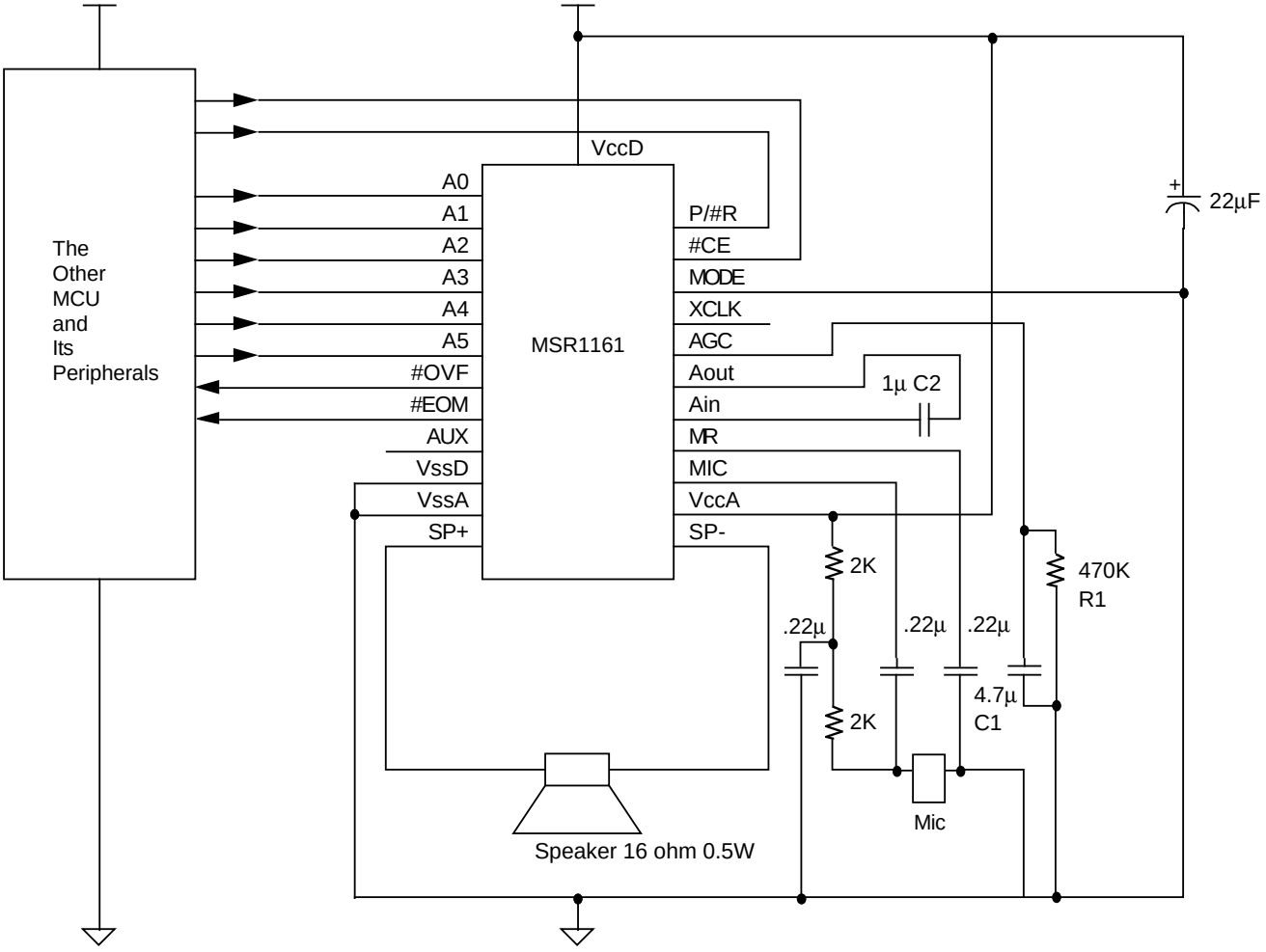


Application circuits

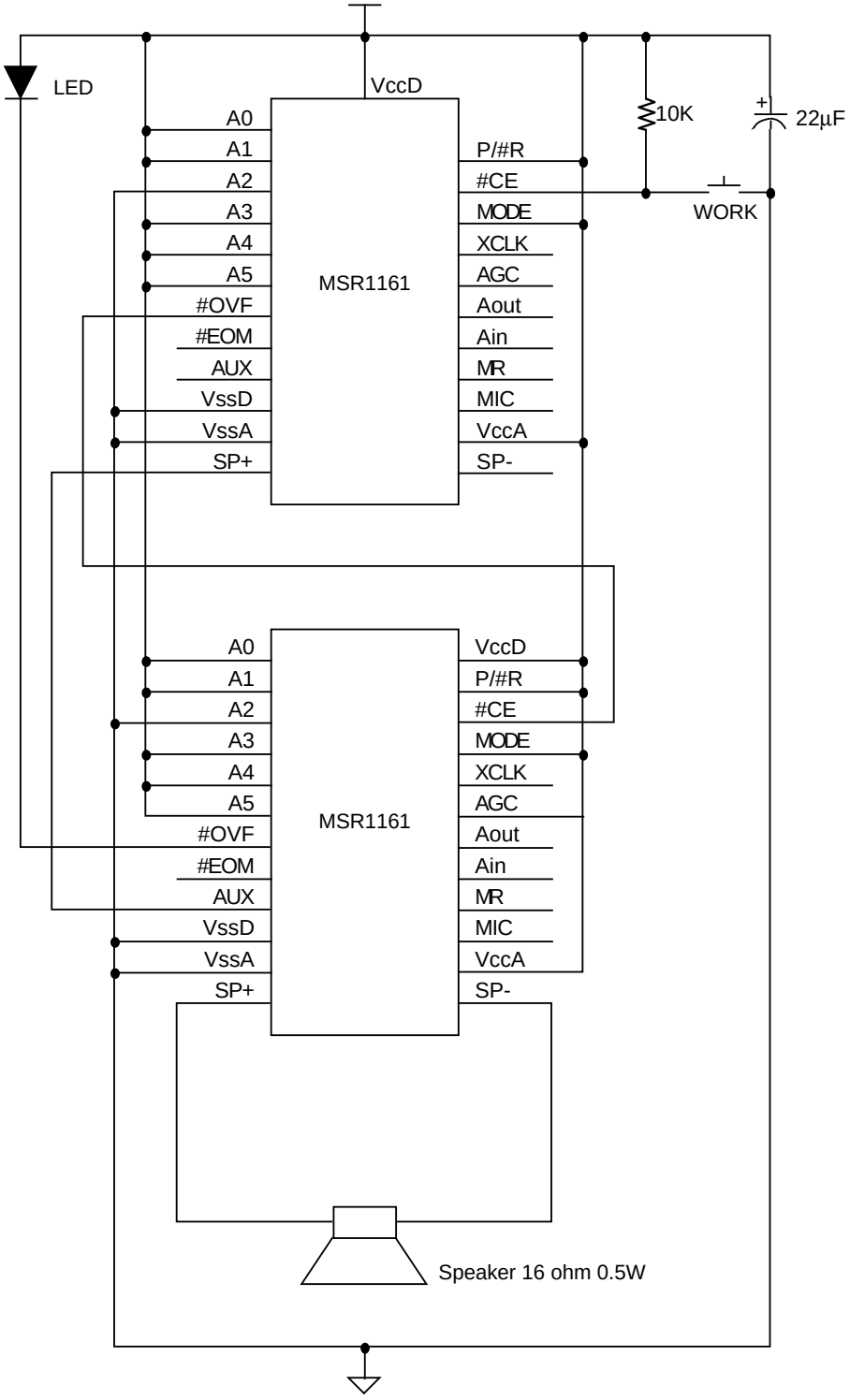
III. Typical Push Button mode



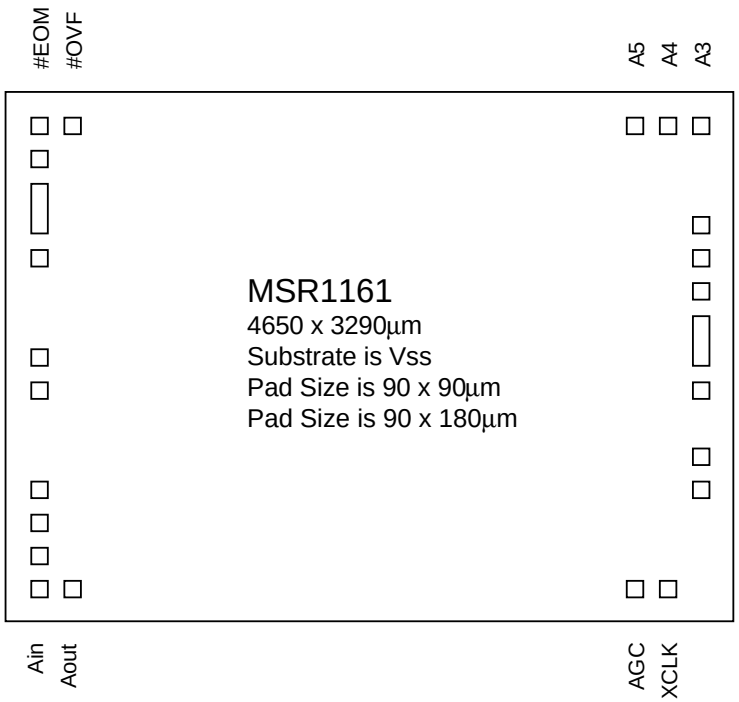
IV. Typical CPU addressing mode



V. Cascading of Playback at P.B. mode



	X	Y
#OVF	-1857	1424
#EOM	-2105	1366
AUX	-2105	1143
VssD	-2104	898
VssA	-2104	693
SP+	-2100	106
SP-	-2100	-116
VccA	-2105	-734
MIC	-2105	-942
MR	-2105	-1163
Ain	-2105	-1386
Aout	-1844	-1424
AGC	1621	-1424
XCLK	1831	-1424
MODE	2103	-953
#CE	2103	-740
P/#R	2103	-302
VddD	2103	-44
A0	2103	212
A1	2103	435
A2/#RST	2103	656
A3	2103	1383
A4	1850	1424
A5	1629	1424



Taiwan

#1, Creation Road I,
Science - based Industrial Park,
Hsinchu, 30077
Taiwan, ROC
"taylor_hsiao@ccmail.mosel.com.tw"
TEL: 886-3-5770055
FAX: 886-3-5772788
FAX: 886-3-5784732

Taipei

7F, #102 Sec. 3,
Ming Chung E. Road,
Taipei
Taiwan, ROC

TEL: 886-2-5451213
FAX: 886-2-5451214

Hongkong

#19 Dai Fu Street,
Taipo Industrial Estate,
Taipo, N.T.
Hongkong
TEL: 852-2388-2777
TEL: 852-2665-4883
FAX: 852-2664-2406
FAX: 852-2770-8011

U.S.A.

#3910 North First Street,
San Jose,
CA. 65134-1501
U.S.A.

TEL: 1-408-433-6000
FAX: 1-408-433-0952