OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM6562B-xx

DOT MATRIX LCD CONTROLLER DRIVER

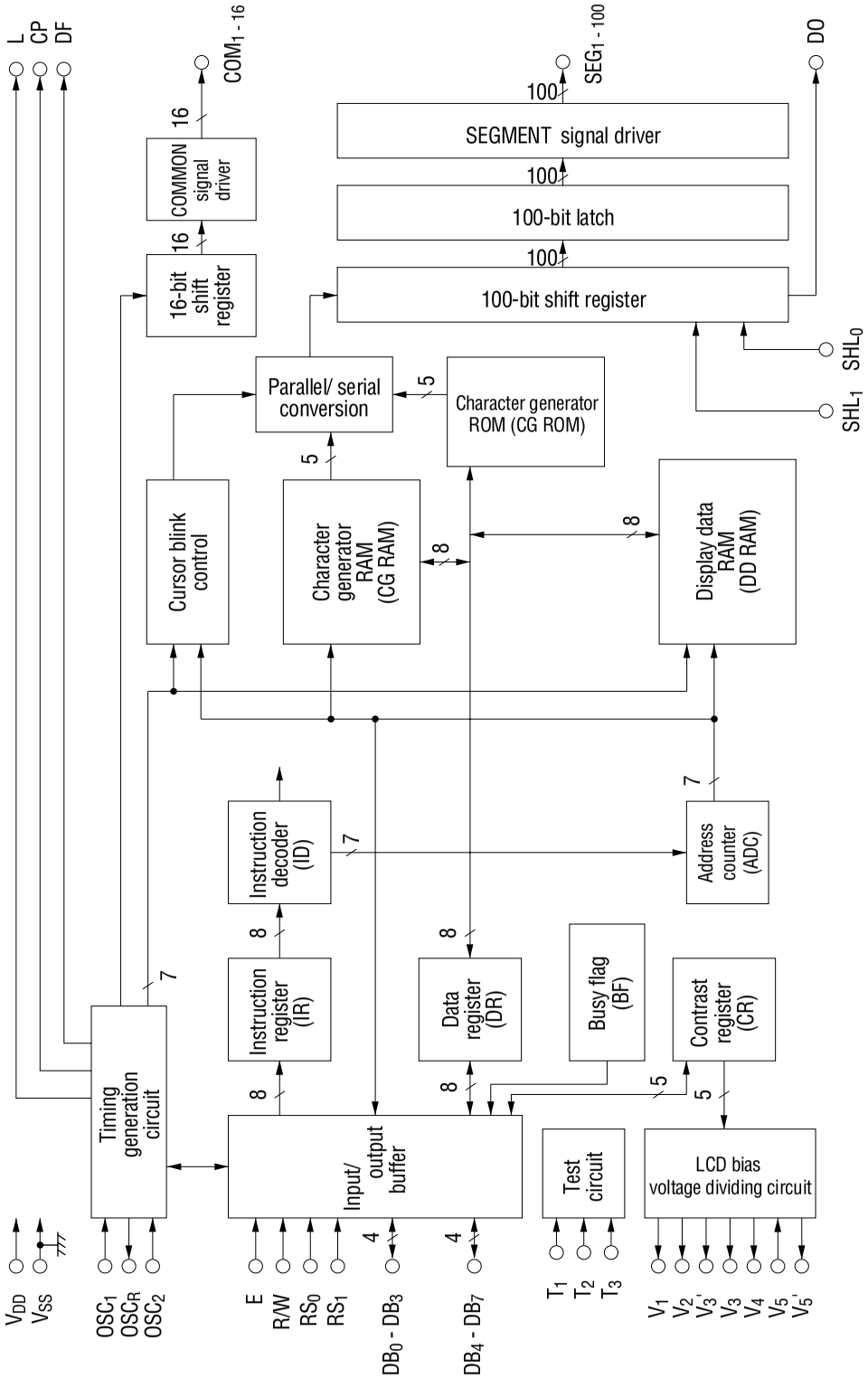
GENERAL DESCRIPTION

The MSM6562B-xx controls a character type dot matrix LCD in combination with an 8-bit or 4-bit microcontroller.
The MSM6562B-xx can control a display of up to 40 characters. With the display data serial transfer function, the MSM6562B-xx, when used in combination with the character extension IC (MSM5259), can control a maximum of 80 characters.

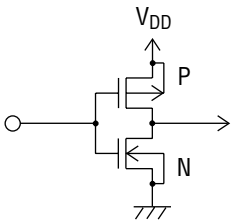
FEATURES

- Easy interface with an 8-bit or 4-bit microcontroller.
- Dot matrix LCD controller driver for 5 × 7 dots font or 5 × 10 dots font.
- Automatic power ON reset.
- 16 COMMON signal drivers and 100 SEGMENT signal drivers are built in.
- Can control up to 80 characters when used in combination with MSM5259.
- Built-in character generator ROM for 160 characters with 5×7 dots font and 32 characters with 5 × 10 dots font.
- Character patterns can be programmed by CG RAM. (5×8 dots font: 8 kinds, 5×11 dots font: 4 kinds)
- 1/8 duty (1 line; 5×7 dots + cursor), 1/11 duty (1 line; 5×10 dots + cursor), or 1/16 duty (2 lines; 5×7 dots + cursor) selectable.
- Built-in RC oscillation circuit by an external resistor or an internal resistor.
- Built-in bias dividing resistors for LCD driving.
- Built-in contrast adjusting circuit.
- Bidirectional transfer available on segment output.
- Aluminum pad chip (Product name: MSM6562B-xx)
  xx indicates code number.

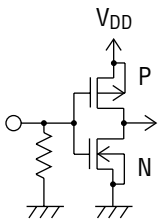
BLOCK DIAGRAM



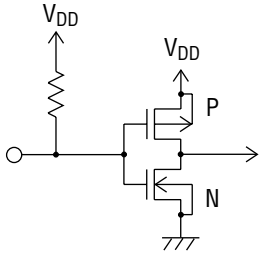
INPUT AND OUTPUT CONFIGURATION



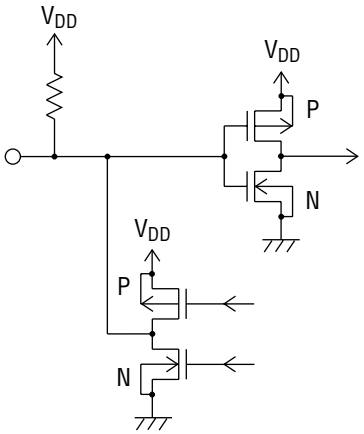
Applied to Pin E.



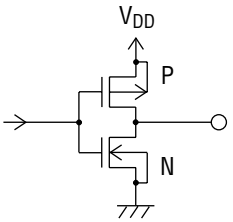
Applied to Pins T_1, T_2 and T_3.



Applied to Pins R/W, RS_0 and RS_1.



Applied to DB_0 - DB_7.



Applied to DO, CP, L and DF.

PIN DESCRIPTIONS

Symbol	Description
R/W	Read/write selection input pin. "H": Read, and "L": Write
RS_0, RS_1	Register selection input pins. RS_0 "H" RS_1 "H": Data register RS_0 "L" RS_1 "H": Instruction register RS_0 "L" RS_1 "L": Contrast register
E	Input pin for data input/output between CPU and MSM6562B-xx and for activating instruction.
DB_0 - DB_7	Input/output pins for data send/receive between CPU and MSM6562B-xx.
OSC_1, OSC_2, OSC_R	Clock oscillating pins required for internal operation upon receipt of CPU instruction and the LCD drive signal. When oscillated by an external resistor, connect a resistor between OSC_1 and OSC_2. When oscillated by a built-in resistor, connect OSC_R and OSC_2 externally.
COM_1 - COM_{16}	LCD COMMON signal output pins.
SEG_1 - SEG_{100}	LCD SEGMENT signal output pins.
SHL_0, SHL_1	Input pins to control the transfer direction of the SEGMENT signal output data. See table below.
DO	Data output pin to send serial data to the character extension IC.
CP	Clock output pin to transfer the serial data to the character extension IC.
L	Latch output pin to latch the transferred data to the character extension IC.
DF	Output pin for the alternating signal (DF, display frequency) required for an LCD display.
V_{DD}	Power supply pin.
V_{SS}	Ground pin.
V_1 - V_5, V_3'	Bias voltage input pins to drive an LCD and bias setting pin. (Built-in bias dividing resistor) 1/4 bias : Connect V_2 and V_3. Leave V_3' open. 1/5 bias : Connect V_3 and V_3'. Since V_{LCD} value depends on V_5 voltage, connect a variable resistor between V_5 pin and V_{SS} potential or connect V_5 pin and V_5' pin to adjust V_{LCD}.
V_5'	Contrast adjusting voltage output pin.

SHL_0	SHL_1	Segment data transfer direction
L	L	$SEG_1 \rightarrow SEG_{100}$
L	H	$SEG_{100} \rightarrow SEG_1$
H	L	$SEG_1 \rightarrow SEG_{50} \Rightarrow SEG_{100} \rightarrow SEG_{51}$
H	H	$SEG_{100} \rightarrow SEG_1$

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable Pin
Supply voltage	V_{DD}	Ta = 25°C	–0.3 to + 7.0	V	V_{DD}, V_{SS}
Supply voltage for LCD display	V_1, V_2, V_3, V_4, V_5	Ta = 25°C	–0.3 to V_{DD} + 0.3	V	V_1, V_2, V_3, V_4, V_5
Input voltage	V_I	Ta = 25°C	–0.3 to V_{DD} + 0.3	V	R / W, RS_1, RS_0, E, DB_0 - DB_7 OSC_1
Junction temperature	T_j	—	150	°C	—
Storage temperature	T_{STG}	—	–55 to + 150	°C	—

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable Pin
Supply voltage	V_{DD}	—	4.5 to 5.5	V	V_{DD}, V_{SS}
LCD driving voltage	V_{LCD}	$V_{DD} - V_{SS}$ 1/4 bias *1	3.0 to 5.5 *3	V	V_{DD}, V_5
		$V_{DD} - V_{SS}$ 1/5 bias *2	3.0 to 5.5 *3	V	
Operating temperature	T_{op}	—	–30 to +85	°C	—

*1 This voltage should be applied to $V_{DD} - V_5$.
Voltages applicable to V_1, V_2, V_3 and V_4 are as follows:
$V_1 = V_{DD} - 1/4 (V_{DD} - V_5)$
$V_2 = V_3 = V_{DD} - 1/2 (V_{DD} - V_5)$
$V_4 = V_{DD} - 3/4 (V_{DD} - V_5)$

*2 This voltage should be applied to $V_{DD} - V_5$.
Voltages applicable to V_1, V_2, V_3 and V_4 are as follows:
$V_1 = V_{DD} - 1/5 (V_{DD} - V_5)$
$V_2 = V_{DD} - 2/5 (V_{DD} - V_5)$
$V_3 = V_{DD} - 3/5 (V_{DD} - V_5)$
$V_4 = V_{DD} - 4/5 (V_{DD} - V_5)$

*3 The relation of $V_{DD} > V_1 > V_2 \geq V_3 (=V_3') > V_4 > V_5 \geq V_{SS}$ must be kept.
(High ← → Low)
LCD driving voltage can be adjusted by varying V_5.
However, V_5 cannot be used under V_{SS} voltage.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 to 5.5V, Ta = -30 to +85°C)

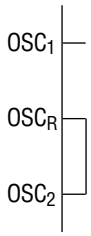
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
"H" input voltage	V_{IH1}	—	2.2	—	V_{DD}	V	R/W, RS_0, RS_1, E, DB_0 - DB_7
"L" input voltage	V_{IL1}	—	–0.3	—	0.6	V	
"H" input voltage	V_{IH2}	—	V_{DD} – 0.8	—	V_{DD}	V	OSC_1, SHL_0, SHL_1
"L" input voltage	V_{IL2}	—	–0.3	—	0.8	V	
"H" output voltage	V_{OH1}	I_O = –0.205mA	2.4	—	—	V	DB_0 - DB_7
"L" output voltage	V_{OL1}	I_O = 1.6mA	—	—	0.4	V	
"H" output voltage	V_{OH2}	I_O = –40µA	$0.9V_{DD}$	—	—	V	DO, CP, L, DF, OSC_2
"L" output voltage	V_{OL2}	I_O = 40µA	—	—	$0.1V_{DD}$	V	
COM voltage drop	V_C	I_O = ± 40µA (Note 1)	—	—	2.3	V	COM_1 - COM_{16}
SEG voltage drop	V_S	I_O = ± 40µA (Note 1)	—	—	3.0	V	SEG_1 - SEG_{100}
Input leakage current	I_{IL}	$V_I = V_{DD}$	—	—	1	µA	E, SHL_0, SHL_1
		$V_I = V_{SS}$	—	—	–1	µA	
"H" input current	I_{IH2}	$V_I = V_{DD}$ Except the current flowing to the pull-up resistor and output driving MOS.	—	—	2	µA	R/W, RS_0, RS_1, DB_0 - DB_7
"L" input current	I_{IL2}	V_{DD} = 5.0V $V_I = V_{SS}$	–34	–83	–204	µA	
Supply current	I_{DD}	V_{DD} = 5.0V E = "L" level, SHL_0, SHL_1 = "L" level Built-in R_f oscillation or external clock input to OSC_1. External clock frequency (f_{IN}) is 270kHz. R/W, RS_0, RS_1, and DB_0 to DB_7 are open. Output pins are all no load. Except bias current for LCD driving. (Note 2, 3, 4)	—	—	1	mA	V_{DD}
LCD driving bias resistance	LBR	—	2	4	8	kΩ	$V_{DD} – V_1$, $V_1 – V_2$ $V_2 – V_3'$, $V_3 – V_4$ $V_4 – V_5$
Variable range by built-in variable resistor for LCD driving voltage	$V_{LCD\ MAX}$	V_{DD} = 5.0V, 1/5 bias	4.6	—	—	V	$V_{DD} – V_5$ (V_5')
	$V_{LCD\ MIN}$	V_{DD} = 5.0V, 1/5 bias	—	—	3.7		
LCD driving bias voltage (external input)	V_{LCD1}	$V_{DD} – V_5$ (Note 5) 1/5 bias	3.0	—	5.5	V	V_{DD}, V_1, V_2, V_3, V_3', V_4, V_5
	V_{LCD2}	1/4 bias	3.0	—	5.5		

(Note 1) Applies to the voltage drop (V_C) from V_{DD}, V_1, V_4 and V_5 to each COMMON pin (COM_1 to COM_{16}) as well as to voltage drop (V_S) from V_{DD}, V_2, V_3 and V_5 to each SEG pin (SEG_1 to SEG_{100}) when 40µA is flowed through one COM or SEG pin. When output level is at V_{DD}, V_1, or V_2 level, 40µA is flowed out, while 40µA is flowed in when the output level is at V_3, V_4 or V_5 level.

This occurs when 5V is input to V_{DD}, V_1 and V_2 , and 0V is input to V_3, V_4 and V_5.

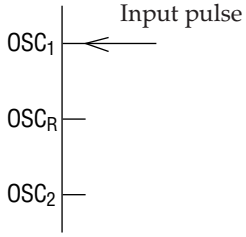
(Note 2) Applies to the current value flowed in the pin V_{DD}, in the case of V_{DD} = 5V, V_{SS} = 0V, V_1, V_2 = 5V, V_3, V_4, V_5 = 0V and V_5' is open.

(Note 3) Built-in R_f oscillation circuit



Minimum wiring is required between OSC_R and OSC_2.
Leave OSC_1 open.

(Note 4) External clock input circuit



Leave OSC_R and OSC_2 open.

(Note 5) Input the voltage to V_5. (However, V_5 cannot be used under V_{SS} voltage.)

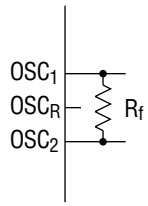
N (number of LCD lines) / Pin	1-line mode Bias : 1/4	2-line mode Bias : 1/5
V_1	$V_{DD} - \frac{V_{LCD}}{4}$	$V_{DD} - \frac{V_{LCD}}{5}$
V_2	$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{2V_{LCD}}{5}$
V_3	$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{3V_{LCD}}{5}$
V_4	$V_{DD} - \frac{3V_{LCD}}{4}$	$V_{DD} - \frac{4V_{LCD}}{5}$
V_5	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

At 1/4 bias : Connect V_2 and V_3 externally and leave V_3' open.
At 1/5 bias : Connect V_3 and V_3' externally.
V_{LCD} is the LCD driving voltage. (For N [number of LCD lines], refer to the explanation of the Function setting instruction of the instruction code.)

AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
R_f clock oscillation frequency	f_{OSC1}	R_f = 120 kΩ ± 2% (Note 1)	175	270	350	kHz	OSC_1 OSC_2
External clock frequency	f_{IN}	OSC_R and OSC_2 are open. Input a pulse to OSC_1. (Note 4)	125	—	480	kHz	OSC_1
External clock duty	f_{duty}	(Note 2)	45	50	55	%	OSC_1
External clock rise time	t_{rf}	(Note 3)	—	—	0.2	µs	OSC_1
External clock fall time	t_{ff}	(Note 3)	—	—	0.2	µs	OSC_1
Built-in R_f clock oscillation frequency	f_{OSC2}	OSC_1 is open. (Note 5) Connect OSC_R and OSC_2.	140	280	480	kHz	OSC_1 OSC_R OSC_2

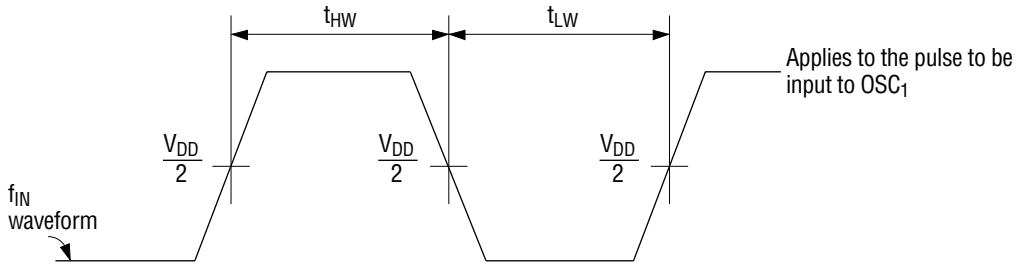
(Note 1)



$R_f = 120k\Omega \pm 2\%$

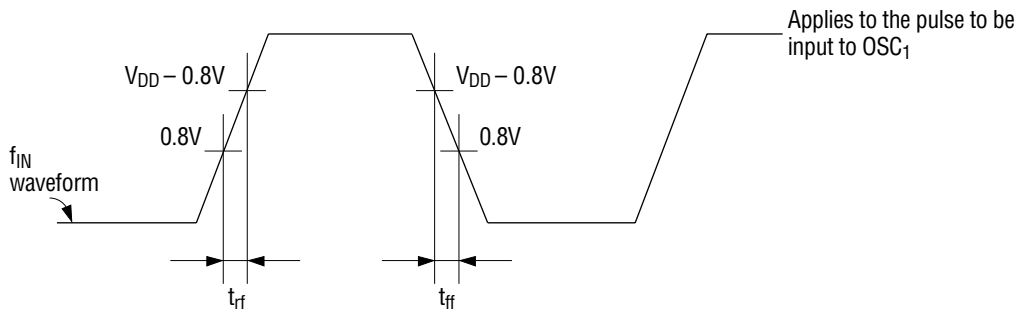
Minimum wiring is required between OSC_1 and R_f and between OSC_2 and R_f.
Leave OSC_R open.

(Note 2)



$f_{duty} = t_{HW} / (t_{HW} + t_{LW}) \times 100$ (%)

(Note 3) Applies to the pulse to be input to OSC_1.



(Note 4) See Note 4 to "DC Characteristics."

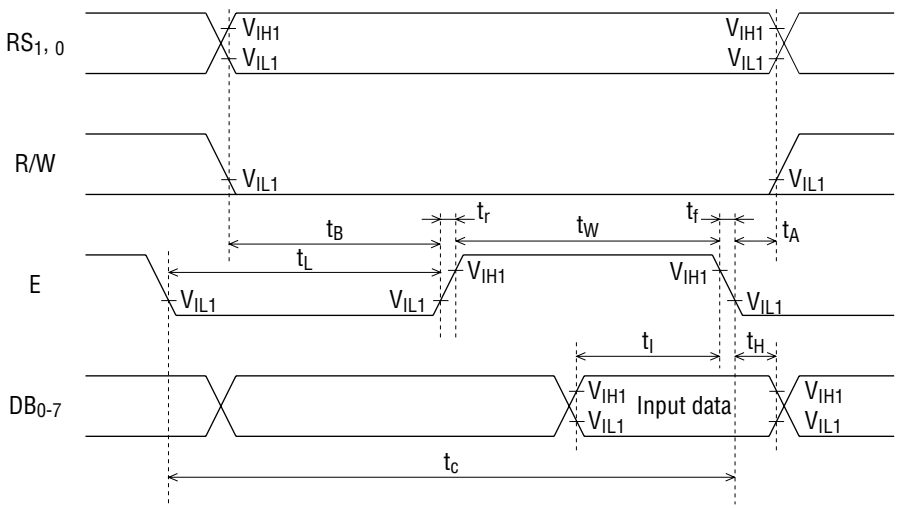
(Note 5) See Note 3 to "DC Characteristics."

Switching Characteristics

1. Timing for input from the CPU (write operation)

(V_{DD} = 4.5 to 5.5V, Ta = –30 to +85°C)

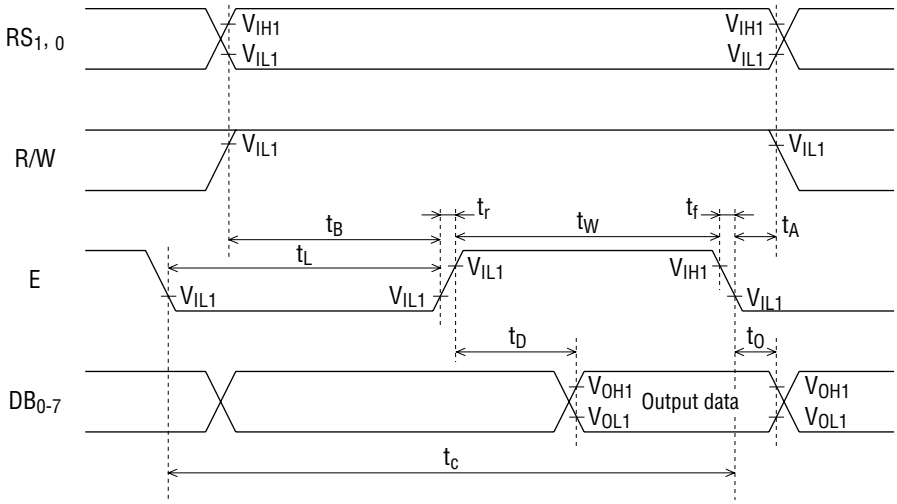
Parameter	Symbol	Min.	Typ.	Max.	Unit
R/W, RS_0 and RS_1 setup time	t_B	40	—	—	ns
E "H" pulse width	t_W	220	—	—	ns
R/W, RS_0 and RS_1 hold time	t_A	10	—	—	ns
E rise time	t_r	—	—	20	ns
E fall time	t_f	—	—	20	ns
E "L" pulse width	t_L	210	—	—	ns
E cycle time	t_C	500	—	—	ns
DB_0 to DB_7 input data setup time	t_I	100	—	—	ns
DB_0 to DB_7 input data hold time	t_H	10	—	—	ns



2. Timing for output to the CPU (read operation)

(V_{DD} = 4.5 to 5.5V, Ta = –30 to +85°C)

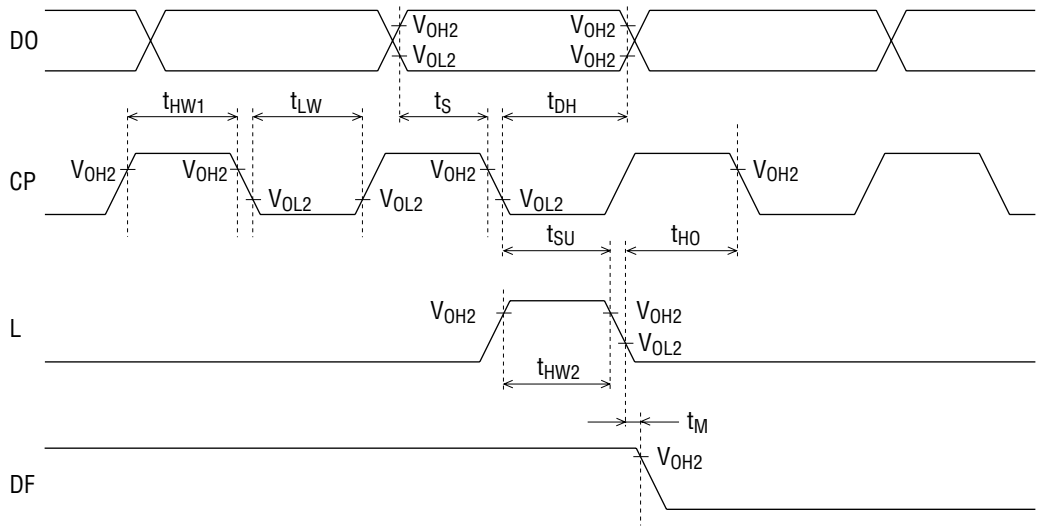
Parameter	Symbol	Min.	Typ.	Max.	Unit
R/W, RS_0 and RS_1 setup time	t_B	40	—	—	ns
E "H" pulse width	t_W	220	—	—	ns
R/W, RS_0 and RS_1 hold time	t_A	10	—	—	ns
E rise time	t_r	—	—	20	ns
E fall time	t_f	—	—	20	ns
E "L" pulse width	t_L	210	—	—	ns
E cycle time	t_C	500	—	—	ns
DB_0 to DB_7 data ouput delay time	t_D	—	—	150	ns
DB_0 to DB_7 data ouput hold time	t_O	20	—	—	ns



3. Timing for output to character extension IC

(V_{DD} = 4.5 to 5.5V, Ta = –30 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CP "H" pulse width	t_{HW1}	800	—	—	ns
CP "L" pulse width	t_{LW}	800	—	—	ns
DO setup time	t_S	300	—	—	ns
DO hold time	t_{DH}	300	—	—	ns
L clock setup time	t_{SU}	500	—	—	ns
L clock hold time	t_{HO}	100	—	—	ns
L "H" pulse width	t_{HW2}	800	—	—	ns
DF delay time	t_M	–1000	—	1000	ns



FUNCTIONAL DESCRIPTION

1. Instruction Register (IR), Data Register (DR), Contrast Register (CR)

These three registers are selected by the register selector pins, RS_0 and RS_1.
When RS_0 and RS_1 are "H" level input, the DR is selected and when RS_0 = "L" level input and RS_1 = "H", the IR is selected. On the other hand, when RS_0 and RS_1 are "L" level input, the CR is selected. (When RS_0 = "H" level input and RS_1 = "L", the registers are ignored.)
The IR is used to store the address codes for the display data RAM (DD RAM) or character generator RAM (CG RAM) and instruction codes.
The IR can be written into, but not be read out by the microcomputer (CPU).
The CR can be used to read out and write. The CR values provide 0 to 1F (hexadecimal) and when this value is 0, V_{LCD} is lowest. On the other hand, when it is 1F, it is highest. (The initial value is 1F.) Therefore, the contrast can be adjusted by varying the CR value (providing that V_5 and V_5' are connected).
The DR is used to write into/read out the data to/from the DD RAM or CG RAM.
The data written to the DR by the CPU is automatically written to the DD RAM or CG RAM as an internal operation.
When an address code is written to the IR, the data (of the specified address) is automatically transferred from the DD RAM or CG RAM to the DR. By having the CPU subsequently read the DR (from the DR data), it is possible to verify the DD RAM or CG RAM data.
After the writing of the DR by the CPU, the DD RAM or CG RAM of the next address is selected to be ready for the next CPU writing. Likewise, after the reading out of the DR by the CPU, the DD RAM or CG RAM data is read out by the DR to be ready for the next CPU reading.
Write/read to and from the three registers is carried out by the READ/WRITE (R/W) pin.

Table 1 Register and R/W pins function table

R/W	RS_0	RS_1	Function
L	L	H	IR write
H	L	H	Read of busy flag (BF) and address counter (ADC)
L	H	H	DR write
H	H	H	DR read
L	L	L	CR write
H	L	L	CR read

2. Busy Flag (BF)

When the busy flag output is at "H", it indicates that the MSM6562B-xx is engaged in internal operation.
When the busy flag is at "H" level, any new instruction is ignored.
When R/W = "H", RS_0 = "L", and RS_1 = "H", the busy flag is output from DB_7.
New instruction should be input when BF is "L" level.
When the busy flag is set to "H", the output code of the address counter (ADC) are undefined.

3. Address Counter (ADC)

The address counter (ADC) allocates the address for the DD RAM and CG RAM and also for the cursor display.
When the instruction code for the DD RAM address or CG RAM address setting is input to the IR, after deciding whether it is the DD RAM or CG RAM, the address code is transferred from the IR to the ADC. After writing (reading) the display data to (from) the DD RAM or CG RAM, the ADC is automatically incremented (decremented) by 1 as its internal operation.
The data of the ADC is output to DB_0 - DB_6 under the conditions that R/W = "H", RS_0 = "L", RS_1 = "H" and BF = "L".

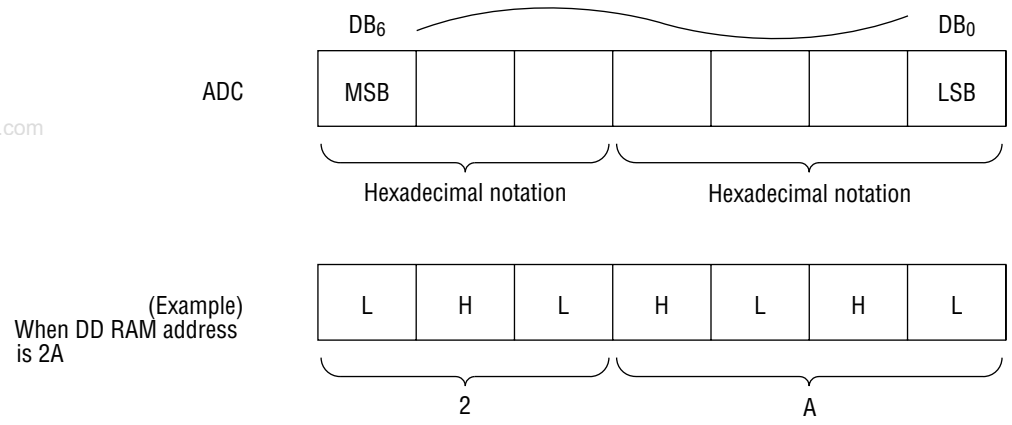
4. Timing Generator Circuit

This circuit generates timing signals used for internal operations upon receipt of CPU instruction. It also generates timing signals for activating such internal circuits as the DD RAM, CG RAM and CG ROM.
It is so designed that the internal operation caused by accessing from the CPU will not interfere with the internal operation caused by the LCD display.
Consequently, when data is written from the CPU to DD RAM no ill effect, e.g., flickering occurs in portions other than the display where the data is written.
In addition, the circuit generates transfer signals to the character extension IC (MSM5259).

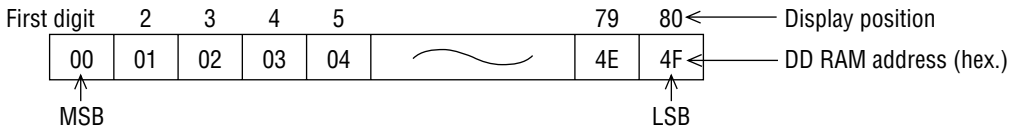
5. Display Data RAM (DD RAM)

This RAM is used to store the display data of 8-bit character codes (see Table 2).
DD RAM address corresponds to the display position of the LCD. The correspondence between the two is described in the following.

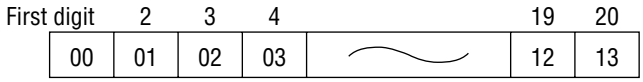
DD RAM address (set to ADC) is expressed in hexadecimal notation as shown below:



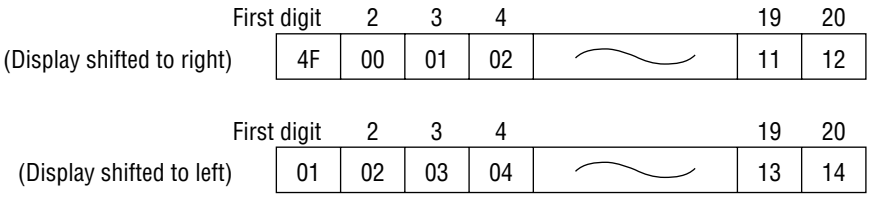
1-1) Correspondence between address and display position in the 1-line display mode



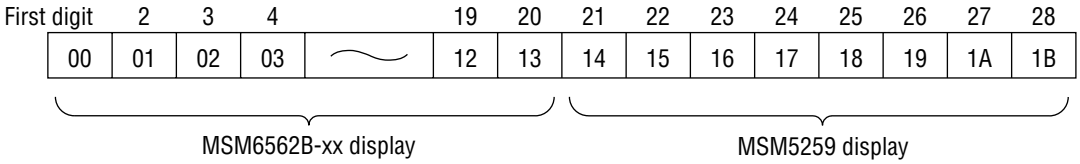
1-2) When the MSM6562B-xx alone is used, up to 20 characters can be displayed from the first digit to the twentieth digit.



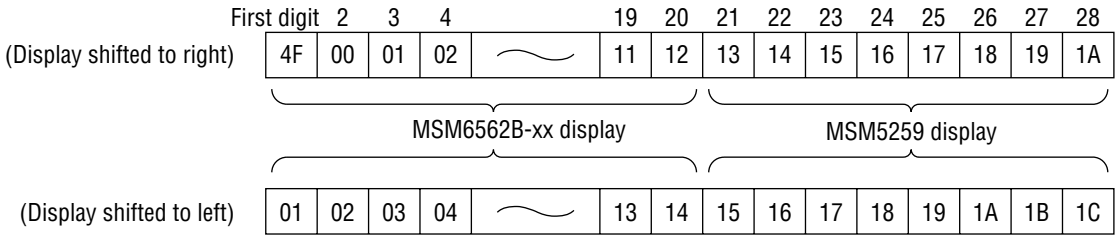
When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:



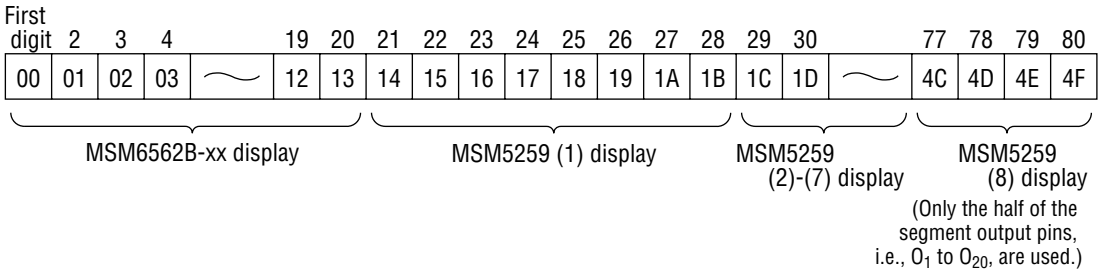
1-3) When the MSM6562B-xx is used with one MSM5259, up to 28 characters can be displayed from the first digit to the twenty-eighth digit as shown below:



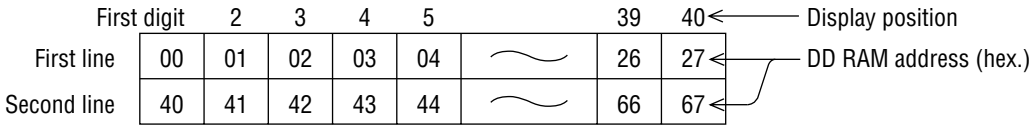
When the display is shifted by instruction, the correspondence between the LCD display and DD RAM address changes as shown below:



1-4) Since the MSM6562B-xx has a DD RAM with a capacity of 80 characters, up to 8 devices of MSM5259 can be connected to MSM6562B-xx so that 80 characters can be displayed.



2-1) Correspondence between address and display position in the 2-line display mode



(Note) Note that the last address of the first line and the leading address of the second line are not consecutive.

2-2) When the MSM6562B-xx alone is used, up to 40 characters (20 character × 2 lines) can be displayed from the first digit to the twentieth digit.

	First digit	2	3	4		19	20
First line	00	01	02	03	~	12	13
Second line	40	41	42	43	~	52	53

When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit	2	3	4		19	20
First line	27	00	01	02	~	11	12
Second line	67	40	41	42	~	51	52

(Display shifted to left)

	First digit	2	3	4		19	20
First line	01	02	03	04	~	13	14
Second line	41	42	43	44	~	53	54

2-3) When the MSM6562B-xx is used with one MSM5259, up to 56 characters (28 characters × 2 lines) can be displayed from the first digit to the twenty-eighth digit as shown below:

	First digit	2	3	4		19	20	21	22	23	24	25	26	27	28
First line	00	01	02	03	~	12	13	14	15	16	17	18	19	1A	1B
Second line	40	41	42	43	~	52	53	54	55	56	57	58	59	5A	5B

MSM6562B-xx display MSM5259 display

When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit	2	3	4		19	20	21	22	23	24	25	26	27	28
First line	27	00	01	02	~	11	12	13	14	15	16	17	18	19	1A
Second line	67	40	41	42	~	51	52	53	54	55	56	57	58	59	5A

MSM6562B-xx display MSM5259 display

(Display shifted to left)

	First digit	2	3	4		19	20	21	22	23	24	25	26	27	28
First line	01	02	03	04	~	13	14	15	16	17	18	19	1A	1B	1C
Second line	41	42	43	44	~	53	54	55	56	57	58	59	5A	5B	5C

MSM6562B-xx display MSM5259 display

2-4) Since the MSM6562B-xx has a DD RAM with a capacity of 80 characters, up to 3 devices of MSM5259 can be connected to the MSM6562B-xx in the 2-line display mode.

First digit	2	3	4		19	20	21	22	23	24	25	26	27	28	29	30		37	38	39	40
00	01	02	03	~	12	13	14	15	16	17	18	19	1A	1B	1C	1D	~	24	25	26	27
40	41	42	43	~	52	53	54	55	56	57	58	59	5A	5B	5C	5D	~	64	65	66	67

MSM6562B display MSM5259 (1) display MSM5259 (2) display MSM5259 (3) display

(Only the half of the segment output pins, i.e., O_1 to O_{20}, are used.)

6. Character Generator ROM (CG ROM)

The CG ROM is used to generate 5 × 7 dot (160 kinds) character patterns or 5 × 10 dot (32 kinds) character patterns from an 8-bit DD RAM character code signal.
The correspondence of 8-bit character codes to character patterns is shown in Table 2.
When the 8-bit character code of the CG ROM is written to the DD RAM, the character pattern of the CG ROM corresponding to the code is displayed on the LCD display position corresponding to the DD RAM address.

Table 2 Character codes and character patterns of standard code (MSM6562B-01)

Lower 4 bits \ Upper 4 bits	MSB 0000	0010		0011		0100		0101		0110		0111		1010		1011		1100		1101		1110		1111	
0000 LSB	CG RAM (1)			0		@		P		\		p				ー		タ		ミ		α		P	
0001	(2)	!		1		A		Q		a		q		。		ア		チ		ム		ä		q	
0010	(3)	″		2		B		R		b		r		「		イ		ツ		メ		β		Θ	
0011	(4)	#		3		C		S		c		s		」		ウ		テ		モ		ε		∞	
0100	(5)	$		4		D		T		d		t		、		エ		ト		ヤ		μ		Ω	
0101	(6)	%		5		E		U		e		u		•		オ		ナ		ユ		σ		ü	
0110	(7)	&		6		F		V		f		v		ヲ		カ		ニ		ヨ		ρ		Σ	
0111	(8)	’		7		G		W		g		w		ァ		キ		ヌ		ラ		g		π	
1000	(1)	(		8		H		X		h		x		ィ		ク		ネ		リ		√		$\overline{X}$	
1001	(2)	)		9		I		Y		i		y		ゥ		ケ		ノ		ル		−1		y	
1010	(3)	*		:		J		Z		j		z		ェ		コ		ハ		レ		j		千	
1011	(4)	+		;		K		[		k		{		ォ		サ		ヒ		ロ		x		万	
1100	(5)	,		<		L		¥		l		|		ャ		シ		フ		ワ		¢		円	
1101	(9)	−		=		M		]		m		}		ュ		ス		ヘ		ン		£		÷	
1110	(7)	.		>		N		^		n		→		ョ		セ		ホ		゛		$\overline{n}$			
1111	(8)	/		?		O		_		o		←		ッ		ソ		マ		゜		ö		■	

7. Character Generator RAM (CG RAM)

The CG RAM is used to display user's original character patterns other than those stored in the CG ROM.
The CG RAM has the capacity (64 bytes = 512 bits) to write 8 kinds for 5 × 7 dots or 4 kinds for 5 × 10 dots.
When displaying character patterns stored in the CG RAM, write 8-bit character codes (00 to 07 or 08 to 0F; hex.) shown on the left in Table 2 to the DD RAM. It is then possible to output the character pattern to the LCD display position corresponding to the DD RAM address.
The following is a description on how to write and read character patterns to and from the CG RAM.

(1) When the character pattern is 5 × 7 dots (see Table 3)

- Method of writing character pattern into the CG RAM by the CPU :
  The CG RAM address bits 0 to 2 correspond to the line position of the character pattern. First, set increment or decrement by the CPU, and then input the CG RAM address. After this, write character pattern into the CG RAM through DB_0 to DB_7 line by line. DB_0 to DB_7 correspond to the CG RAM data bits 0 to 7 in Table 3.
  The display of the character pattern is turned on when "H" is set as input data, while it is turned off when "L" is set as the input data.
  Since the ADC is automatically incremented or decremented by 1 after writing the data to the CG RAM, it is not necessary to set the CG RAM address again.
  When performing a cursor indication, set to "0" all the input data for the line the CG RAM address bits 0 to 2 of which are all "1".
  Although the CG RAM data bits 0 ~ 4 are output to the LCD as display data, the CG RAM data bits 5 ~ 7 are not. It is possible, however, to use the CG RAM as a data RAM.

- Method of displaying the CG RAM character pattern to the LCD :
  The CG RAM is selected when high-order 4 bits of the character code are all "L".
  Since bit 3 of the character code is invalid, the display of "0" in Table 3 is selected by character code "00" or "08" (hex.). When the 8-bit character code of the CG RAM is written to the DD RAM, the character pattern of the CG RAM is displayed on the LCD display position corresponding to the DD RAM address. (DD RAM data bits 0 to 2 correspond to CG RAM address bits 3 to 5.)

(2) When the character pattern is 5 × 10 dots (see Table 4).

- Method of writing character pattern into the CG RAM by the CPU :
  The CG RAM address bits 0 to 3 correspond to the line position of the character pattern. First, set increment or decrement by the CPU, and then input the CG RAM address. After this, write the character pattern into the CG RAM through DB_0 to DB_7 line by line. DB_0 to DB_7 correspond to the CG RAM data bits 0 to 7, in Table 4.
  The display of the character pattern is turned on when "H" is set as the input data, while it is turned off when "L" is set as the input data.
  Since the ADC is automatically incremented or decremented by 1 after writing the data to the CG RAM, it is not necessary to set the CG RAM address again.
  When performing a cursor indication, set to "0" all the input data for the line the CG RAM address bits 0 to 2 are all "1".
  CG RAM data is displayed on the LCD when the CG RAM data ranges from CG RAM data bits 0 to 4 and the CG RAM addresses (address bits 0 to 3) are "0" to "A" (hex.). Other CG RAM data is not displayed on the LCD (that is, when the CG RAM data ranges from CG RAM data bits 5 to 7 and the CG RAM addresses (address bits 0 to 3) are "B" to "F" (hex.)). It is possible, however, to read such CG RAM data through DB_0 to DB_7.

- Method of displaying the CG RAM character pattern to the LCD :
  The CG RAM is selected when high-order 4 bits of the character code are all "L". Since bits 0 and 3 of the character code are invalid, the display of "β" in Table 4 is selected by character codes "00", "01", "08" and "09" (hex.).
  When the 8-bit character code of the CG RAM character code is written to the DD RAM, the character pattern of the CG RAM is displayed on the LCD display position corresponding to the DD RAM address.
  (DD RAM data bits 1 to 2 correspond to CG RAM address bits 4 to 5.)

Table 3 Example of the CG RAM data (character pattern) corresponding to the CG RAM addresses when the character pattern is 5×7 dots, and relationship between character patterns and the DD RAM data

CG RAM address	CG RAM data (character pattern)		DD RAM data (character code)
5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB		7 6 5 4 3 2 1 0 MSB LSB
0 0 0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	X X X 0 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 1 0 0 0 0 0 0		0 0 0 0 X 0 0 0
0 0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	X X X 1 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 0 0 0 0		0 0 0 0 X 0 0 1
~	~		~
1 1 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	X X X 0 1 1 1 1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 1 1 1 0 0 0 0 0 0		0 0 0 0 X 1 1 1

X : Don't Care

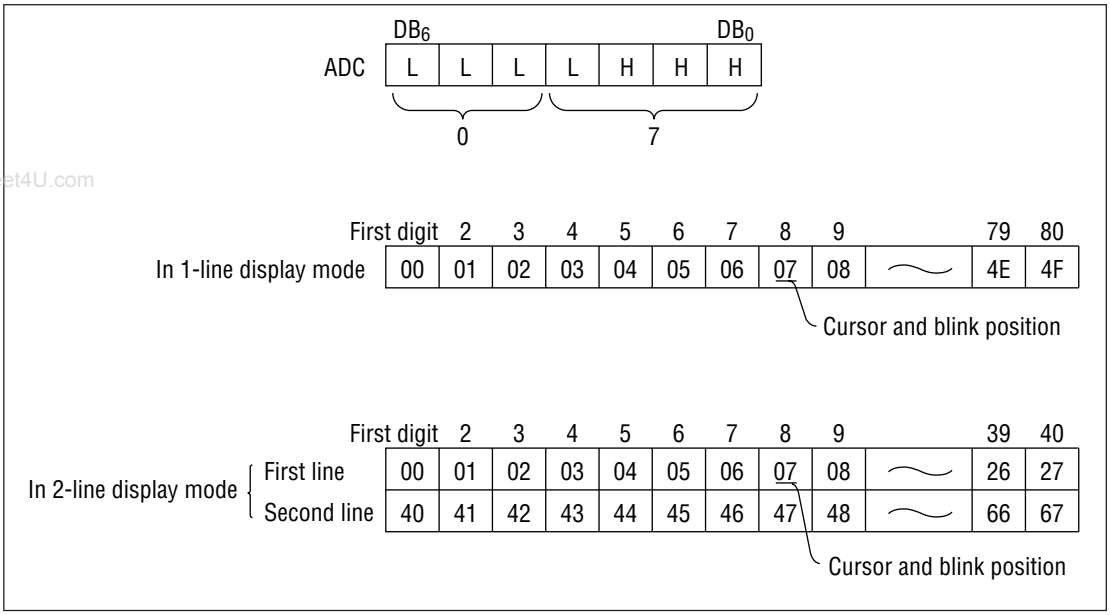
Table 4 Example of the CG RAM data (character pattern) corresponding to the CG RAM addresses when the character pattern is 5 × 10 dots, and relationship between character patterns and the DD RAM data

CG RAM address	CG RAM data (character pattern)		DD RAM data (character code)
5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB		7 6 5 4 3 2 1 0 MSB LSB
0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	X X X 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 1 1 1 0 1 0 0 0 1 1 1 1 1 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 X X X X X		0 0 0 0 X 0 0 X
0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	X X X 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 1 1 1 1 0 0 0 0 1 0 0 0 0 1 0 1 1 1 0 0 0 0 0 0 X X X X X		0 0 0 0 X 0 1 X
0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	X X X 0 0 0 0 0 0 0 0 0 0 1 1 0 1 1 0 1 0 1 0 1 0 0 0 1 1 0 0 0 1 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 X X X X X		0 0 0 0 X 1 1 X

X : Don't care

8. Cursor and Blink Control Circuit

This circuit generates the LCD cursor and blink.
This circuit is under the control of the CPU program. The display of the cursor or blink on the LCD is made at a position corresponding to the DD RAM address set to the ADC.
The figure below shows an example of the cursor and blink position when the value of the ADC is set at "07" (hex.).



(Note) The cursor and blink are displayed even when the CG RAM address is set to the ADC. For this reason, it is necessary to inhibit the display of the cursor and blink while the CG RAM address is set to the ADC.

9. LCD Display Circuit (COM_1 to COM_{16}, SEG_1 to SEG_{100}, L, CP, DO, DF, SHL_0, SHL_1) :

Since the MSM6562B-xx provides the COM signal outputs (16 outputs) and the SEG signal outputs (100 outputs), even a single MSM6562B-xx device can display 20 characters (1-line display) or 40 characters (2-line display).
The character pattern data is converted into the serial data and is serially transferred through the shift register. The transfer direction of the serial data is controlled by SHL_0 and SHL_1 and is shown as follows.

SHL_0	SHL_1	Transfer direction
L	L	$SEG_1 \rightarrow SEG_{100}$
L	H	$SEG_{100} \rightarrow SEG_1$
H	L	$SEG_1 \rightarrow SEG_{50} \Rightarrow SEG_{100} \rightarrow SEG_{51}$
H	H	$SEG_{100} \rightarrow SEG_1$

Connect SHL_0 and SHL_1 to V_{DD} or V_{SS}. Keep the set states of the SHL_0 and SHL_1 pins unchanged during IC operation.

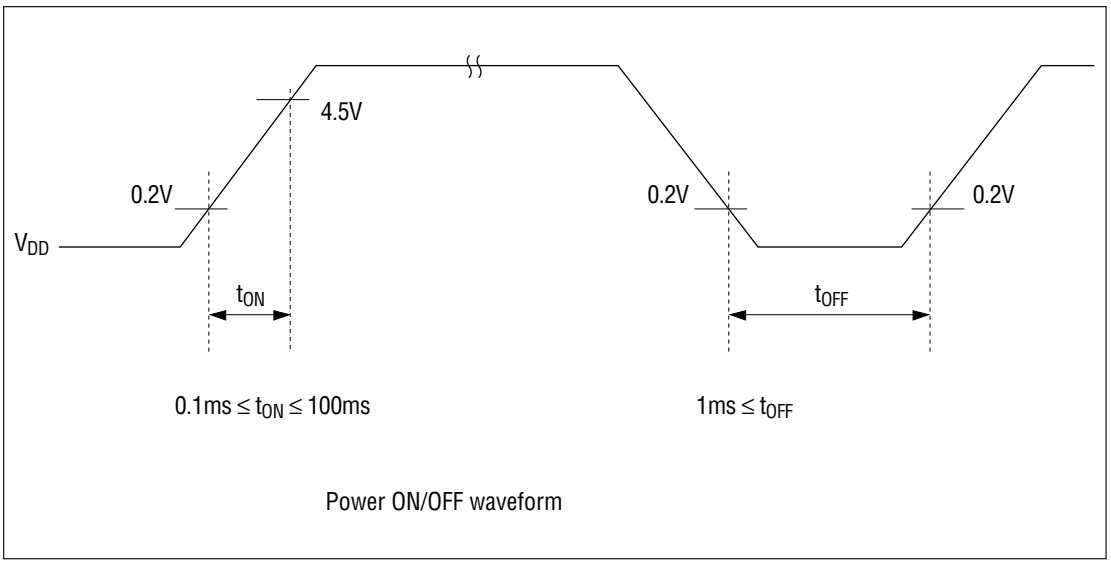
The SEG_1 to SEG_{100} are used to display 20-digit display on the LCD. To display more than 20 digits, the character extension IC (MSM5259) is used.
The character extension IC (MSM5259) is an extended IC for segment signal output. Interfacing with the MSM5259 is provided through data output pin (DO), clock output pin (CP), latch output pin (L), and display frequency pin (DF). The character pattern data is serially transferred to the MSM5259 through DO and CP. When 60-character (= 1-line display) or 20-character (= 2-line display) is output, the latch pulse is also output through pin L. By this latch pulse, the data transferred serially to the MSM5259 is latched to be used as the display data. The display frequency (DF) signal required when the LCD is displayed is also output from DF pin in synchronization with this latch pulse.

10. Built-in Reset Circuit

The MSM6562B-xx is automatically initialized when the power is turned on.
During initialization, the busy flag (BF) holds "H" and does not accept instructions (other than the busy flag read).
The busy flag goes to "H" for 15 ms after V_{DD} reaches 4.5V or more.
During initialization, the MSM6562B-xx executes the following instructions :

- Display clear
- Data length of interface with CPU : 8 bits (8B/4B = "H")
- LCD : 1-line display (N = "L")
- Character font : 5 × 7 dots (F = "L")
- ADC : increment (I/D = "H")
- No display shift (S = "L")
- Display : Off (D = "L")
- Cursor : Off (C = "L")
- No blink (B = "L")
- Contrast data : 1F (hex.) set

When the built-in reset circuit is used, the power supply conditions shown in the figure below must be satisfied. If they are not satisfied, because in that case the built-in reset circuit does not operate normally, initialize the MSM6562B-xx by instruction through the CPU (see the section on instruction initialization).
If a battery is used as supply voltage source, be sure to initialize the instruction.



Power ON/OFF waveform

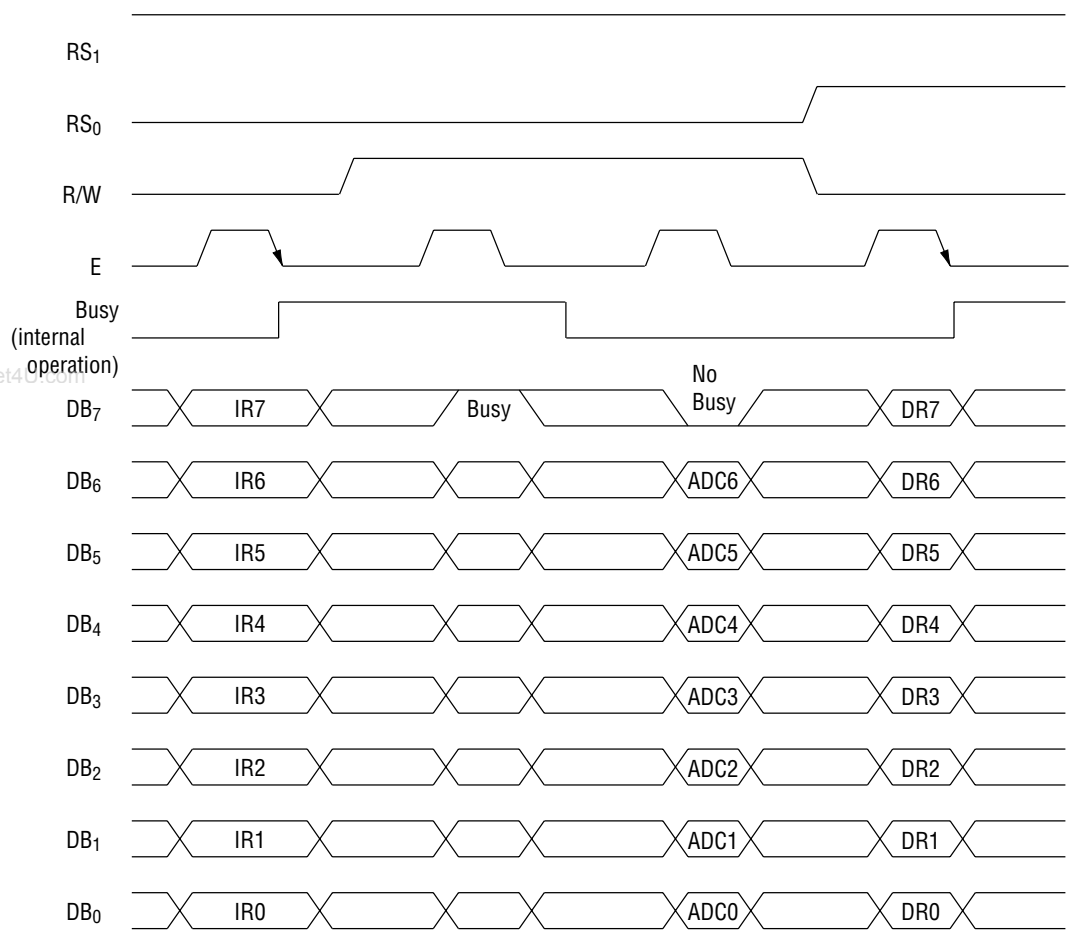
11. Data Bus with CPU

The MSM6562B-xx has either a one-step access in 8 bits or a two-step access in 4 bits to execute an instruction so that the MSM6562B-xx can interface with both an 8-bit CPU and a 4-bit CPU.

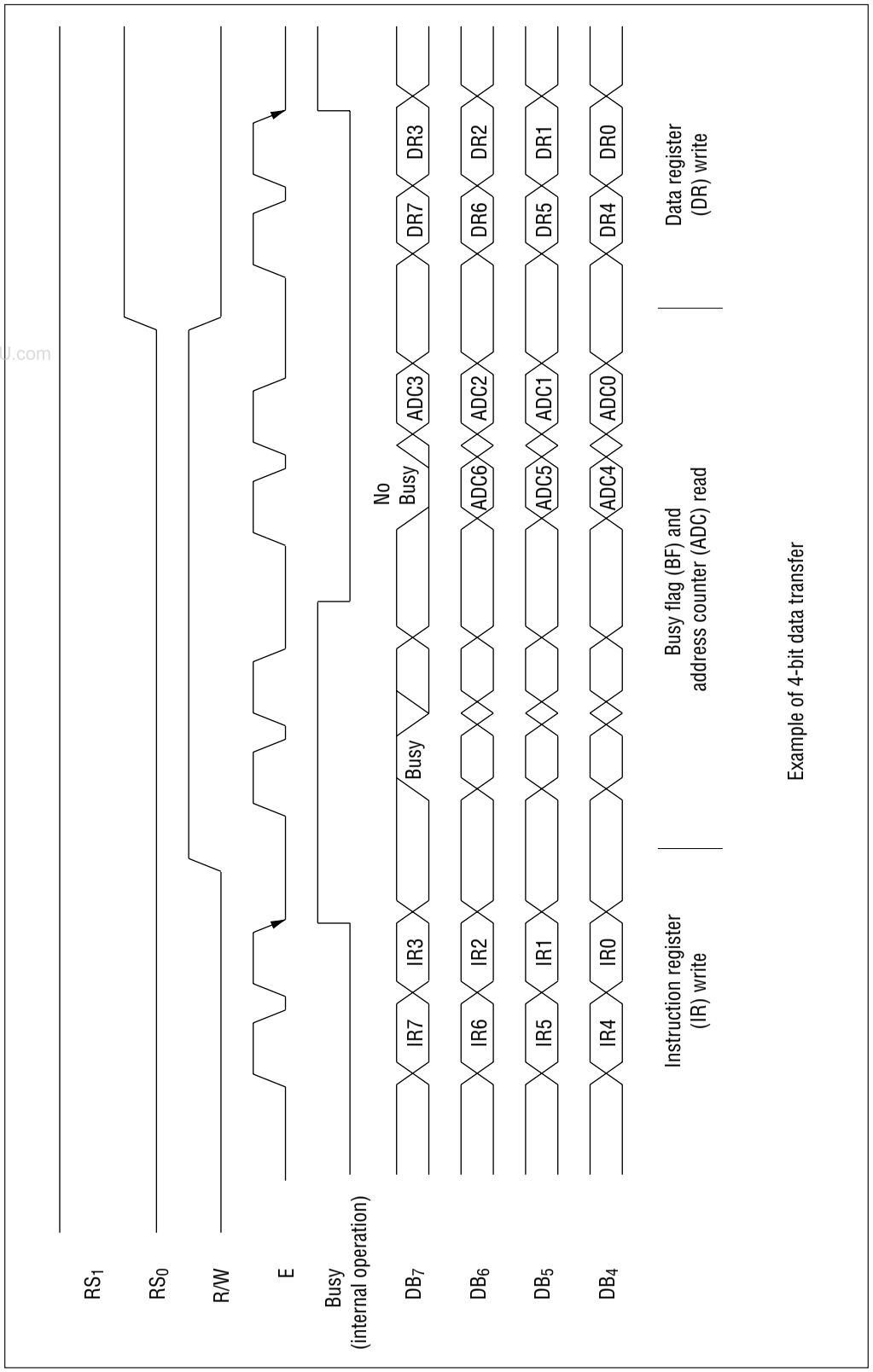
(1) When the interface data length is 8 bits
Data buses DB_0 to DB_7 (8 lines) are all used and data input/output is carried out in one step.

(2) When the interface data length is 4 bits
The 8-bit data input/output is carried out in two steps by using only high-order 4 bits of data buses DB_4 to DB_7 (4 lines).

The first time data input/output is made for high-order 4 bits (DB_4 to DB_7 when the interfaces data length is 8 bits) and the second time data input/output is made for low-order 4 bits (DB_0 to DB_3 when the interface data length is 8 bits). Even when the data input/output can be completely made through high-order 4 bits, be sure to make another input/output of low-order 4 bits. (Example : Busy flag read)
Since the data input/output is carried out in two steps but as one execution, no normal data transfer is executed from the next input/output if accessed only once.



Example of 8-bit data transfer



Example of 4-bit data transfer

12. Instruction Code

• Instruction code table

Instruction	Code											Description	Execution Time $f_{CP}=f_{OSC}$=250kHz
	RS1	RS0	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display clear	1	0	0	0	0	0	0	0	0	0	1	After all display are cleared, address counter for DD RAM is set to "00".	1.64ms
Cursor home	1	0	0	0	0	0	0	0	0	1	✻	Address counter for DD RAM is set to "00". The shifted display returns to the position before shift. The contents of the DD RAM are not changed.	1.64ms
Entry mode setting	1	0	0	0	0	0	0	0	1	I/D	S	Direction of the cursor move and whether display is shifted are set. Upon data write or read, the cursor and the display will actually be moved and shifted.	40µs
Display on/off control	1	0	0	0	0	0	0	1	D	C	B	The on/off of all display (D), the on/off of the cursor (C) and the blink (B) of the character at the cursor position are set.	40µs
Cursor/display shift	1	0	0	0	0	0	1	S/C	R/L	✻	✻	The cursor and display are shifted without changing the contents of the DD RAM.	40µs
Function setting	1	0	0	0	0	1	8B/4B	N	F	✻	✻	The interface data length (8B/4B), the display line numbers (N) and the character font (F) are set.	40µs
CG RAM address setting	1	0	0	0	1	ACG						The address of the CG RAM is set and then the CG RAM data is specified for the data for transmission and reception.	40µs
DD RAM address setting	1	0	0	1	ADD							The address of the DD RAM is set and then the DD RAM data is specified for the data for transmission and reception.	40µs
Busy flag/address read	1	0	1	BF	ADC							The busy flag (BF) indicating that the internal circuits are operating and the contents of address counter are read out.	1µs
CG RAM/DD RAM data write	1	1	0	WRITE DATA								Data is written into the DD RAM or CG RAM	40µs
CG RAM/DD RAM data read	1	1	1	READ DATA								Data is read out from the DD RAM or CG RAM.	40µs
Contrast adjusting data write	0	0	0	0	0	1	WRITE CONTRAST DATA					The data for contrast adjustment is written.	40µs
Contrast adjusting data read	0	0	1	0	0	0	READ CONTRAST DATA					The data for contrast adjustment is read.	40µs
	I/D=1 : Increment , I/D=0 : Decrement S=1 : Always involves display shift S/C=1 : Shift of display , S/C=0 : Shift of cursor R/L=1 : Shift to the right , R/L=0 : Shift to the left 8B/4B=1: 8 bits , 8B/4B=0 : 4 bits N=1 : 2 lines , N=0 : 1 line F=1 : 5×10-dots , F=0 : 5×7-dots BF=1 : Engaged in internal operation , BF=0 : Instruction acceptable											DD RAM : Display data RAM CG RAM : Character generator RAM ACG : CG RAM address ADD : DD RAM address, corresponding to the cursor address ADC : Address counter, used for both DD RAM and CG RAM	When the frequency is changed, the execution time is also changed. (Example) When f_{CP} or f_{OSC}=270kHz, 40µs × 250/270 = 37µs

✻: Don't Care

13. Description of Instructions

The instruction code is defined as the signal through which the MSM6562B-xx is accessed by the CPU.
The MSM6562B-xx begins operation upon receipt of the instruction code input.
As the internal processing operation of MSM6562B-xx is started with a timing that does not affect the LCD display, the busy status continues longer than the CPU cycle time.
Under the busy status (when the busy flag is set to "H"), the MSM6562B-xx does not execute any instructions other than the busy flag read.
Therefore, it must be confirmed before an instruction code is input from the CPU that the busy flag is set to "L".

(1) Display clear
When this instruction is executed, the LCD display is cleared.
The I/D value for the entry mode set instruction is set to 1 (increment). The S value for the entry mode set instruction does not change.
When the cursor and blink are being displayed, the blinking and cursor position moves to the left end of the LCD (the left end of the first line in the 2-line display mode).

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	0	0	0	0	0	0	0	1

(Note) All DD RAM data goes to "20" (hex.), while the address counter (ADC) goes to "00" (hex.) of the DD RAM address. The execution time when the OSC oscillation frequency is 250kHz is 1.64ms (max.).

(2) Cursor home
When this instruction is executed, the cursor and blinking position move to the left end of the LCD (to the left end of the first line in the 2-line display mode) when the cursor and blink are being displayed.
When the display is in shift, the display returns to its original position before shifting.

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	0	0	0	0	0	0	1	X

X : Don't Care

(Note) The address counter (ADC) goes to "00" (hex.) of the DD RAM address. The execution time when the OSC oscillation frequency is 250kHz is 1.64ms (max.).

(3) Entry mode set

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	0	0	0	0	0	1	I/D	S

① When the I/D is set, the 8-bit character code is written or read to and from the DD RAM, the cursor and blink shift to the right by 1 character position (I/D = "H"; increment) or to the left by 1 character position (I/D = "L"; decrement).
The address counter (ADC) is incremented (I/D = "H") or decremented (I/D = "L") by 1 at this time. Even after the character pattern code is written or read to and from the CG RAM, the address counter (ADC) is incremented (I/D = "H") or decremented (I/D = "L") by 1.

② When S = "H" is set, the character code is written to the DD RAM, and then the cursor and blink stop and the entire display shifts to the left (I/D = "H") or to the right (I/D = "L") by 1 character position.
When the character is read from the DD RAM when S = "H" is set, or when the character pattern data is written or read to or from the CG RAM when S = "H" is set, the entire display does not shift, but normal write/read is performed (the entire display does not shift, but the cursor and blink shift to the right (I/D = "H") or to the left (I/D = "L") by 1 character position).
When S = "L" is set, the display does not shift, but normal write/read is performed.
The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(4) Display ON/OFF control

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	0	0	0	0	1	D	C	B

① The D bit controls whether the character pattern is displayed or not.
When D is "H", this bit makes the character pattern display on the LCD.
When D is "L", this bit makes the display of the character pattern turned off. The cursor and blink are also cancelled at this time.

(Note) Different from the display clear, the DD RAM data is absolutely not rewritten.

② The cursor goes off when C = "L" and it is displayed when D = "H" and C = "H".

③ A blink is cancelled when B = "L" and a blink is executed when D = "H" and B = "H".
In the blink mode, all dots (including the cursor) and displaying character pattern (including the cursor) are displayed alternately at 409.6ms (in 5×7 dots character font) or 563.2ms (in 5 × 10 dots character font) when the OSC oscillation frequency is 250kHz.
The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(5) Cursor/display shift

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	0	0	0	1	S/C	R/L	X	X

X : Don't Care

When S/C = "L" and R/L = "L", the cursor and blink position are shifted to the left by 1 character position (the ADC is then decremented by 1).
When S/C = "L" and R/L = "H", the cursor and blink position are shifted to the right by 1 character position (the ADC is then incremented by 1).
When S/C = "H" and R/L = "L", the entire display is shifted to the left by 1 character position.

The cursor and blink position are also shifted together with the display (ADC remains unchanged).
When S/C = "H" and R/L = "H", the entire display is shifted to the right by 1 character position. The cursor and blink position are also shifted together with the display (ADC remains unchanged).
In the 2-line display mode, the cursor and blink position are shifted from the first line to the second line when the cursor is shifted to the right next to the fortieth digit (27; hex.) in the first line. No such shifting is made in other cases.
When shifting the entire display, the display pattern, cursor and blink position are not shifted between lines (from the first line to the second line or vice versa).
The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(6) Function set

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	0	0	1	8B/4B	N	F	X	X

X : Don't Care

① When 8B/4B = "H", the data input/output to and from the CPU is carried out in one step using 8 bits of DB_7 to DB_0. When 8B/4B = "L", the data input/output to and from the CPU is carried out in two steps using 4 bits of DB_7 to DB_4.

② The 2-line display mode of the LCD is selected when N = "H", while the 1-line display mode is selected when N = "L".

③ The 5 × 7 dots character font is slected when F = "L", while the 5 × 10 dots character font is selected when F = "H" and N = "L".

Do this initial setting prior to other instructions except the busy flag read after power is applied to the MSM6562B-xx. After that, no initial setting other than setting of 8B/4B value can be done.

N	F	Number of display lines	Character font	Duty ratio	Number of biases	Number of COMMON signals
L	L	1	5x7 dots	1/8	4	8
L	H	1	5x10 dots	1/11	4	11
H	L	2	5x7 dots	1/16	5	16
H	H	2	5x7 dots	1/16	5	16

The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(7) CG RAM address set

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	0	1	C_5	C_4	C_3	C_2	C_1	C_0

The CG RAM address is set to a value indicated by C_5 to C_0 (binary).
Once the CG RAM address is set, the CG RAM is specified until the DD RAM address is set.
Write/read of the character pattern to and from the CPU begins with the current CG RAM address indicated by C_5 to C_0.
The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(8) DD RAM address set

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	0	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0

The DD RAM address is set to a value indicated by D_6 to D_0 (binary).
Once the DD RAM address is set, the DD RAM is specified until the CG RAM address is set.
Write/read of the character code to and from the CPU begins with the current DD RAM address indicated by D_6 to D_0.
In the 1-line mode (N="L"), D_6 to D_0 (binary) must be set to one of the values among "00" to "4F" (hex.).
Likewise, in the 2-line mode (N="H"), D_6 to D_0 (binary) must be set to one of the values among "00" to "27" (hex.) or "40" to "67" (hex.).
When any value other than the above is input, it is impossible to make a normal write/read of character codes to and from the DD RAM.
The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(9) DD RAM and CG RAM data write

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	1	0	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0

E_7 to E_0 (binary) codes are written to the DD RAM or CG RAM. Once they are written, the cursor and display move as described in "(5) Cursor/display shift". The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(10) Busy flag and address counter read (execution time = 1μs)

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	0	1	BF	O_6	O_5	O_4	O_3	O_2	O_1	O_0

The busy flag (BF) is output by this instruction to indicate whether the MSM6562B is engaged in internal operations (BF = "H") or not (BF = "L").
When BF = "H", no new instruction is accepted. It is therefore necessary to confirm BF = "L" before inputting a new instruction.
When BF = "L", a correct address counter value is output. The address counter value must match the DD RAM address or CG RAM address. The decision of whether it is a DD RAM address or CG RAM address is made by the address previously set.
Since the address counter value when BF = "H" may be incremented or decremented by 1 during internal operations, it is not always a correct value.

(11) DD RAM and CG RAM data read

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	1	1	1	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Character codes (P_7 to P_0) are read from the DD RAM, and character patterns (P_7 to P_0) are read from the CG RAM.
Selection of DD RAM or CG RAM is decided by the address previously set.
After reading those data, the address counter (ADC) is incremented or decremented by 1 as set by the shift mode mentioned in item "(3) Entry mode setting".
The execution time, when the OSC oscillation frequency is 250kHz, is 40μs.

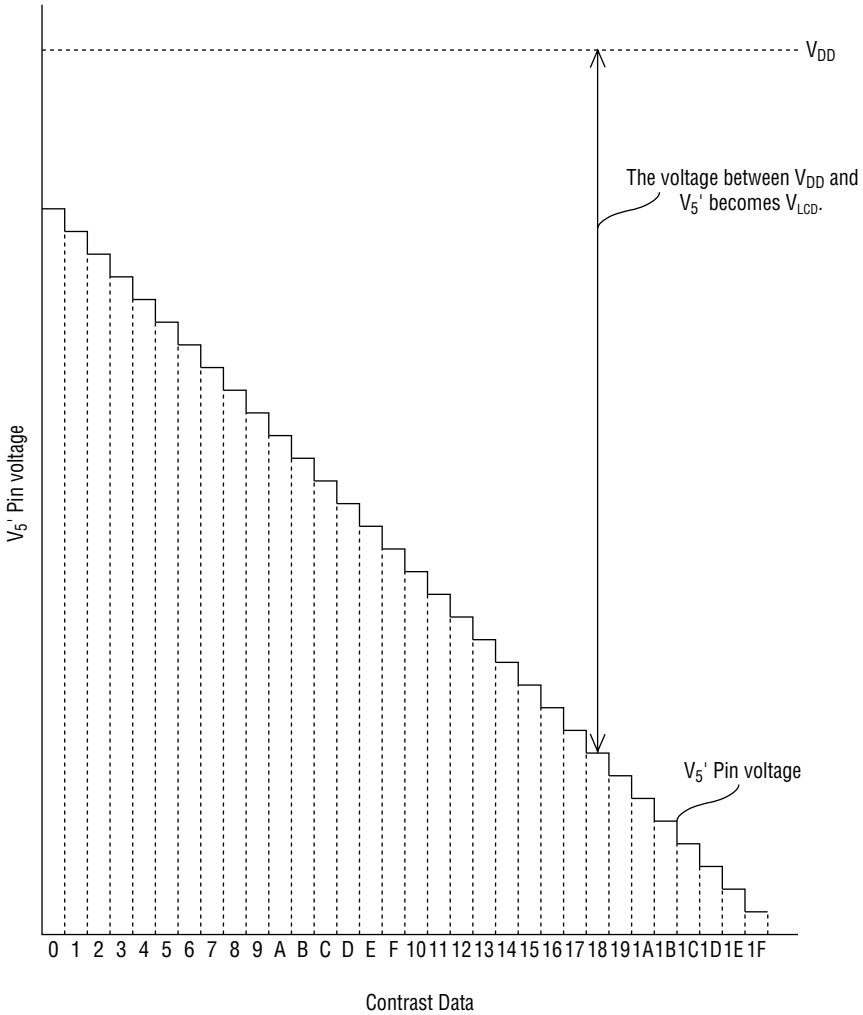
(Note) Correct data is read if any of the following conditions are met:
1 When the DD RAM address or CG RAM address setting instruction is input before inputting this instruction.
2 When the cursor/display shift instruction is input before inputting this instruction in cases where case the character code from the DD RAM is read.
3 When reading the data after the second reading from RAM when read more than once.

Correct data is not output in any other case.
The execution time, when the OSC oscillation frequency is 250kHz, is 40μs.

(12) Contrast adjusting data write

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	0	0	0	0	0	1	F_4	F_3	F_2	F_1	F_0

The contrast adjusting data (F_4 to F_0) is written to the contrast register. After writing, the voltage output to V_5' is changed according to the data. When the contents of the contrast register are "1F" (hex.), the V_{LCD} becomes maximum. When they are "00" (hex.), it becomes minimum.
(The contrast adjusting is valid only when the V_5' and V_5 pins are connected externally.)



The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

(13) Contrast adjusting data read

	RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	0	0	1	0	0	0	G_4	G_3	G_2	G_1	G_0

The contents (G_4 to G_0) of the contrast register are read out.
The execution time, when the OSC oscillation frequency is 250kHz, is 40µs.

14. Interface with LCD and the Character Extension IC (MSM5259)

Display examples when setting the 5 × 7 dots character font 1-line mode (Figure 1), 5 × 10 dots character font 1-line mode (Figure 2), and 5 × 7 dots character font 2-line mode (Figs. 3 and 4) through instructions are shown below.
When the 5 × 7 dots character font is set in the 1-line display mode, COM_9 to COM_{16} output the COM signals for turning the display off.
Likewise, when the 5 × 10 dots character font is set in the 1-line display mode, COM_{12} to COM_{16} output the COM signals for turning the display off.
The display examples show 20 characters (40 characters in Figure 3, 32 characters in Figure 4). When the number of MSM5259s are increased according to the increase in the number of characters, it is possible to display a maximum of 80 characters.

The bias voltage required to operate the LCD is made by a bias dividing resistor built in the MSM6562B-xx and this voltage must be input to the MSM5259.
These bias examples are shown in Figures 5, 6, 7 and 8 and there are following two ways for adjusting the bias voltage.
As shown in Figures 5 and 6, this method divides the bias by installing VR to V_5. On the other hand, as shown in Figures 7 and 8, this uses the built-in contrast adjusting circuit by connecting V_5 and V_5'.
Figure 9 shows the connection of the MSM6562B-xx and the MSM5259 including the bias circuit. (The example shows the display of 40 characters and 2 lines using the built-in contrast adjusting circuit.)
In addition, the bias voltage must keep the potential relation of $V_{DD} > V_1 > V_2 \geq V_3$ (= V_3') > V_4 > $V_5 \geq V_{SS}$.

- In the case of 1-line 20-character display (5 × 7 dot/font)

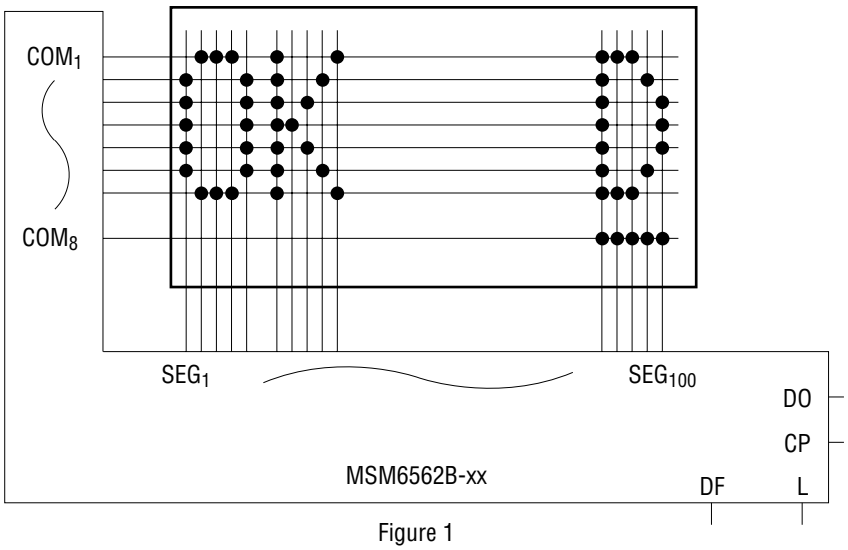


Figure 1

- In the case of 1-line 20-character display (5 × 10 dot/font)

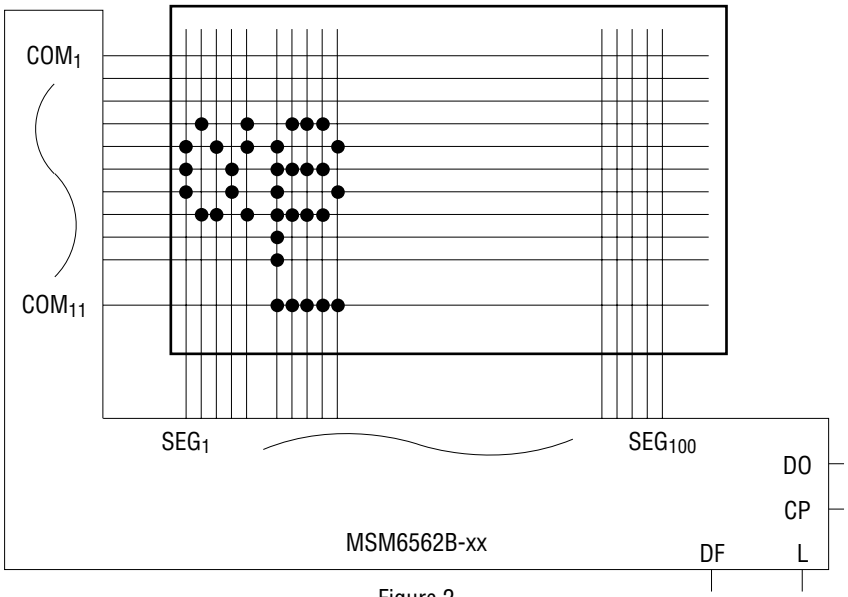


Figure 2

- In the case of 2-line 20 character display (5 × 7 dot/font)

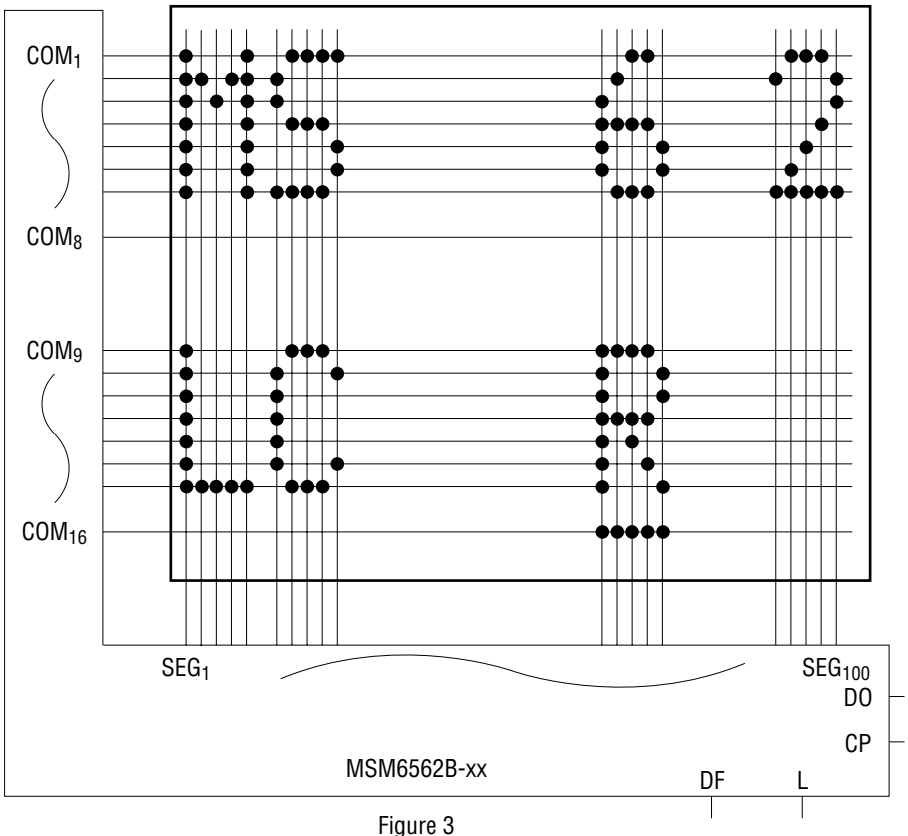


Figure 3

- In the case of 2-line 16-character display (5 × 7 dot/font)

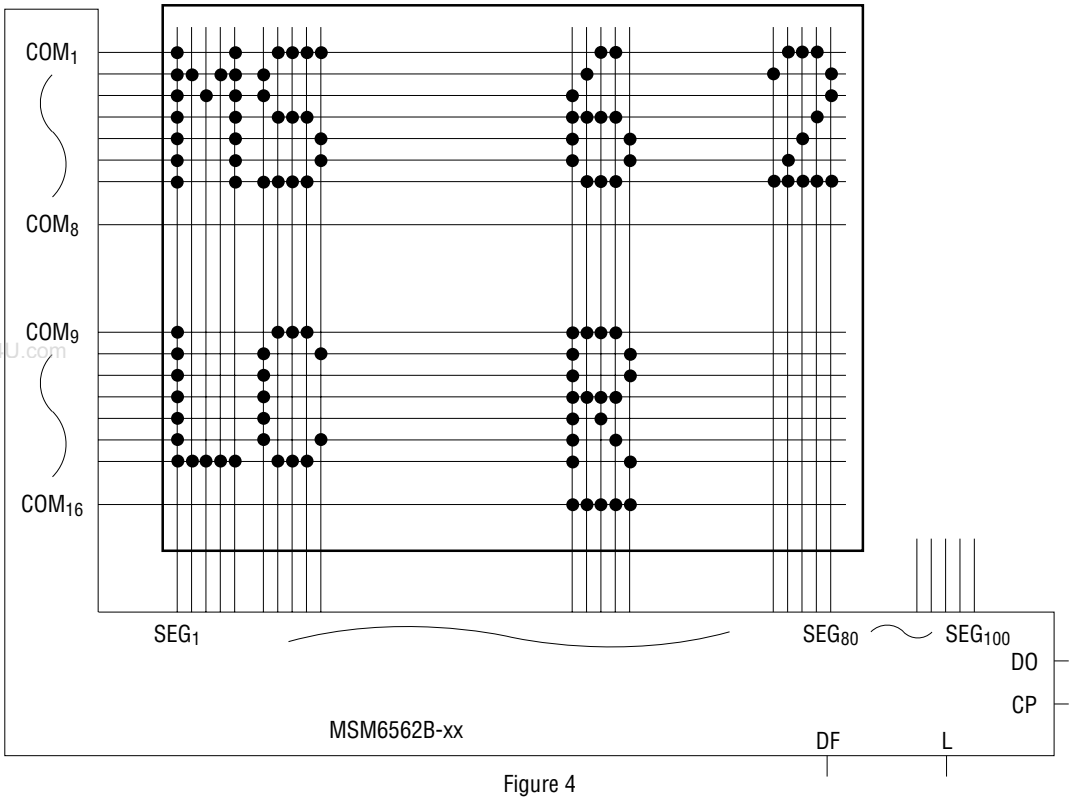


Figure 4

- V_{LCD} variable circuit using external VR (1-line display mode, 1/4 bias)

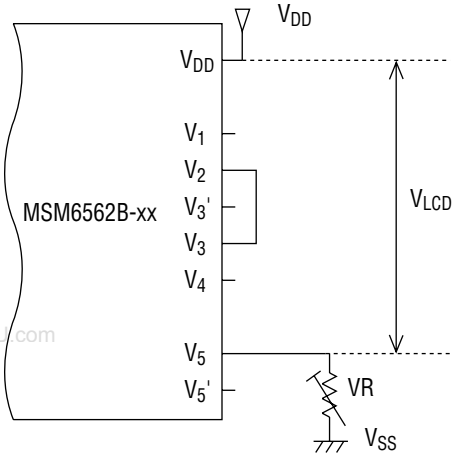


Figure 5

- V_{LCD} variable circuit using external VR (2-line display mode, 1/5 bias)

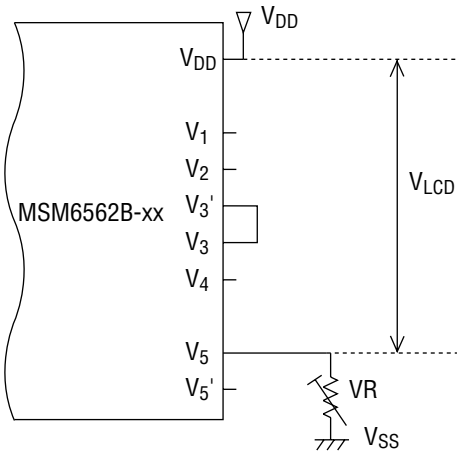


Figure 6

- Internal V_{LCD} variable circuit (1-line display mode, 1/4 bias)

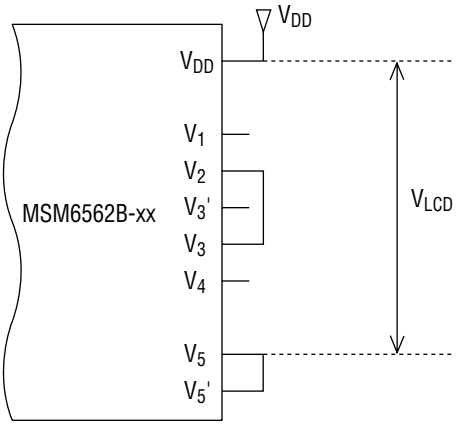


Figure 7

- Internal V_{LCD} variable circuit (2-line display mode, 1/5 bias)

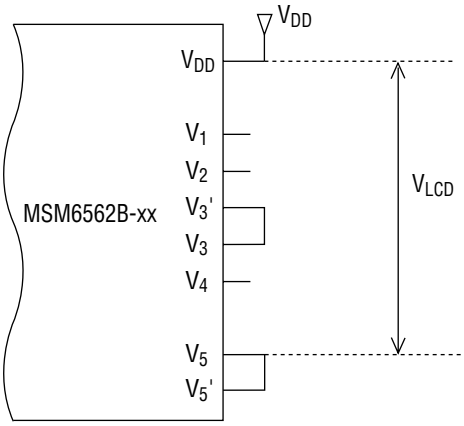


Figure 8

(V_{LCD} : LCD driving voltage)

- Connection between MSM6562B-xx and MSM5259 (40 characters, 2 lines)

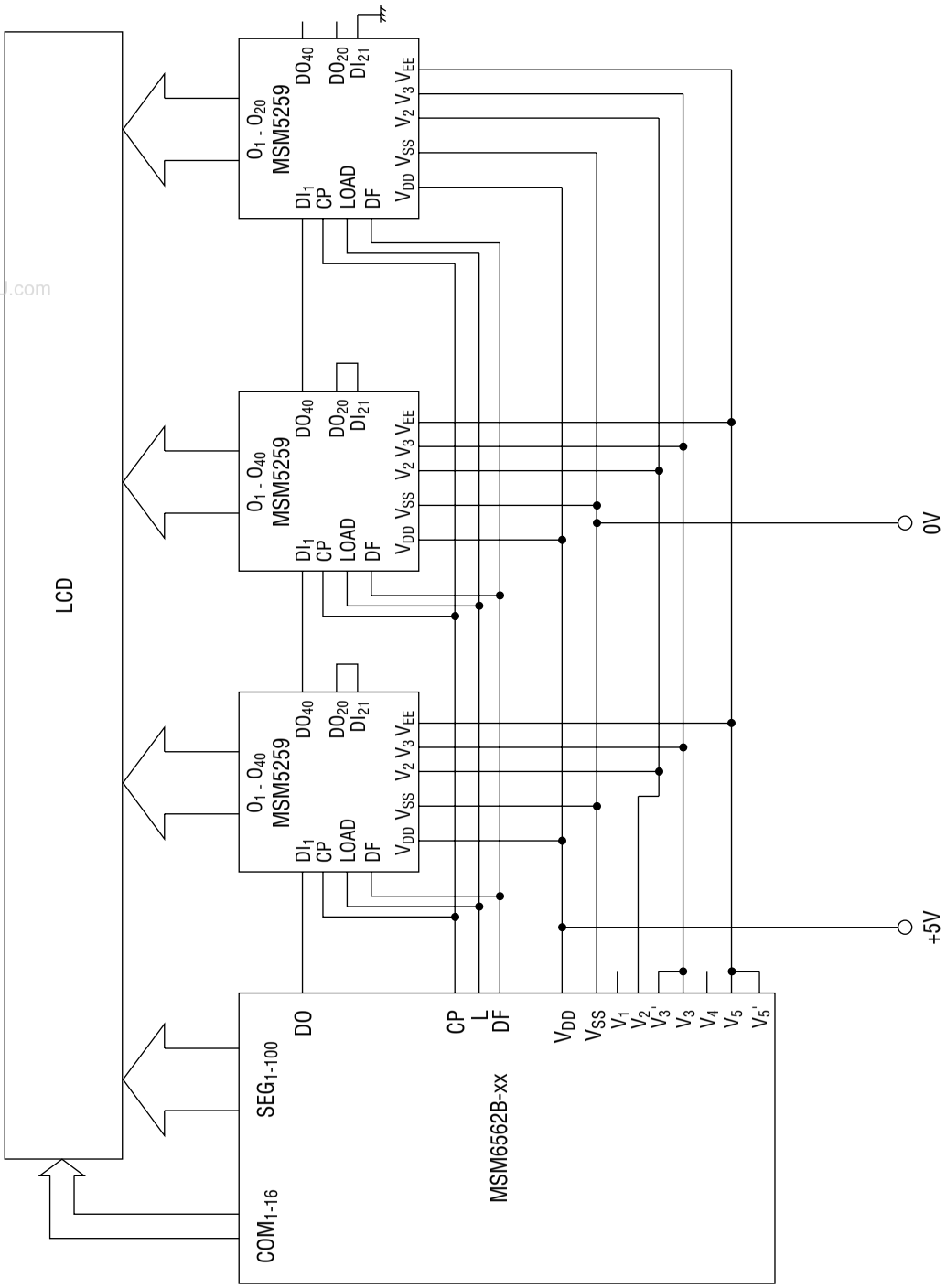


Figure 9

15. Instruction Initialization

(1) When data input/output to and from the CPU is carried out by 8 bits (DB_0 to DB_7) :

① • Turn on the power.
② • Wait for 15ms or more after V_{DD} has reached 4.5V or more.
③ • Set 8B/4B to "H" by the Function setting instruction.
④ • Wait for 4.1ms or more.
⑤ • Set 8B/4B to "H" by the Function setting instruction.
⑥ • Wait for 100µs or more.
⑦ • Set 8B/4B to "H" by the Function setting instruction.
⑧ • Check the busy flag as No Busy.
⑨ • Set 8B/4B to "H", the number of lines displayed on LCD (N) and character font (F) by the Function setting instruction.
(After this, the number of lines displayed on LCD and character font cannot be changed.)
⑩ • Check No Busy.
⑪ • Display off by the Display on/off control instruction.
⑫ • Check No Busy.
⑬ • Execute the Display clear instruction.
⑭ • Check No Busy.
⑮ • Execute the Entry mode setting instruction.
⑯ • Check No Busy.
⑰ • Initialization completed.

Example of Instruction Code for Steps ③, ⑤ and ⑦.

RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	0	0	0	1	1	X	X	X	X

X : Don't Care

(2) When data input/output to and from the CPU is carried out by 4 bits (DB_4 to DB_7) :

① • Turn on the power.
② • Wait for 15ms or more after V_{DD} has reached 4.5V or more.
③ • Set 8B/4B to "H" by the Function setting instruction.
④ • Wait for 4.1ms or more.
⑤ • Set 8B/4B to "H" by the Function setting instruction.
⑥ • Wait for 100µs or more.
⑦ • Set 8B/4B to "H" by the Function setting instruction.
⑧ • Check the busy flag as No Busy (or wait for 100µs or more).
⑨ • Set 8B/4B to "L" by the Function setting instruction.
⑩ • Wait for 100µs or more.
⑪ • Set 8B/4B to "L", the number of lines displayed on LCD (N) and character font (F) by the Function setting instruction.
(After this, the number of lines displayed on LCD and character font cannot be changed.)

⑫ • Check No Busy.
⑬ • Display off by the Display on/off control instruction.
⑭ • Check No Busy.
⑮ • Execute the Display clear instruction.
⑯ • Check No Busy.
⑰ • Execute the Entry mode setting instruction.
⑱ • Check No Busy.
⑲ • Initialization completed.

Example of Instruction Code for Steps ③, ⑤ and ⑦.

RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4
1	0	0	0	0	1	1

Example of Instruction Code for Step ⑧.

RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4
1	0	1	BF	O_6	O_5	O_4

Example of Instruction Code for Step ⑨.

RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4
1	0	0	0	0	1	0

Execute steps ⑪ to ⑱ with two-step accesses in 4 bits.

16. LCD Driving Waveforms

Figures 10, 11 and 12 show the LCD driving waveforms that consist of COM waveforms, SEG waveform, DF (display frequency) signal and L (latch pulse) signal, in the duty of 1/8, 1/11 and 1/16 respectively.
The relation between duty and frame frequency is as follows:

Duty	Frame frequency
1/8	78.1Hz
1/11	56.8Hz
1/16	78.1Hz

(Note) The OSC oscillation frequency is assumed to be 250kHz.

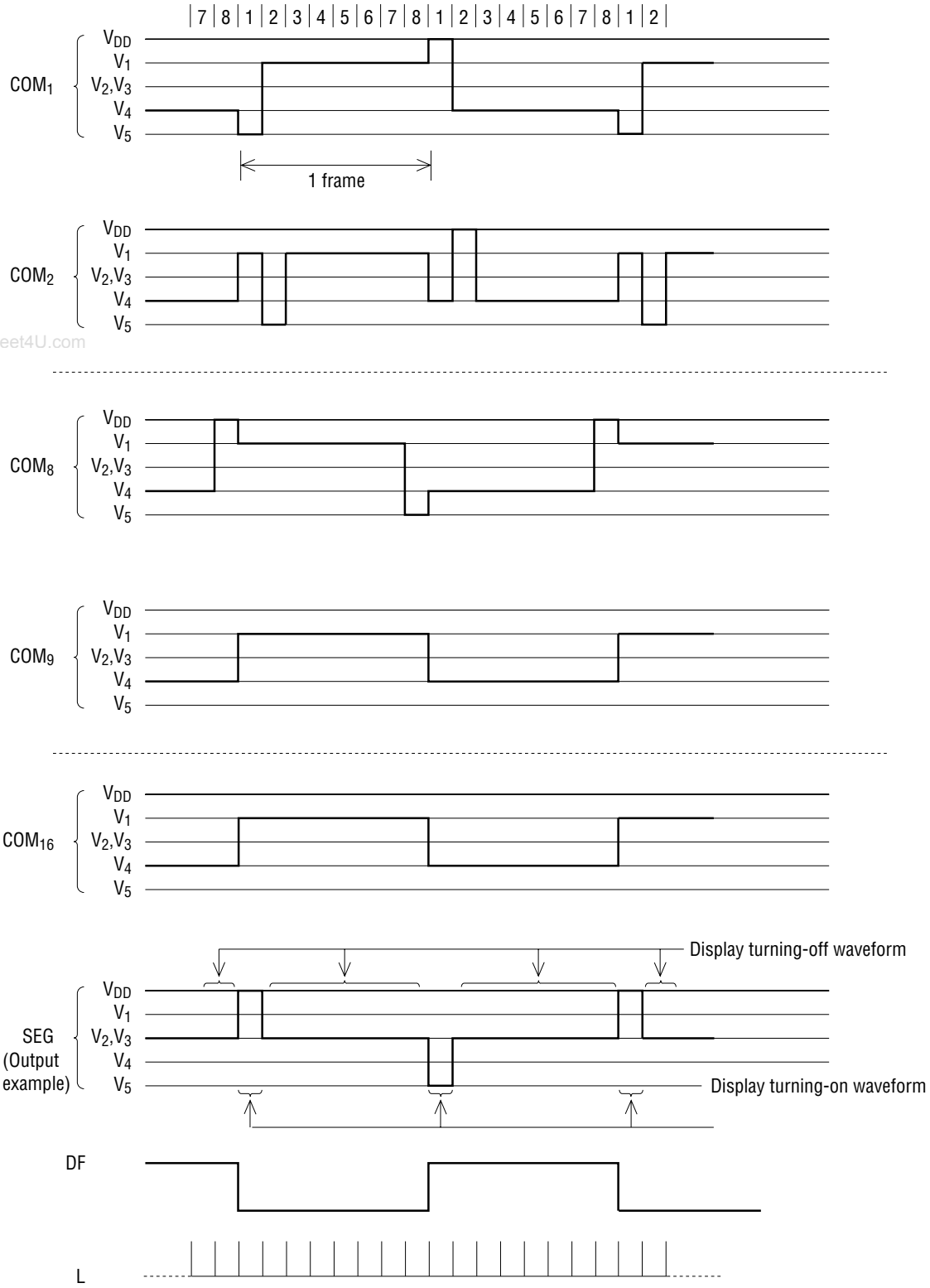


Figure 10 LCD driving waveforms at 1/8 duty

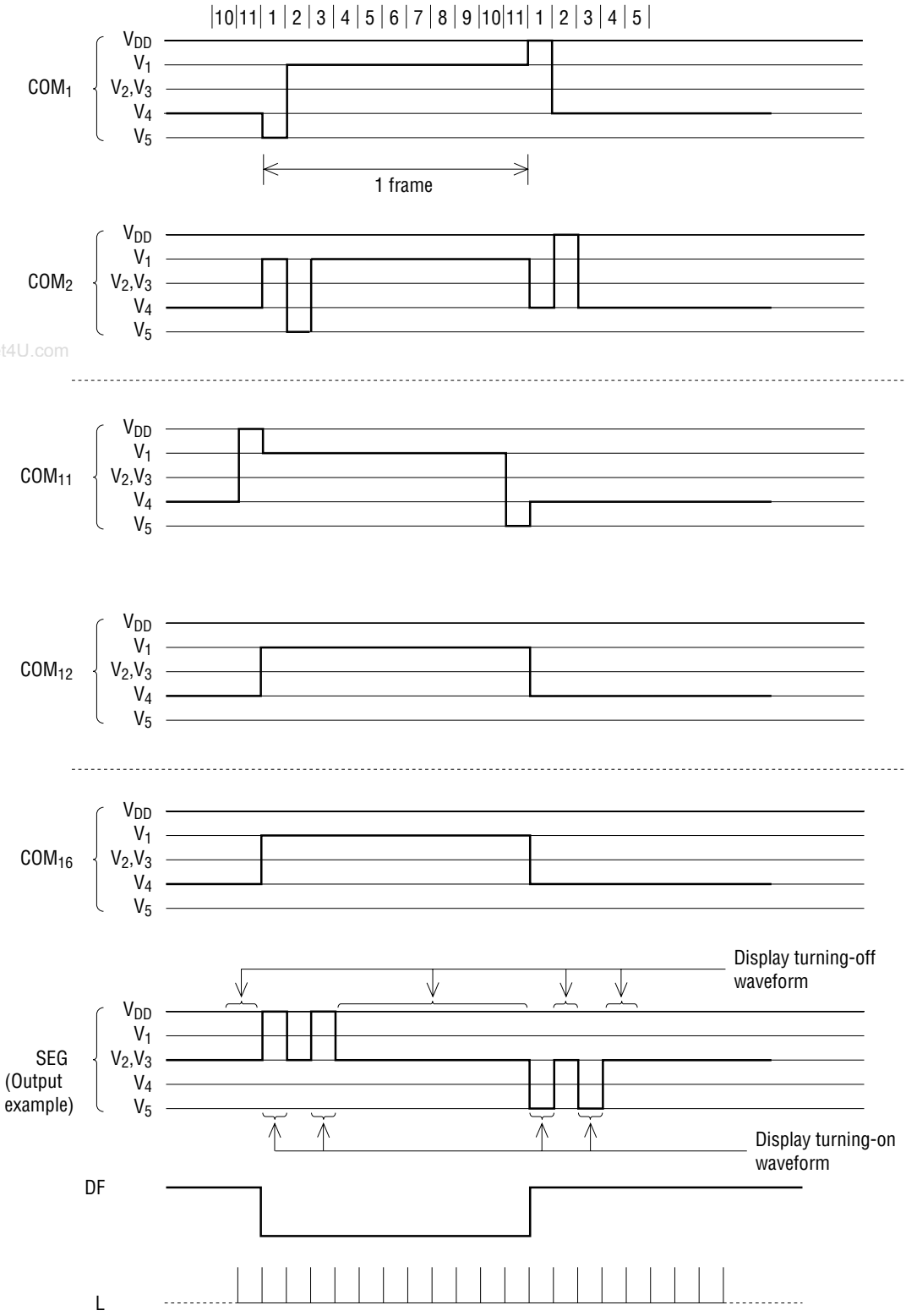


Figure 11 LCD driving waveforms at 1/11 duty

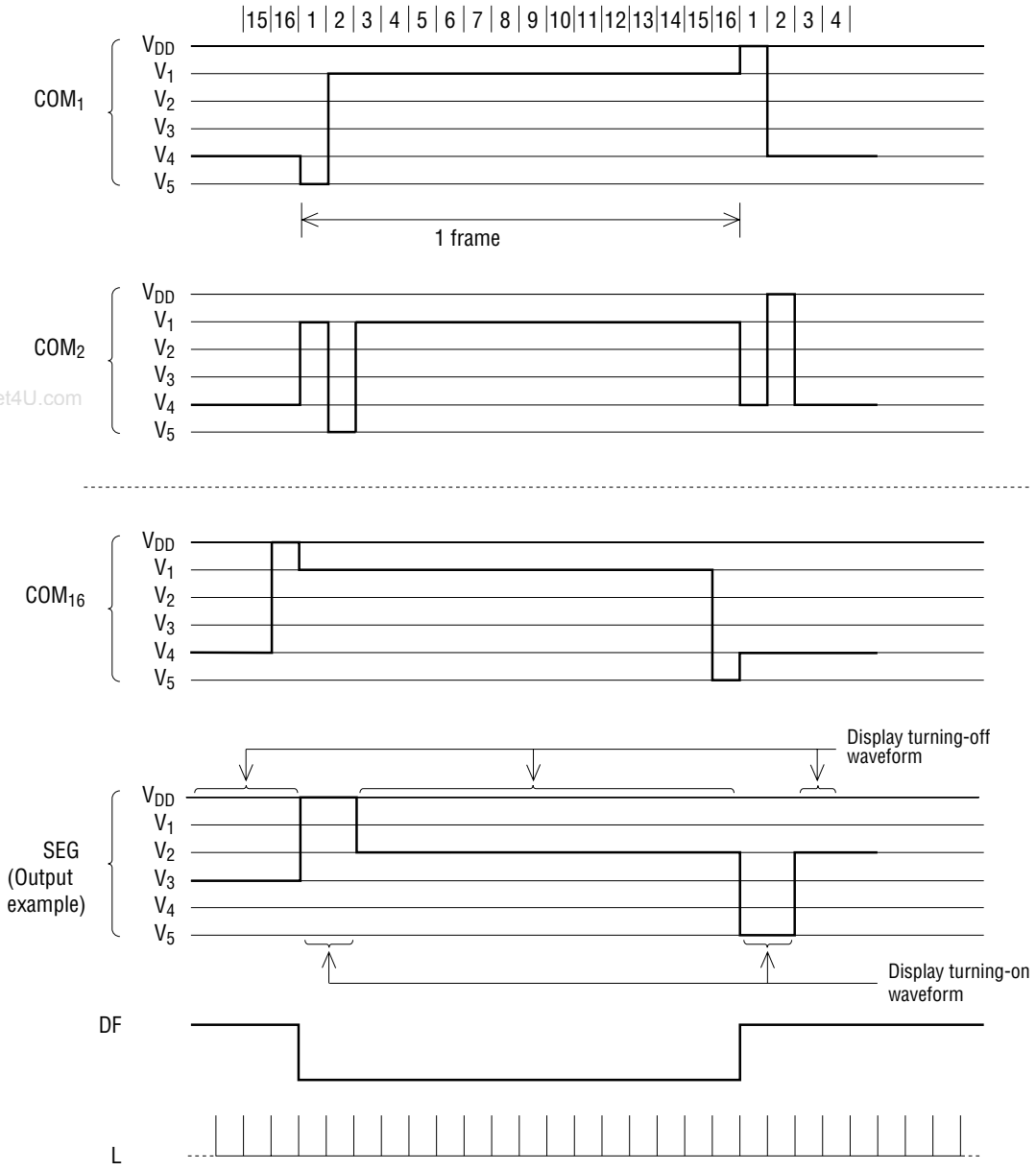
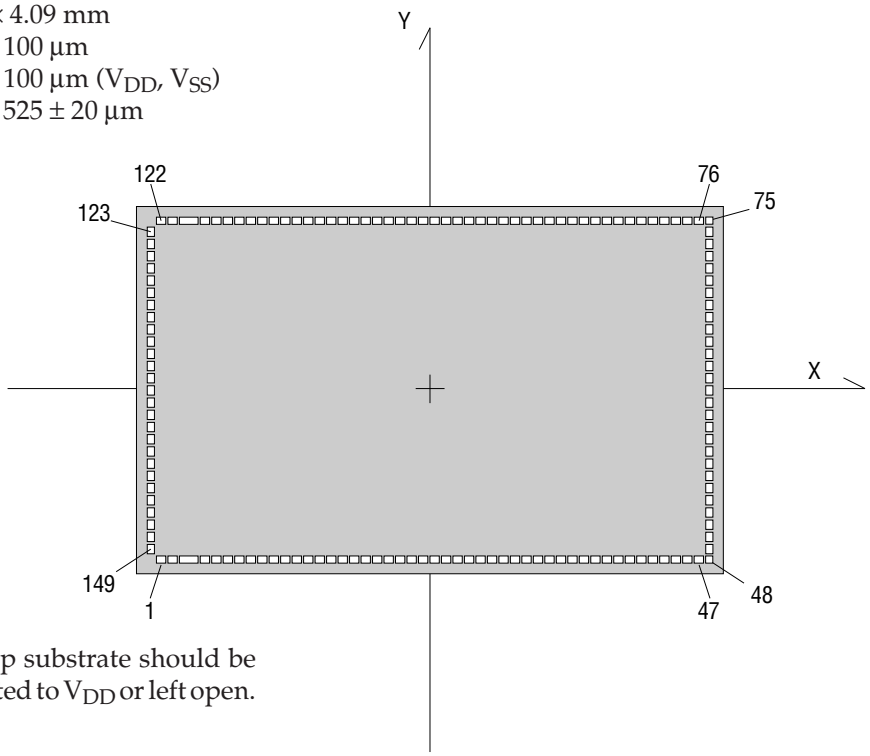


Figure 12 LCD driving waveforms at 1/16 duty

PAD CONFIGURATION

Pad Layout

Chip Size : 7.12 × 4.09 mm
Pad Size : 100 × 100 µm
(PV Hole) 210 × 100 µm (V_{DD}, V_{SS})
Chip Thickness : 525 ± 20 µm



Note : The chip substrate should be connected to V_{DD} or left open.

Pad Coordinates

Pad	Symbol	X (µm)	Y (µm)
1	T_2	–3275	–1900
2	T_3	–3135	–1900
3	V_{SS}	–2940	–1900
4	COM1	–2745	–1900
5	COM2	–2605	–1900
6	COM3	–2465	–1900
7	COM4	–2325	–1900
8	COM5	–2185	–1900
9	COM6	–2045	–1900
10	COM7	–1905	–1900
11	COM8	–1765	–1900
12	COM9	–1625	–1900
13	COM10	–1485	–1900
14	COM11	–1345	–1900
15	COM12	–1205	–1900
16	COM13	–1065	–1900
17	COM14	–925	–1900
18	COM15	–785	–1900
19	COM16	–645	–1900
20	SEG100	–505	–1900

Pad	Symbol	X (µm)	Y (µm)
21	SEG99	–365	–1900
22	SEG98	–225	–1900
23	SEG97	–85	–1900
24	SEG96	55	–1900
25	SEG95	195	–1900
26	SEG94	335	–1900
27	SEG93	475	–1900
28	SEG92	615	–1900
29	SEG91	755	–1900
30	SEG90	895	–1900
31	SEG89	1035	–1900
32	SEG88	1175	–1900
33	SEG87	1315	–1900
34	SEG86	1455	–1900
35	SEG85	1595	–1900
36	SEG84	1735	–1900
37	SEG83	1875	–1900
38	SEG82	2015	–1900
39	SEG81	2155	–1900
40	SEG80	2295	–1900

Pad Coordinates (continued)

Pad	Symbol	X (µm)	Y (µm)
41	SEG79	2435	–1900
42	SEG78	2527	–1900
43	SEG77	2715	–1900
44	SEG76	2855	–1900
45	SEG75	2995	–1900
46	SEG74	3135	–1900
47	SEG73	3275	–1900
48	SEG72	3415	–1900
49	SEG71	3415	–1750
50	SEG70	3415	–1610
51	SEG69	3415	–1470
52	SEG68	3415	–1330
53	SEG67	3415	–1190
54	SEG66	3415	–1050
55	SEG65	3415	–910
56	SEG64	3415	–770
57	SEG63	3415	–630
58	SEG62	3415	–490
59	SEG61	3415	–350
60	SEG60	3415	–210
61	SEG59	3415	–70
62	SEG58	3415	70
63	SEG57	3415	210
64	SEG56	3415	350
65	SEG55	3415	490
66	SEG54	3415	630
67	SEG53	3415	770
68	SEG52	3415	910
69	SEG51	3415	1050
70	SEG50	3415	1190
71	SEG49	3415	1330
72	SEG48	3415	1470
73	SEG47	3415	1610
74	SEG46	3415	1750
75	SEG45	3415	1900
76	SEG44	3275	1900
77	SEG43	3135	1900
78	SEG42	2995	1900
79	SEG41	2855	1900
80	SEG40	2715	1900
81	SEG39	2575	1900
82	SEG38	2435	1900
83	SEG37	2295	1900
84	SEG36	2155	1900
85	SEG35	2015	1900

Pad	Symbol	X (µm)	Y (µm)
86	SEG34	1875	1900
87	SEG33	1735	1900
88	SEG32	1595	1900
89	SEG31	1455	1900
90	SEG30	1315	1900
91	SEG29	1175	1900
92	SEG28	1035	1900
93	SEG27	895	1900
94	SEG26	755	1900
95	SEG25	615	1900
96	SEG24	475	1900
97	SEG23	335	1900
98	SEG22	195	1900
99	SEG21	55	1900
100	SEG20	–85	1900
101	SEG19	–225	1900
102	SEG18	–365	1900
103	SEG17	–505	1900
104	SEG16	–645	1900
105	SEG15	–785	1900
106	SEG14	–925	1900
107	SEG13	–1065	1900
108	SEG12	–1205	1900
109	SEG11	–1345	1900
110	SEG10	–1485	1900
111	SEG9	–1625	1900
112	SEG8	–1765	1900
113	SEG7	–1905	1900
114	SEG6	–2045	1900
115	SEG5	–2185	1900
116	SEG4	–2325	1900
117	SEG3	–2465	1900
118	SEG2	–2605	1900
119	SEG1	–2745	1900
120	V_{DD}	–2940	1900
121	SHL0	–3135	1900
122	SHL1	–3275	1900
123	OSC1	–3415	1820
124	OSCR	–3415	1680
125	OSC2	–3415	1540
126	V_1	–3415	1400
127	V_2	–3415	1260
128	V_3'	–3415	1120
129	V_3	–3415	980
130	V_4	–3415	840

Pad Coordinates (continued)

Pad	Symbol	X (µm)	Y (µm)
131	V_5	–3415	700
132	V_5'	–3415	560
133	L	–3415	420
134	CP	–3415	280
135	DF	–3415	140
136	DO	–3415	0
137	RS0	–3415	–140
138	RS1	–3415	–280
139	R/W	–3415	–420
140	E	–3415	–560
141	DB0	–3415	–700
142	DB1	–3415	–840
143	DB2	–3415	–980
144	DB3	–3415	–1120
145	DB4	–3415	–1260
146	DB5	–3415	–1400
147	DB6	–3415	–1540
148	DB7	–3415	–1680
149	T_1	–3415	–1820

Pad	Symbol	X (µm)	Y (µm)