Freescale Semiconductor
Data Sheet: Product Preview

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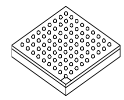
MSC8144



Quad Core Digital Signal Processor

- Four StarCore™ SC3400 DSP subsystems, each with an SC3400 DSP core, 16 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, memory management unit (MMU), extended programmable interrupt controller (EPIC), two general-purpose 32-bit timers, debug and profiling support, and low-power Wait and Stop processing modes.
- Chip-level arbitration and system (CLASS) that provides full fabric non-blocking arbitration between the processing elements and other initiators and the M2 memory, DDR SRAM controller, device configuration control and status registers, and other targets.
- 128 Kbyte L2 shared instruction cache.
- 512 Kbyte M2 memory for critical data and temporary data buffering.
- 10 Mbyte 128-b8t wide M3 memory.
- 96 Kbyte boot ROM.
- Three input clocks (shared, global, and differential).
- Four PLLs (system, core, global, and serial RapidIO).
- DDR controller with up to a 200 MHz clock (400 MHz data rate), 16/32 bit data bus, supporting up to 1 Gbyte in up to two banks and support for DDR1 and DDR2.
- DMA controller with 16 bidirectional channels with up to 1024 buffer descriptors, and programmable priority, buffer, and multiplexing configuration.
- Up to eight independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/μ-law conversion, up to 128 Mbps data rate for all channels, with glueless interface to E1 or T1 framers, and can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.
- QUICC Engine™ technology subsystem with dual RISC processors, 48 Kbyte multi-master RAM, 48 Kbyte instruction RAM, supporting three communication controllers with one ATM and two Gigabit Ethernet interfaces, to offload scheduling tasks from the DSP cores.
  - The two Ethernet controllers support 10/100/1000 Mbps operations via MII/RMII/SMII/RGMII/SGMII and the SGMII protocol using a 4-pin SerDes interface at 1000 Mbps data rate only.
  - The ATM controller supports UTOPIA level II 8/16 bits at 25/50 MHz in UTOPIA/POS mode with adaptation layer support AAL0, AAL2, and AAL5.
- PCI designed to comply with the PCI specification revision 2.2 at 33 MHz or 66 MHz with access to all PCI address spaces.
- Serial RapidIO® 1x/4x endpoint corresponds to Specification 1.2 of the RapidIO trade association, and supports read, write, messages, doorbells, and maintenance accesses in inbound mode, and messages and doorbells in outbound mode.
- I/O interrupt concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and the cores.
- UART that permits full-duplex operation with a bit rate of up to 6.25 Mbps.
- Serial peripheral interface (SPI).
- Four timer modules, each with four configurable16-bit timers.
- Four software watchdog timer (SWT) modules.
- Up to 32 general-purpose input/output (GPIO) ports, 16 of which can be configured as maskable interrupt inputs.
- I^{2}C interface that allows booting from EEPROM devices.
- Eight programmable hardware semaphores.
- Thirty two virtual maskable interrupts and one virtual $\overline{\text{NMI}}$ that can be generated by a simple write access.
- Optional booting via serial RapidIO port, PCI, I^{2}C, SPI, or Ethernet interfaces.

Note: This document supports mask set M31H.

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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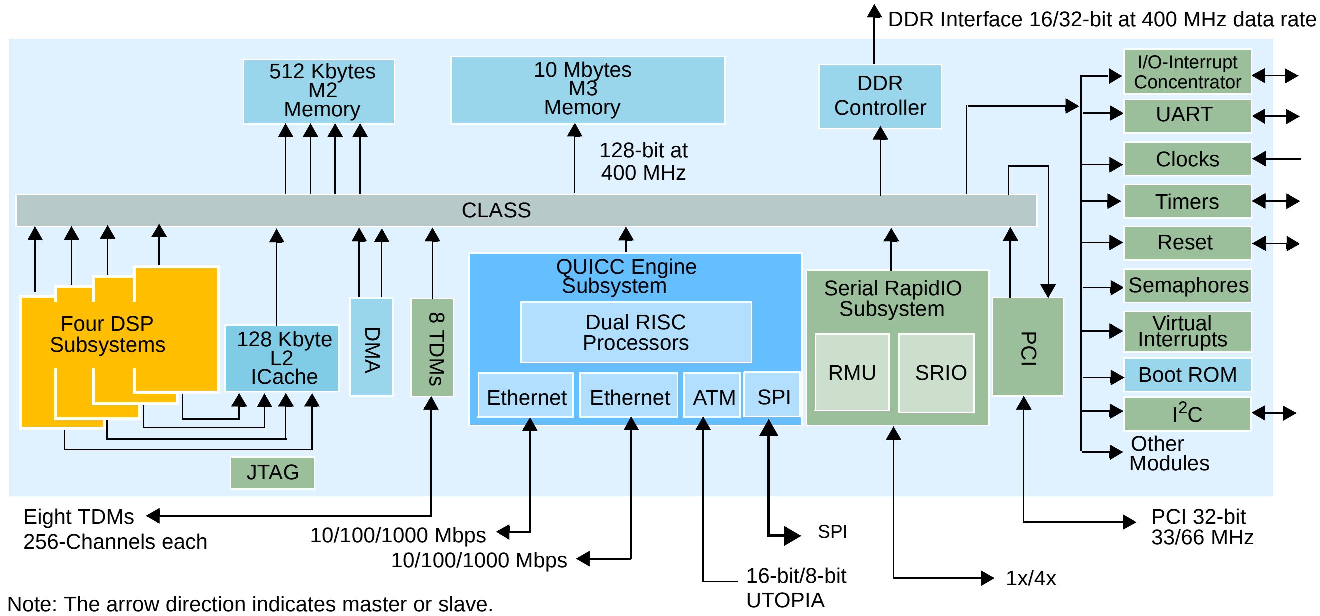


Figure 1. MSC8144 Block Diagram

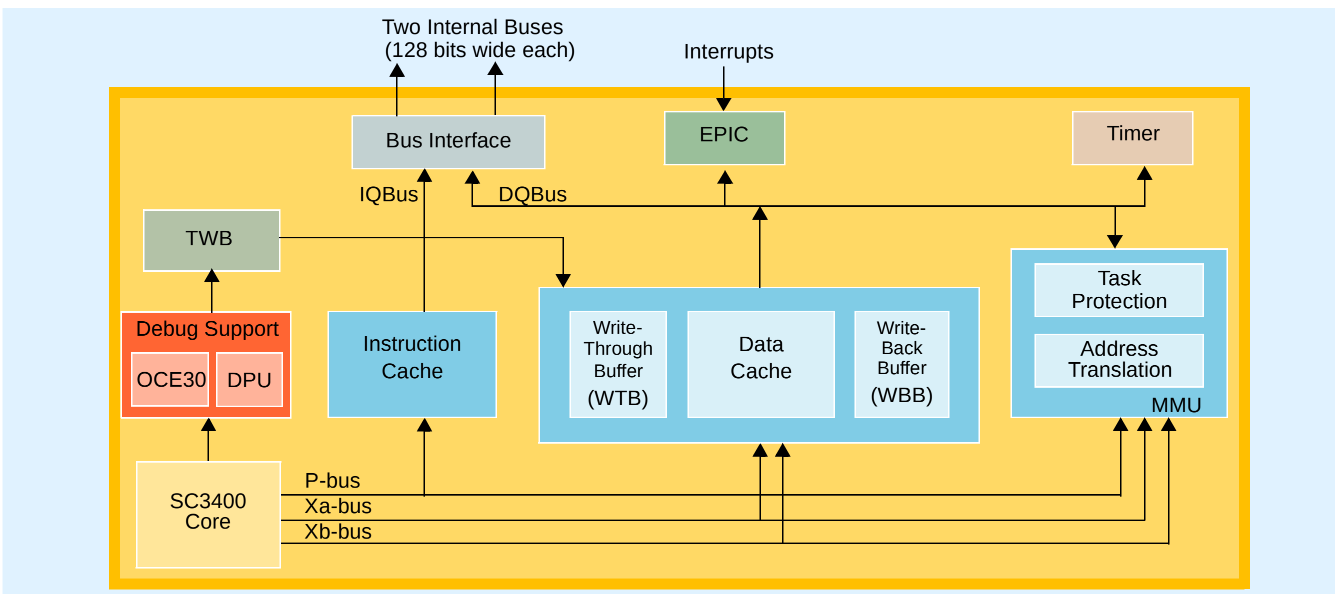


Figure 2. StarCore SC3400 DSP Core Subsystem Block Diagram

1 Pin Assignments and Reset States

This section includes diagrams of the MSC8144 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

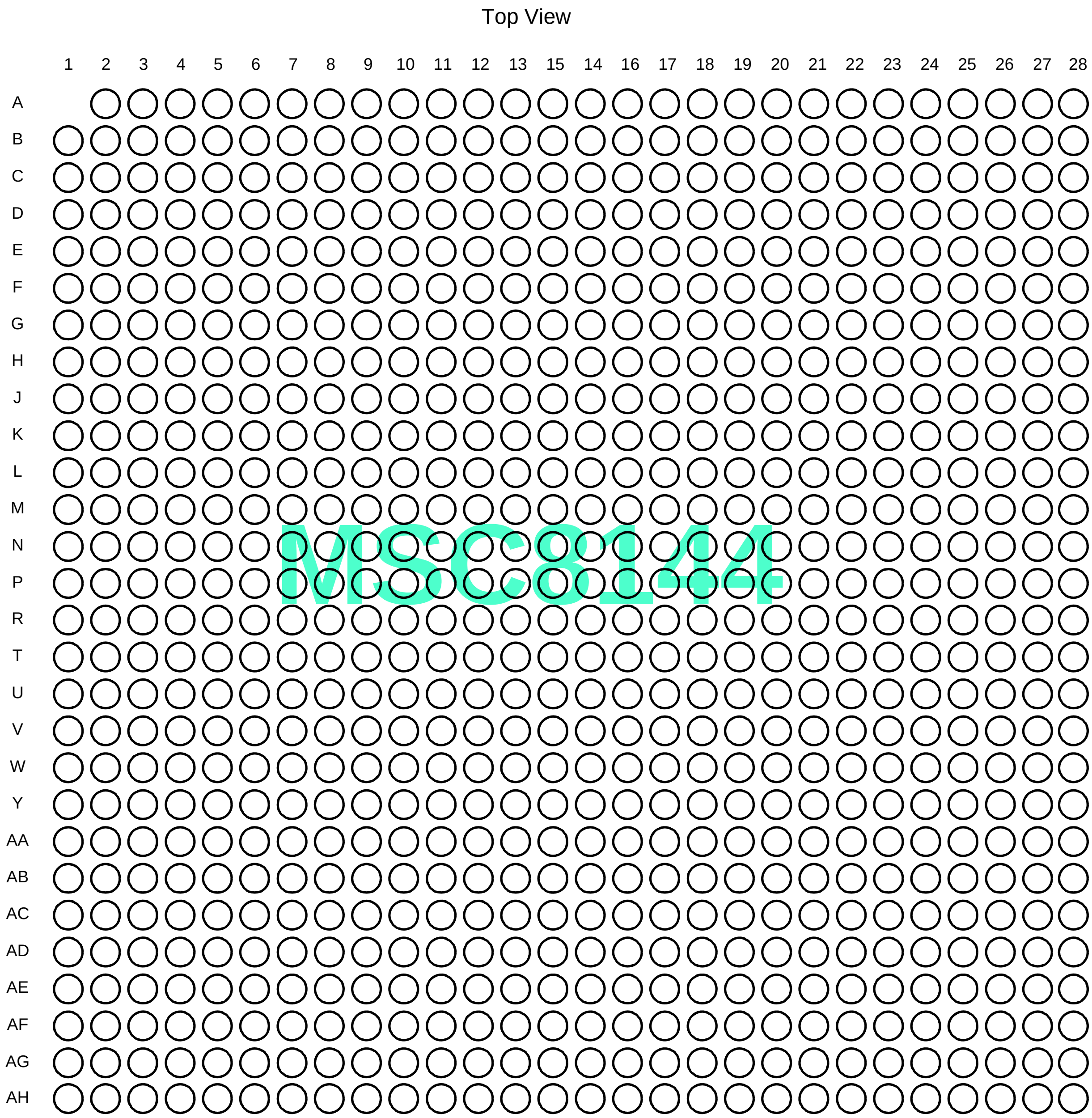


Figure 3. MSC8144 FC-PBGA Package, Top View

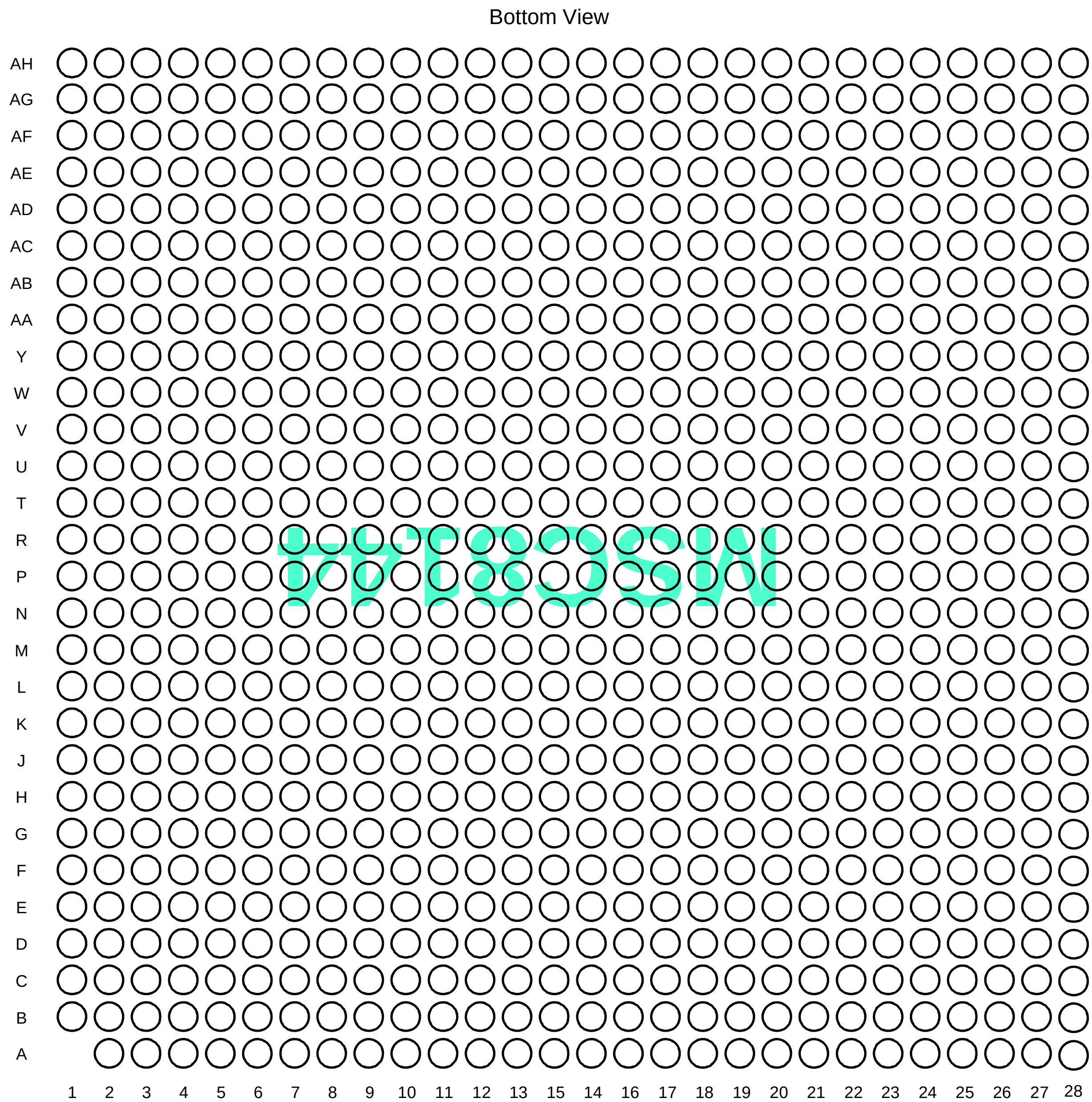


Figure 4. MSC8144 FC-PBGA Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/PCI_CBE0		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	SRIO_REF_CLK										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	MDQS3										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/PCI_CBE1		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/PCI_CBE2		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
B10	Reserved[1]										—
B11	Reserved[1]										—
B12	SRIO_RXD0										V_{DDSXC}
B13	GND_{SXC}										GND_{SXC}
B14	SRIO_RXD1										V_{DDSXC}
B15	GND_{SXC}										GND_{SXC}
B16	SRIO_REF_CLK										V_{DDSXC}
B17	Reserved[1]										—
B18	V_{DDSXC}										V_{DDSXC}
B19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B20	GND_{SXC}										GND_{SXC}
B21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B22	GND_{SXC}										GND_{SXC}
B23	GND_{SXP}										GND_{SXP}
B24	MDQ27										V_{DDDDR}
B25	V_{DDDDR}										V_{DDDDR}
B26	GND										GND
B27	V_{DDDDR}										V_{DDDDR}
B28	MDQS3										V_{DDDDR}
C1	Reserved[1]										—
C2	GE2_RX_CLK/PCI_AD29		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C3	V_{DDGE2}										V_{DDGE2}
C4	TDM7RSYN/GE2_TD2/ PCI_AD2/UTP_TER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C5	TDM7RCLK/GE2_RD2/ PCI_AD0/UTP_RVL		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C6	V_{DDGE2}										V_{DDGE2}
C7	GE2_RD0/PCI_AD27		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C8	Reserved[1]										—
C9	Reserved[1]										—
C10	Reserved[1]										—
C11	Reserved[1]										—
C12	V_{DDSXP}										V_{DDSXP}
C13	SRIO_TXD0										V_{DDSXP}
C14	V_{DDSXP}										V_{DDSXP}
C15	SRIO_TXD1										V_{DDSXP}
C16	GND_{SXC}										GND_{SXC}
C17	GND_{RIOPLL}										GND_{RIOPLL}
C18	Reserved[1]										—
C19	V_{DDSXP}										V_{DDSXP}
C20	SRIO_TXD2/GE1_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
C21	V_{DDSXP}										V_{DDSXP}
C22	$\overline{\text{SRIO\_TXD3/GE2\_SGMII\_TX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
C23	V_{DDSXP}										V_{DDSXP}
C24	MDQ26										V_{DDDDR}
C25	MDQ25										V_{DDDDR}
C26	MDM3										V_{DDDDR}
C27	GND										GND
C28	MDQ24										V_{DDDDR}
D1	Reserved[1]										—
D2	GE2_RD1/PCI_AD28		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/PCI_AD3/UTP_TMD		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D5	TDM7RDAT/GE2_RD3/PCI_AD1/UTP_STA		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D6	GE1_RD0/UTP_RD2/$\overline{\text{PCI\_CBE2}}$		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
D7	TDM7TCLK/GE2_TCK/PCI_IDS/UTP_RER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D8	Reserved[1]										—
D9	Reserved[1]										—
D10	Reserved[1]										—
D11	Reserved[1]										—
D12	GND_{SXP}										GND_{SXP}
D13	SRIO_TXD0										V_{DDSXP}
D14	GND_{SXP}										GND_{SXP}
D15	SRIO_TXD1										V_{DDSXP}
D16	V_{DDSXC}										V_{DDSXC}
D17	Reserved[1]										—
D18	Reserved[1]										—
D19	GND_{SXP}										GND_{SXP}
D20	SRIO_TXD2/GE1_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D21	GND_{SXP}										GND_{SXP}
D22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D23	GND_{SXP}										GND_{SXP}
D24	MDQ23										V_{DDDDR}
D25	V_{DDDDR}										V_{DDDDR}
D26	MDQ22										V_{DDDDR}
D27	MDQ21										V_{DDDDR}
D28	$\overline{\text{MDQS2}}$										V_{DDDDR}
E1	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E6	V_{DDGE1}										V_{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E8	Reserved[1]										—
E9	Reserved[1]										—
E10	GND										GND
E11	V_{DD}										V_{DD}
E12	GND										GND
E13	V_{DD}										V_{DD}
E14	GND										GND
E15	V_{DD}										V_{DD}
E16	GND										GND
E17	V_{DD}										V_{DD}
E18	GND										GND
E19	V_{DD}										V_{DD}
E20	GND										GND
E21	V_{DD}										V_{DD}
E22	GND										GND
E23	V_{DDDDR}										V_{DDDDR}
E24	MDQ20										V_{DDDDR}
E25	GND										GND
E26	V_{DDDDR}										V_{DDDDR}
E27	GND										GND
E28	MDQS2										V_{DDDDR}
F1	Reserved[1]										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F3	V_{DDGE1}										V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F8	V_{DDGE1}										V_{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
F10	V_{DD}										V_{DD}
F11	GND										GND
F12	V_{DD}										V_{DD}
F13	GND										GND
F14	V_{DD}										V_{DD}
F15	GND										GND
F16	V_{DD}										V_{DD}
F17	GND										GND
F18	V_{DD}										V_{DD}
F19	GND										GND
F20	V_{DD}										V_{DD}
F21	Reserved[1]										—
F22	V_{DDDDR}										V_{DDDDR}
F23	GND										GND
F24	MDQ19										V_{DDDDR}
F25	MDQ18										V_{DDDDR}
F26	MDM2										V_{DDDDR}
F27	MDQ17										V_{DDDDR}
F28	MDQ16										V_{DDDDR}
G1	Reserved[1]										—
G2	$\overline{\text{SRESET}}$[4]										V_{DDIO}
G3	GND										GND
G4	$\overline{\text{PORESET}}$[4]										V_{DDIO}
G5	GE1_COL/UTP_RD1		UTOPIA	Ethernet 1		UTOPIA			Ethernet 1	UTOPIA	V_{DDIO}
G6	GE1_TD2/UTP_TD4/ PCI_AD29		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
G7	GE1_RX_DV/UTP_RD7		UTOPIA	Ethernet 1		UTOPIA			Ethernet 1	UTOPIA	V_{DDGE1}
G8	GE1_TX_ER/UTP_TD7/ $\overline{\text{PCI\_CBE1}}$		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
G9	V_{DD}										V_{DD}
G10	GND										GND
G11	V_{DD}										V_{DD}
G12	GND										GND
G13	V_{DD}										V_{DD}
G14	GND										GND
G15	V_{DD}										V_{DD}
G16	GND										GND
G17	V_{DD}										V_{DD}
G18	GND										GND
G19	V_{DD}										V_{DD}
G20	GND										GND
G21	Reserved[1]	—									—
G22	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G23	MBA1										V_{DDDDR}
G24	MA3										V_{DDDDR}
G25	MA8										V_{DDDDR}
G26	V_{DDDDR}										V_{DDDDR}
G27	GND										GND
G28	$\overline{MCK0}$										V_{DDDDR}
H1	Reserved[1]										—
H2	CLKIN										V_{DDIO}
H3	$\overline{HRESET}$										V_{DDIO}
H4	PCI_CLK_IN										V_{DDIO}
H5	$\overline{NMI}$										V_{DDIO}
H6	URXD/GPIO14/$\overline{IRQ8}$/$\overline{RC\_LDF}$[3, 6]	$\overline{RC\_LDF}$	UART/GPIO/IRQ								V_{DDIO}
H7	GE1_RX_ER/PCI_AD6/GPIO25/$\overline{IRQ15}$[3, 6]		GPIO/IRQ	Ethernet 1	PCI			GPIO/IRQ	Ethernet 1		V_{DDIO}
H8	GE1_CRS/PCI_AD5		PCI	Ethernet 1	PCI				Ethernet 1		V_{DDIO}
H9	GND										GND
H10	V_{DD}										V_{DD}
H11	GND										GND
H12	V_{DD}										V_{DD}
H13	GND										GND
H14	V_{DD}										V_{DD}
H15	V_{DD}										V_{DD}
H16	V_{DD}										V_{DD}
H17	GND										GND
H18	V_{DD}										V_{DD}
H19	GND										GND
H20	V_{DD}										V_{DD}
H21	V_{DD}										V_{DD}
H22	V_{DDDDR}										V_{DDDDR}
H23	MBA0										V_{DDDDR}
H24	MA15										V_{DDDDR}
H25	V_{DDDDR}										V_{DDDDR}
H26	MA9										V_{DDDDR}
H27	MA7										V_{DDDDR}
H28	MCK0										V_{DDDDR}
J1	Reserved[1]										—
J2	GND										GND
J3	V_{DDIO}										V_{DDIO}
J4	STOP_BS										V_{DDIO}
J5	$\overline{NMI\_OUT}$[4]										V_{DDIO}
J6	$\overline{INT\_OUT}$[4]										V_{DDIO}
J7	SDA/GPIO27[3, 4, 6]		I2C/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
K23	MBA2										V_{DDDDR}
K24	MA10										V_{DDDDR}
K25	MA12										V_{DDDDR}
K26	MA14										V_{DDDDR}
K27	MA4										V_{DDDDR}
K28	MV_{REF}										V_{DDDDR}
L1	Reserved[1]										—
L2	CLKOUT										V_{DDIO}
L3	TMR1/UTP_IR/$\overline{\text{PCI\_CBE3}}$/GPIO17[3, 6]		UTOPIA		TMR/ GPIO	UTOPIA	PCI	UTOPIA			V_{DDIO}
L4	TMR4/PCI_PAR/GPIO20[3, 6]/ UTP_REOP		TIMER/GPIO				PCI	TIMER/GPIO			V_{DDIO}
L5	GND										GND
L6	TMR2/$\overline{\text{PCI\_FRAME}}$/GPIO18[3, 6]		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
L7	SCL/GPIO26[3, 4, 6]		I^2C/GPIO								V_{DDIO}
L8	UTXD/GPIO15/$\overline{\text{IRQ9}}$[3, 6]		UART/GPIO/IRQ								V_{DDIO}
L9	GND										GND
L10	V_{DD}										V_{DD}
L11	GND										GND
L12	V_{DD}										V_{DD}
L13	GND										GND
L14	V_{DD}										V_{DD}
L15	Reserved[1]										GND
L16	V_{DD}										V_{DD}
L17	GND										GND
L18	V_{DD}										V_{DD}
L19	GND										GND
L20	V_{DD}										V_{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V_{DDDDR}
L24	MA1										V_{DDDDR}
L25	V_{DDDDR}										V_{DDDDR}
L26	GND										GND
L27	V_{DDDDR}										V_{DDDDR}
L28	$\overline{\text{MCK1}}$										V_{DDDDR}
M1	Reserved[1]										—
M2	$\overline{\text{TRST}}$										V_{DDIO}
M3	EE0										V_{DDIO}
M4	EE1										V_{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA		PCI	UTOPIA					V_{DDIO}
M6	UTP_RADDR0/PCI_AD7		UTOPIA		PCI	UTOPIA					V_{DDIO}
M7	UTP_TD8/PCI_AD30		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
M8	V_{DDIO}										V_{DDIO}
M9	V_{DD}										V_{DD}
M10	GND										GND
M11	V_{DD}										V_{DD}
M12	GND										GND
M13	V_{DD}										V_{DD}
M14	GND										GND
M15	V_{DD}										V_{DD}
M16	GND										GND
M17	V_{DD}										V_{DD}
M18	GND										GND
M19	V_{DD}										V_{DD}
M20	GND										GND
M21	V_{DD}										V_{DD}
M22	V_{DDDDR}										V_{DDDDR}
M23	$\overline{MCS1}$										V_{DDDDR}
M24	MA13										V_{DDDDR}
M25	MA2										V_{DDDDR}
M26	MA0										V_{DDDDR}
M27	GND										GND
M28	MCK1										V_{DDDDR}
N1	Reserved[1]										—
N2	V_{DDIO}										V_{DDIO}
N3	TMS										V_{DDIO}
N4	UTP_RD10/PCI_AD14[5]		UTOPIA		PCI	UTOPIA					V_{DDIO}
N5	V_{DDIO}		Power								V_{DDIO}
N6	UTP_RADDR1/PCI_AD8		UTOPIA		PCI	UTOPIA					V_{DDIO}
N7	UTP_TD9/PCI_AD31		UTOPIA		PCI	UTOPIA					V_{DDIO}
N8	TMR3/$\overline{PCI\_IRDY}$/GPIO19[3,6]/ UTP_TEOP		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
N9	GND										GND
N10	V_{DDM3}										V_{DDM3}
N11	V_{DD}										V_{DD}
N12	V_{DDM3}										V_{DDM3}
N13	V_{DD}										V_{DD}
N14	V_{DDM3}										V_{DDM3}
N15	V_{DD}										V_{DD}
N16	V_{DDM3}										V_{DDM3}
N17	V_{DD}										V_{DD}
N18	V_{DDM3}										V_{DDM3}
N19	V_{DD}										V_{DD}
N20	V_{DDM3}										V_{DDM3}
N21	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
N22	GND										GND
N23	MODT1										V_{DDDDR}
N24	MCKE0										V_{DDDDR}
N25	V_{DDDDR}										V_{DDDDR}
N26	MA5										V_{DDDDR}
N27	MA6										V_{DDDDR}
N28	MA11										V_{DDDDR}
P1	Reserved[1]										—
P2	TDI[5]										V_{DDIO}
P3	UTP_RD11/PCI_AD15		UTOPIA		PCI	UTOPIA					V_{DDIO}
P4	GND										GND
P5	UTP_RADDR3/PCI_AD10		UTOPIA		PCI	UTOPIA					V_{DDIO}
P6	UTP_RADDR2/PCI_AD9		UTOPIA		PCI	UTOPIA					V_{DDIO}
P7	$\overline{PCI\_GNT}$/GPIO29/$\overline{IRQ7}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P8	$\overline{PCI\_STOP}$/GPIO30/$\overline{IRQ2}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P9	GND										GND
P10	GND										GND
P11	V_{DDM3}										V_{DDM3}
P12	GND										GND
P13	V_{DDM3}										V_{DDM3}
P14	GND										GND
P15	V_{DDM3}										V_{DDM3}
P16	GND										GND
P17	V_{DDM3}										V_{DDM3}
P18	GND										GND
P19	V_{DDM3}										V_{DDM3}
P20	GND										GND
P21	GND										GND
P22	V_{DDDDR}										V_{DDDDR}
P23	$\overline{MCS0}$										V_{DDDDR}
P24	$\overline{MRAS}$										V_{DDDDR}
P25	GND										GND
P26	V_{DDDDR}										V_{DDDDR}
P27	GND										GND
P28	$\overline{MCK2}$										V_{DDDDR}
R1	Reserved[1]										—
R2	TCK										V_{DDIO}
R3	TDO										V_{DDIO}
R4	UTP_RD12/PCI_AD16		UTOPIA		PCI	UTOPIA					V_{DDIO}
R5	UTP_RCLAV_PDRPA/ PCI_AD12		UTOPIA		PCI	UTOPIA					V_{DDIO}
R6	UTP_RADDR4/PCI_AD11		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
R7	V_{DDIO}										V_{DDIO}
R8	$\overline{\text{PCI\_REQ}}$		PCI								V_{DDIO}
R9	GND										GND
R10	GND										GND
R11	GND										GND
R12	GND										GND
R13	GND										GND
R14	GND										GND
R15	GND										GND
R16	GND										GND
R17	GND										GND
R18	GND										GND
R19	GND										GND
R20	GND										GND
R21	GND										GND
R22	GND										GND
R23	MODT0										V_{DDDDR}
R24	MDIC1										V_{DDDDR}
R25	MDIC0										V_{DDDDR}
R26	$\overline{\text{MCAS}}$										V_{DDDDR}
R27	$\overline{\text{MWE}}$										V_{DDDDR}
R28	MCK2										V_{DDDDR}
T1	Reserved[1]										—
T2	UTP_RPRTY/PCI_AD21		UTOPIA		PCI	UTOPIA					V_{DDIO}
T3	UTP_RD13/PCI_AD17		UTOPIA		PCI	UTOPIA					V_{DDIO}
T4	V_{DDIO}										V_{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA		PCI	UTOPIA					V_{DDIO}
T6	UTP_RD15/PCI_AD19		UTOPIA		PCI	UTOPIA					V_{DDIO}
T7	$\overline{\text{PCI\_TRDY}}$		PCI								V_{DDIO}
T8	$\overline{\text{PCI\_DEVSEL}}$/GPIO31/ $\overline{\text{IRQ3}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
T9	GND										GND
T10	GND										GND
T11	GND										GND
T12	GND										GND
T13	GND										GND
T14	GND										GND
T15	GND										GND
T16	GND										GND
T17	GND										GND
T18	GND										GND
T19	GND										GND
T20	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2] 0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	Ref. Supply
T21	GND										GND
T22	V_{DDDDR}										V_{DDDDR}
T23	GND										GND
T24	V_{DDDDR}										V_{DDDDR}
T25	GND										GND
T26	V_{DDDDR}										V_{DDDDR}
T27	GND										GND
T28	V_{DDDDR}										V_{DDDDR}
U1	Reserved[1]										—
U2	UTP_TCLK/PCI_AD29		UTOPIA		PCI	UTOPIA					V_{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA		PCI	UTOPIA					V_{DDIO}
U4	UTP_TADDR2		UTOPIA								V_{DDIO}
U5	GND										GND
U6	$\overline{\text{UTP\_REN}}$/PCI_AD20		UTOPIA		PCI	UTOPIA					V_{DDIO}
U7	PCI_AD26		PCI								V_{DDIO}
U8	PCI_AD25		PCI								V_{DDIO}
U9	Reserved[1]										V_{DDIO}
U10	V_{DDM3}										V_{DDM3}
U11	GND										GND
U12	V_{DDM3}										V_{DDM3}
U13	GND										GND
U14	V_{DDM3}										V_{DDM3}
U15	GND										GND
U16	V_{DDM3}										V_{DDM3}
U17	GND										GND
U18	V_{DDM3}										V_{DDM3}
U19	GND										GND
U20	V_{DDM3}										V_{DDM3}
U21	GND										GND
U22	GND										GND
U23	MDQ7										V_{DDDDR}
U24	MDQ3										V_{DDDDR}
U25	MDQ4										V_{DDDDR}
U26	MDQ5										V_{DDDDR}
U27	MDQ1										V_{DDDDR}
U28	MDQ0										V_{DDDDR}
V1	Reserved[1]										—
V2	UTP_TD10/$\overline{\text{PCI\_CBE0}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
V3	UTP_TADDR3		UTOPIA								V_{DDIO}
V4	UTP_TD1/$\overline{\text{PCI\_PERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA		PCI	UTOPIA					V_{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA		PCI	UTOPIA					V_{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
V8	V_{DDIO}										V_{DDIO}
V9	Reserved[1]										V_{DDIO}
V10	GND										GND
V11	V_{DDM3}										V_{DDM3}
V12	GND										GND
V13	V_{DDM3}										V_{DDM3}
V14	GND										GND
V15	V_{DDM3}										V_{DDM3}
V16	GND										GND
V17	V_{DDM3}										V_{DDM3}
V18	GND										GND
V19	V_{DDM3}										V_{DDM3}
V20	GND										GND
V21	GND										GND
V22	V_{DDDDR}										V_{DDDDR}
V23	MDQ2										V_{DDDDR}
V24	V_{DDDDR}										V_{DDDDR}
V25	MDQ6										V_{DDDDR}
V26	GND										GND
V27	V_{DDDDR}										V_{DDDDR}
V28	MDQS0										V_{DDDDR}
W1	Reserved[1]										—
W2	UTP_TD12/$\overline{\text{PCI\_CBE2}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W3	UTP_TD11/$\overline{\text{PCI\_CBE1}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W4	V_{DDIO}										V_{DDIO}
W5	GND										GND
W6	UTP_TD15/$\overline{\text{PCI\_IRDY}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W7	UTP_TD0/$\overline{\text{PCI\_SERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
W8	UTP_RSOC/PCI_AD22		UTOPIA		PCI	UTOPIA					V_{DDIO}
W9	Reserved[1]										V_{DDIO}
W10	V_{DDM3}										V_{DDM3}
W11	GND										GND
W12	V_{25M3}										V_{25M3}
W13	GND										GND
W14	V_{DDM3}										V_{DDM3}
W15	V_{25M3}										V_{25M3}
W16	V_{DDM3}										V_{DDM3}
W17	GND										GND
W18	V_{25M3}										V_{25M3}
W19	GND										GND
W20	V_{DDM3}										V_{DDM3}
W21	GND										GND
W22	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
W23	MDQ10										V_{DDDDR}
W24	GND										GND
W25	MDQ11										V_{DDDDR}
W26	MDM0										V_{DDDDR}
W27	GND										GND
W28	$\overline{\text{MDQS0}}$										V_{DDDDR}
Y1	Reserved[1]										-
Y2	UTP_TD14/$\overline{\text{PCI\_FRAME}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
Y3	TDM5TSYN/PCI_AD18/ GPIO12[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
Y4	TDM5TCLK/PCI_AD16		TDM			PCI		TDM			V_{DDIO}
Y5	TDM4RCLK/PCI_AD7		TDM			PCI		TDM			V_{DDIO}
Y6	TDM4TSYN/PCI_AD12		TDM			PCI		TDM			V_{DDIO}
Y7	UTP_TPRTY/RC14	RC14	UTOPIA								V_{DDIO}
Y8	$\overline{\text{UTP\_TEN}}$/PCI_PAR		UTOPIA		PCI	UTOPIA					V_{DDIO}
Y9	Reserved[1]										V_{DDIO}
Y10	GND										GND
Y11	V_{DDM3}										V_{DDM3}
Y12	GND										GND
Y13	V_{DDM3}										V_{DDM3}
Y14	GND										GND
Y15	V_{DDM3}										V_{DDM3}
Y16	GND										GND
Y17	V_{DDM3}										V_{DDM3}
Y18	GND										GND
Y19	V_{DDM3}										V_{DDM3}
Y20	GND										GND
Y21	GND										GND
Y22	V_{DDDDR}										V_{DDDDR}
Y23	MDQ13										V_{DDDDR}
Y24	V_{DDDDR}										V_{DDDDR}
Y25	GND										GND
Y26	MDQ9										V_{DDDDR}
Y27	V_{DDDDR}										V_{DDDDR}
Y28	MDQ8										V_{DDDDR}
AA1	Reserved[1]										—
AA2	UTP_TD13/$\overline{\text{PCI\_CBE3}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
AA3	TDM5RSYN/PCI_AD15/ GPIO10[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA4	TDM5TD3, AT/PCI_AD17/ GPIO11[6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA5	TDM5RCLK/PCI_AD13/ GPIO28[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA6	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AA7	TDM4TCLK/PCI_AD10		TDM			PCI		TDM			V_{DDIO}
AA8	TDM4TDAT/PCI_AD11		TDM			PCI		TDM			V_{DDIO}
AA9	V_{DDIO}										V_{DDIO}
AA10	V_{DDM3}										V_{DDM3}
AA11	GND										GND
AA12	V_{DDM3}										V_{DDM3}
AA13	GND										GND
AA14	V_{DDM3}										V_{DDM3}
AA15	GND										GND
AA16	V_{DDM3}										V_{DDM3}
AA17	GND										GND
AA18	V_{DDM3}										V_{DDM3}
AA19	GND										GND
AA20	V_{DDM3}										V_{DDM3}
AA21	GND										GND
AA22	GND										GND
AA23	MDQ15										V_{DDDDR}
AA24	MDQ14										V_{DDDDR}
AA25	MDM1										V_{DDDDR}
AA26	MDQ12										V_{DDDDR}
AA27	$\overline{\text{MDQS1}}$										V_{DDDDR}
AA28	MDQS1										V_{DDDDR}
AB1	Reserved[1]										-
AB2	UTP_TSOC/RC15	RC15	UTOPIA								V_{DDIO}
AB3	V_{DDIO}										V_{DDIO}
AB4	TDM6RDAT/PCI_AD20/ GPIO5/$\overline{\text{IRQ11}}$[3, 6]		TDM/GPIO/ IRQ			PCI		TDM/GPIO/ IRQ			V_{DDIO}
AB5	TDM5RDAT/PCI_AD14/ GPIO9[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AB6	TDM6TSYN/PCI_AD24/ GPIO8/ $\overline{\text{IRQ14}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB7	TDM6RCLK/PCI_AD19/ GPIO4/$\overline{\text{IRQ10}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB8	TDM4RSYN/PCI_AD9		TDM			PCI		TDM			V_{DDIO}
AB9	TDM4RDAT/PCI_AD8		TDM			PCI		TDM			V_{DDIO}
AB10	GND										GND
AB11	V_{DDM3}										V_{DDM3}
AB12	GND										GND
AB13	V_{DDM3}										V_{DDM3}
AB14	GND										GND
AB15	V_{DDM3}										V_{DDM3}
AB16	GND										GND
AB17	V_{DDM3}										V_{DDM3}
AB18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AB19	V_{DDM3}										V_{DDM3}
AB20	GND										GND
AB21	GND										GND
AB22	V_{DDDDR}										V_{DDDDR}
AB23	MECC7										V_{DDDDR}
AB24	MECC1										V_{DDDDR}
AB25	MECC4										V_{DDDDR}
AB26	MECC5										V_{DDDDR}
AB27	MECC2										V_{DDDDR}
AB28	ECC_MDQS										V_{DDDDR}
AC1	Reserved[1]										—
AC2	UTP_RD9/RC13	RC13	UTOPIA								V_{DDIO}
AC3	UTP_RD8/RC12	RC12	UTOPIA								V_{DDIO}
AC4	TDM6TCLK/PCI_AD22		TDM			PCI		TDM			V_{DDIO}
AC5	TDM6RSYN/PCI_AD21/ GPIO6/ $\overline{IRQ12}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AC6	V_{DDIO}										V_{DDIO}
AC7	TDM3TSYN/RC11	RC11	TDM								V_{DDIO}
AC8	PCI_AD23/GPIO7/$\overline{IRQ13}$/ TDM6TDAT[3, 6]/UTP_RMOD		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ		UTOPIA	V_{DDIO}
AC9	TDM7TSYN/ PCI_AD4		TDM		PCI			reserved			V_{DDIO}
AC10	V_{DDM3IO}										V_{DDM3IO}
AC11	GND										GND
AC12	V_{DDM3}										V_{DDM3}
AC13	GND										GND
AC14	V_{DDM3}										V_{DDM3}
AC15	GND										GND
AC16	V_{DDM3}										V_{DDM3}
AC17	GND										GND
AC18	V_{DDM3}										V_{DDM3}
AC19	GND										GND
AC20	V_{DDM3IO}										V_{DDM3IO}
AC21	Reserved[1]										—
AC22	MECC6										V_{DDDDR}
AC23	MECC3										V_{DDDDR}
AC24	ECC_MDM										V_{DDDDR}
AC25	V_{DDDDR}										V_{DDDDR}
AC26	MECC0										V_{DDDDR}
AC27	V_{DDDDR}										V_{DDDDR}
AC28	$\overline{ECC\_MDQS}$										V_{DDDDR}
AD1	Reserved[1]										—
AD2	GPIO1[3, 6]		GPIO								V_{DDIO}
AD3	TMR0/GPIO13		TIMER/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AD4	GPIO2[3, 6]		GPIO								V_{DDIO}
AD5	GND										GND
AD6	TDM1TCLK		TDM								V_{DDIO}
AD7	TDM3TDAT/RC10	RC10	TDM								V_{DDIO}
AD8	TDM3RSYN/RC9	RC9	TDM								V_{DDIO}
AD9	TDM3RDAT/RC8	RC8	TDM								V_{DDIO}
AD10	GND										GND
AD11	V_{25M3}										V_{25M3}
AD12	GND										GND
AD13	V_{DDM3}										V_{DDM3}
AD14	GND										GND
AD15	V_{25M3}										V_{25M3}
AD16	GND										GND
AD17	V_{DDM3}										V_{DDM3}
AD18	GND										GND
AD19	V_{25M3}										V_{25M3}
AD20	GND										GND
AD21	Reserved[1]										—
AD22	V_{DDDDR}										V_{DDDDR}
AD23	GND										GND
AD24	V_{DDDDR}										V_{DDDDR}
AD25	GND										GND
AD26	V_{DDDDR}										V_{DDDDR}
AD27	GND										GND
AD28	V_{DDDDR}										V_{DDDDR}
AE1	Reserved[1]										—
AE2	GPIO0[3, 6]		GPIO								V_{DDIO}
AE3	GPIO3[3, 6]		GPIO								V_{DDIO}
AE4	TDM1RCLK		TDM								V_{DDIO}
AE5	TDM1TSYN/RC3	RC3	TDM								V_{DDIO}
AE6	TDM1TDAT/RC2	RC2	TDM								V_{DDIO}
AE7	TDM1RSYN/RC1	RC1	TDM								V_{DDIO}
AE8	TDM3RCLK/RC16	RC16	TDM								V_{DDIO}
AE9	TDM3TCLK		TDM								V_{DDIO}
AE10	TDM2TDAT/RC6	RC6	TDM								V_{DDIO}
AE11	GPIO21/$\overline{\text{IRQ1}}$[3. 6]		GPIO/IRQ/SPI_SCK								V_{DDIO}
AE12	GND										GND
AE13	Reserved[1]										—
AE14	GND										GND
AE15	Reserved[1]										—
AE16	Reserved[1]										—
AE17	Reserved[1]										—
AE18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AE19	GND										GND
AE20	V_{DDM3IO}										V_{DDM3IO}
AE21	Reserved[1]										—
AE22	GND										GND
AE23	GND										GND
AE24	GND										GND
AE25	V_{DDDDR}										V_{DDDDR}
AE26	GND										GND
AE27	V_{DDDDR}										V_{DDDDR}
AE28	GND										GND
AF1	Reserved[1]										—
AF2	V_{DDIO}										V_{DDIO}
AF3	GND										GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM								V_{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM								V_{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM								V_{DDIO}
AF7	V_{DDIO}										V_{DDIO}
AF8	GND										GND
AF9	TDM2RDAT/RC4	RC4	TDM								V_{DDIO}
AF10	TDM2TCLK		TDM								V_{DDIO}
AF11	GPIO22/$\overline{IRQ4}$[3, 6]		GPIO/IRQ/SPI_MOSI								V_{DDIO}
AF12	GND										GND
AF13	GND										GND
AF14	V_{DDM3IO}										V_{DDM3IO}
AF15	GND										GND
AF16	GND										GND
AF17	Reserved[1]										—
AF18	V_{DDM3IO}										V_{DDM3IO}
AF19	GND										GND
AF20	Reserved[1]										—
AF21	Reserved[1]										—
AF22	$\overline{M3\_RESET}$										V_{DDM3IO}
AF23	GND										GND
AF24	V_{DDDDR}										V_{DDDDR}
AF25	GND										GND
AF26	V_{DDDDR}										V_{DDDDR}
AF27	GND										GND
AF28	V_{DDDDR}										V_{DDDDR}
AG1	Reserved[1]										—
AG2	GPIO16/$\overline{IRQ0}$[3, 6]		GPIO/IRQ								V_{DDIO}
AG3	TDM0TCLK		TDM								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AG4	TDM0RSYN/RCW_SRC0	RCW_ SRC0	TDM								V_{DDIO}
AG5	TDM0RCLK		TDM								V_{DDIO}
AG6	TDM0TDAT/RCW_SRC1	RCW_ SRC1	TDM								V_{DDIO}
AG7	TDM2TSYN/RC7	RC7	TDM								V_{DDIO}
AG8	TDM2RCLK		TDM								V_{DDIO}
AG9	TDM2RSYN/RC5	RC5	TDM								V_{DDIO}
AG10	GPIO24/$\overline{\text{IRQ6}}$[3, 6]		GPIO/IRQ/$\overline{\text{SPI\_SL}}$								V_{DDIO}
AG11	GPIO23/$\overline{\text{IRQ5}}$[3, 6]		GPIO/IRQ/SPI_MISO								V_{DDIO}
AG12	Reserved[1]										—
AG13	GND										GND
AG14	GND										GND
AG15	GND										GND
AG16	GND										GND
AG17	Reserved[1]										—
AG18	Reserved[1]										—
AG19	GND										GND
AG20	GND										GND
AG21	V_{DDM3IO}										V_{DDM3IO}
AG22	GND										GND
AG23	GND										GND
AG24	GND										GND
AG25	V_{DDDDR}										V_{DDDDR}
AG26	GND										GND
AG27	V_{DDDDR}										V_{DDDDR}
AG28	GND										GND
AH1	Reserved[1]										—
AH2	Reserved[1]										—
AH3	Reserved[1]										—
AH4	Reserved[1]										—
AH5	Reserved[1]										—
AH6	Reserved[1]										—
AH7	Reserved[1]										—
AH8	Reserved[1]										—
AH9	Reserved[1]										—
AH10	Reserved[1]										—
AH11	Reserved[1]										—
AH12	Reserved[1]										—
AH13	Reserved[1]										—
AH14	Reserved[1]										—
AH15	Reserved[1]										—
AH16	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AH17	Reserved[1]										—
AH18	Reserved[1]										—
AH19	Reserved[1]										—
AH20	Reserved[1]										—
AH21	Reserved[1]										—
AH22	Reserved[1]										—
AH23	Reserved[1]										—
AH24	Reserved[1]										—
AH25	Reserved[1]										—
AH26	Reserved[1]										—
AH27	Reserved[1]										—
AH28	Reserved[1]										—

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device.
2. For signals with same functionality in all modes the appropriate cells are empty.
3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23,** *GPIO* in the *MSC8144 Reference Manual*.
4. Open-drain signal.
5. Internal 20 KΩ pull-up resistor.
6. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See **Chapter 23**, *GPIO* of the *MSC8144 Reference Manual* for configuration details.

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8144 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8144.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{dd}	–0.3 to 1.1	V
PLL supply voltage	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1	V
M3 memory Internal voltage	V_{DDM3}	–0.3 to 1.32	V
DDR memory supply voltage • DDR mode • DDR2 mode	V_{DDDDR}	 –0.3 to 2.75 –0.3 to 1.98	 V V
DDR reference voltage	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage	V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
Ethernet 1 I/O voltage	V_{DDGE1}	–0.3 to 3.465	V
Input Ethernet 1 I/O voltage	V_{INGE1}	–0.3 to V_{DDGE1} + 0.3	V
Ethernet 2 I/O voltage	V_{DDGE2}	–0.3 to 3.465	V
Input Ethernet 2I/O voltage	V_{INGE2}	–0.3 to V_{DDGE2} + 0.3	V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	–0.3 to 3.465	V
Input I/O voltage	V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
M3 memory I/O and M3 memory charge pump voltage	V_{DDM3IO} V_{25M3}	–0.3 to 2.75	V
Input M3 memory I/O voltage	V_{INM3IO}	–0.3 to V_{DDM3IO} + 0.3	V
Rapid I/O C voltage	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O P voltage	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	–0.3 to 1.21	V
Operating temperature	T_J	–40 to 105	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature (T_J).
4. PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see **Figure 46**)

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage	V_{DD}	0.97	1.0	1.05	V
PLL supply voltage	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	0.97	1.0	1.05	V
M3 memory Internal voltage	V_{DDM3}	1.14	1.2	1.26	V
DDR memory supply voltage • DDR mode • DDR2 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 2.375 1.71 $0.49 \times V_{DDDDR}$	 2.5 1.8 $0.5 \times V_{DDDDR}$	 2.625 1.89 $0.51 \times V_{DDDDR}$	 V V V
Ethernet 1 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE1}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
Ethernet 2 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE2}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	3.135	3.3	3.465	V
M3 memory I/O and M3 charge pump voltage	V_{DDM3IO} V_{25M3}	2.375	2.5	2.625	V
Rapid I/O C voltage	V_{DDSXC}	0.95	1.0	1.05	V
Rapid I/O P voltage • Short run (haul) mode • Long run (haul) mode	V_{DDSXP}	 0.95 1.14	 1.0 1.2	 1.05 1.26	 V V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	0.95	1.0	1.05	V
Operating temperature range: • Standard • Extended	 T_J T_A T_J	 0 –40 —		 90 — 105	 °C °C °C
Note: PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see **Figure 46**).					

2.3 Default Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Impedance

Driver Type	Output Impedance (Ω)
DDR signal	18
DDR2 signal	18 35 (half strength mode)
PCI signals	25
Rapid I/O signals	100
Other signals	50

2.4 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8144 for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8144

Characteristic	Symbol	FC-PBGA 29 × 29 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	20	15	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	15	12	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	7		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.8		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature.

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

2.5 Power Characteristics

The estimated typical power dissipation for MSC8144 versus the core frequency is shown in **Table 6**.

Table 6. Power Dissipation

Extended Core Frequency	Core Frequency	Typical	Unit
266	400	TBD	W
	533	TBD	
	667	TBD	
	800	TBD	
333	500	TBD	W
	667	TBD	
	833	TBD	
	1000	TBD	
400	400	TBD	W
	600	TBD	
	800	TBD	
	1000	TBD	
500	500	TBD	W
	750	TBD	
	1000	TBD	

Note: Measured for 1.0 V core at 25°C junction temperature.

The typical power values were measured using an EFR code with the device running at a junction temperature of 25°C. No peripherals were enabled and the ICache was not enabled. The source code was optimized to use all the ALUs and AGUs and all four cores. It was created using CodeWarrior® 3.0. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Section 3** of this document.

At allowable voltage levels, **Table 7** lists the estimated power dissipation on the 1.0-V AV_{DD} supplies for the MSC8144 PLLs.

Table 7. MSC8144 PLLs Power Dissipation

PLL supply	Typical	Maximum	Unit
V_{DDPLL0}	TBD	10	mW
V_{DDPLL1}	TBD	10	mW
V_{DDPLL2}	TBD	10	mW
Note: Typical value is based on V_{DD} = 1.0 V, T_A = 70°C, T_J = 105°C.			

2.6 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144.

2.6.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144.

Note: DDR SDRAM uses V_{DDDDR}(typ) = 2.5 V and DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V.

2.6.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 8 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 1.8 V.

Table 8. DDR2 SDRAM DC Electrical Characteristics for V_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	1.7	1.9	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} – 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DD} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} – 0.125$	V
Output leakage current[4]	I_{OZ}	–30	30	µA
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

Table 9 provides the DDR capacitance when V_{DDDDR}(typ) = 1.8 V.

Table 9. DDR2 SDRAM Capacitance for V_{DDDDR}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF
Note: This parameter is sampled. V_{DDDDR} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = V_{DDDDR}/2, V_{OUT} (peak-to-peak) = 0.2 V.				

2.6.1.2 DDR (2.5V) SDRAM DC Electrical Characteristics

Table 10 provides the recommended operating conditions for the DDR SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 2.5 V.

Table 10. DDR SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	2.3	2.7	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V
Input high voltage	V_{IH}	MV_{REF} + 0.15	V_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.15	V
Output leakage current[4]	I_{OZ}	–30	30	μA
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \leq V_{OUT} \leq V_{DDDDR}$.

Table 11 provides the DDR capacitance when V_{DDDDR} (typ) = 2.5 V.

Table 11. DDR SDRAM Capacitance for V_{DDDDR} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF
Note: This parameter is sampled. V_{DDDDR} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = V_{DDDDR}/2, V_{OUT} (peak-to-peak) = 0.2 V.				

Table 12 lists the current draw characteristics for MV_{REF}.

Table 12. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REF}	I_{MVREF}	—	500	μA
Note: The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.				

2.6.2 Serial RapidIO DC Electrical Characteristics

DC receiver logic levels are not defined since the receiver is AC-coupled.

2.6.2.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$ are AC-coupled differential inputs. Each differential clock input has an internal 50 Ω termination to GND_{SXC}. The reference clock must be able to drive this termination. The recommended minimum operating voltage is –0.4 V; the recommended maximum operating voltage is 1.32 V; and the maximum absolute voltage is 1.72 V.

The maximum average current allowed in each input is 8 mA. This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 Ω = 8 mA) while the minimum common mode input level is GND_{SXC}. For example, a clock with a 50/50 duty cycle can be driven by a current source output that ranges from 0 mA to 16 mA (0–0.8 V). The input is AC-coupled internally, so, therefore, the exact common mode input voltage is not critical.

Note: This internal AC-couple network does not function correctly with reference clock frequencies below 90 MHz.

If the device driving the $\overline{\text{SRIO\_REF\_CLK}}$ inputs cannot drive 50 Ω to GND_{SXC}, or if it exceeds the maximum input current limitations, then it must use external AC-coupling. The minimum differential peak-to-peak amplitude of the input clock is 0.4 V (0.2 V peak-to-peak per phase). The maximum differential peak-to-peak amplitude of the input clock is 1.6 V peak-to-peak (see **Figure 5**. The termination to GND_{SXC} allows compatibility with HCSL type reference clocks specified for PCI-Express applications. Many other low voltage differential type outputs can be used but will probably need to be AC-coupled due to the limited common mode input range. LVPECL outputs can produce too large an amplitude and may need to be source terminated with a divider network to reduce the amplitude. The amplitude of the clock must be at least a 400 mV differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive 100 mV around common mode voltage. The differential reference clock (SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$) input is HCSL-compatible DC coupled or LVDS-compatible with AC-coupling.

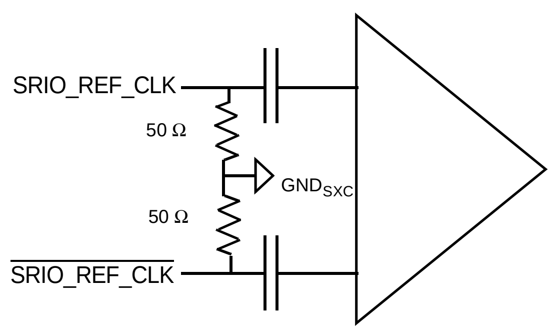


Figure 5. SerDes Reference Clocks Input Stage

2.6.2.2 Spread Spectrum Clock

SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$ is designed to work with a spread spectrum clock (0 to 0.5% spreading at 3033 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.6.3 PCI DC Electrical Characteristics

The measurements in **Table 13** assume the following system conditions:

- T_A = 25 °C
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal conditions.

Table 13. PCI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDPCI}	3.135	3.465	V
Input high voltage	V_{IH}	0.5 × V_{DDPCI}	3.465	V
Input low voltage	V_{IL}	–0.5	0.3 × V_{DDPCI}	V
Input Pull-up voltage[2]	V_{IPU}	0.7 × V_{DDPCI}		
Input leakage current, 0<V_{IN} <V_{DDPCI}	I_{IN}	–10	10	µA
Tri-state (high impedance off state) leakage current, 0<V_{IN} <V_{DDPCI}	I_{OZ}	–10	10	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–10	10	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–10	10	µA
Output high voltage, I_{OH} = –0.5 µA, except open drain pins	V_{OH}	0.9 × V_{DDPCI}	—	V
Output low voltage, I_{OL}= 1.5 µA	V_{OL}	—	0.1 × V_{DDPCI}	V
Input Pin Capacitance	C_{IN}		10	pF

Notes:
1. See **Figure 6** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.

2.6.4 TDM DC Electrical Characteristics

The measurements in **Table 14** assume the following system conditions:

- T_A = 25 °C
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal conditions.

Table 14. TDM DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDTDM}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, 0<V_{IN} <V_{DDTDM}	I_{IN}	–10	10	µA
Tri-state (high impedance off state) leakage current,	I_{OZ}	–10	10	µA
Signal input current,[1]	I_L	–10	10	µA
Output high voltage, I_{OH} = –1.6 mA,	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 0.4mA	V_{OL}	—	0.4	V
Pin Capacitance	Cp		8	pF

Note: Not tested. Guaranteed by design.

2.6.5 UART DC Electrical Characteristics

TBD

2.6.6 Ethernet DC Electrical Characteristics

The measurements assume:

- T_A = 25 °C
- GND = 0 V_{DC}

2.6.6.1 MII, SMII and RMII DC Electrical Characteristics

Table 15. MII, SMII and RMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDGE1} V_{DDGE2}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–10	10	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–10	10	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–10	10	µA
Output high voltage, I_{OH} = –4 mA,	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 4mA	V_{OL}	—	0.4	V
Input Pin Capacitance	C_{IN}		8	pF
Note: Not tested. Guaranteed by design.				

2.6.6.2 RGMII DC Electrical Characteristics

Table 16. RGMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 2.5V	V_{DDGE1} V_{DDGE2}	2.375	2.625	V
Input high voltage	V_{IH}	1.7	2.625	V
Input low voltage	V_{IL}	–0.3	0.7	V
Input high voltage ac	$V_{IH\text{-}AC}$	1.9	—	V
Input low voltage ac	$V_{IL\text{-}AC}$	—	0.7	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–10	10	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–10	10	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–10	10	µA
Output high voltage, I_{OH} = –1 mA,	V_{OH}	2.0	2.625	V
Output low voltage, I_{OL}= 1 mA	V_{OL}	—	0.4	V
Input Pin Capacitance	C_{IN}		8	pF
Note: Not tested. Guaranteed by design.				

2.6.7 ATM/UTOPIA DC Electrical Characteristics

Table 17. ATM/UTOPI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–10	10	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–10	10	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–10	10	µA
Output high voltage, I_{OH} = –8 mA,	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 8 mA	V_{OL}	—	0.5	V
Notes: **1.** Not tested. Guaranteed by design.				

2.6.8 SPI DC Electrical Characteristics

Table 18 provides the SPI DC electrical characteristics.

Table 18. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	µA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

2.6.9 GPIO, EE, CLKIN, JTAG Ports DC Electrical Characteristics

The measurements in **Table 19** assume:

- T_A = 25 °C
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal conditions.

Table 19. GPIO and CLKIN DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–10	10	µA
Tri-state (high impedance off state) leakage current, V_{IN} = supply voltage	I_{OZ}	–10	10	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–10	10	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–10	10	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	3.465	V

Table 19. GPIO and CLKIN DC Electrical Characteristics (continued)

Characteristic	Symbol	Min	Max	Unit
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V
Notes: **1.** See **Figure 6** for undershoot and overshoot voltages. **2.** Not tested. Guaranteed by design.				

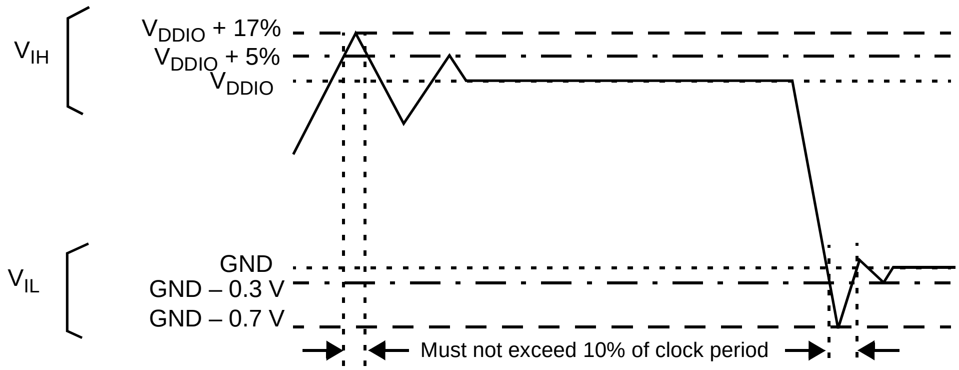


Figure 6. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.7 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs.

2.7.1 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.7.2** describes the clocking characteristics. **Section 2.7.3** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8144 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence using the V_{DDIO} (3.3 V) supply. See **Table 24** for timing. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. During functional operation when JTAG is not used, $\overline{\text{TRST}}$ can be asserted and remain asserted after the power ramp.

Note: For applications that use M3 memory, $\overline{\text{M3\_RESET}}$ should replicate the $\overline{\text{PORESET}}$ sequence timing, but using the V_{DDM3IO} (2.5 V) supply. See **Section 3.1.1**, *Power-on Sequence* for additional design information.

- CLKIN should start toggling at least 32 cycles before the $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 7**). 32 cycles should be accounted only after V_{DDIO} reaches its nominal value.
- CLKIN and PCI_CLK_IN should either be stable low during the power-up of V_{DDIO} supply and start their swings after power-up or should swing within V_{DDIO} range during V_{DDIO} power-up., so their amplitude grows as V_{DDIO} grows during power-up.

Figure 7 shows a sequence in which V_{DDIO} is raised after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

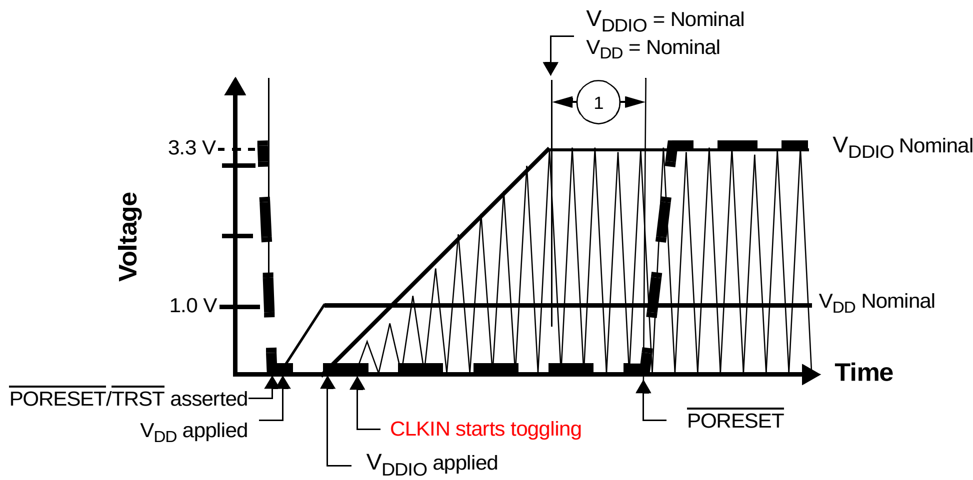


Figure 7. Start-Up Sequence with V_{DD} Raised Before V_{DDIO} with CLKIN Started with V_{DDIO}

2.7.2 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 20** shows the maximum frequency values for internal (Core, Reference, Bus and DSI) and external (CLKIN, PCI_CLK_IN and CLKOUT. The user must ensure that maximum frequency values are not exceeded.

Table 20. Clock Frequencies

Characteristic	Symbol	MIN	Max	Unit
CLKIN frequency	F_{CLKIN}	25	150	MHz
PCI_CLK_IN frequency	$F_{PCI\_CLK\_IN}$	25	150	MHz
CLKIN duty cycle	D_{CLKIN}	40	60	%
PCI_CLK_IN duty cycle	$D_{PCI\_CLK\_IN}$	40	60	%

Table 21. Clock Parameters

Characteristic	Min	Max	Unit
CLKIN slew rate	1	—	V/ns
PCI_CLK_IN slew rate	1	—	V/ns

2.7.3 Reset Timing

The MSC8144 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- JTAG reset
- RapidIO reset
- Software hard reset
- Software soft reset

All MSC8144 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 22** describes the reset sources.

Table 22. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC8144 and configures various attributes of the MSC8144. On PORESET, the entire MSC8144 device is reset. All PLLs states is reset, HRESET and SRESET are driven, the extended cores are reset, and system configuration is sampled. The reset source and word are configured only when PORESET is asserted.
External hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8144. While HRESET is asserted, SRESET is also asserted. HRESET is an open-drain pin. Upon hard reset, HRESET and SRESET are driven, the extended cores are reset, and system configuration is sampled. Note that the RCW (reset Configuration Word) is not reloaded during HRESET assertion after out of power on reset sequence. The reset configuration word is described in the Reset chapter in the MSC8144 Reference Manual.
External soft reset (SRESET)	Input/ Output	Initiates the soft reset flow. The MSC8144 detects an external assertion of SRESET only if it occurs while the MSC8144 is not asserting reset. SRESET is an open-drain pin. Upon soft reset, SRESET is driven, the extended cores are reset, and system configuration is maintained.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.
Software watchdog reset	Internal	When the MSC8144 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
RapidIO reset	Internal	When the RapidIO logic asserts the RapidIO hard reset signal, it generates an internal hard reset sequence.
Software hard reset	Internal	A hard reset sequence can be initialized by writing to a memory mapped register (RCR)
Software soft reset	Internal	A soft reset sequence can be initialized by writing to a memory mapped register (RCR)

Table 23 summarizes the reset actions that occur as a result of the different reset sources.

Table 23. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.7.3.2** for details).	Yes	No	No	No
PLL state reset	Yes	No	No	No
Select reset configuration source	Yes	No	No	No
System reset configuration write	Yes	No	No	No
HRESET driven	Yes	Yes	No	No
IPBus modules reset (TDM, UART, SWT, DDRC, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
SRESET driven	Yes	Yes	Yes	Depends on command
Extended cores reset	Yes	Yes	Yes	Yes
CLASS registers reset	Yes	Yes	Some registers	Some registers
Timers, Performance Monitor	Yes	Yes	No	No
Packet Processor, PCI, DMA	Yes	Yes	Most registers	Most registers

2.7.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 32 CLKIN cycles after V_{DD} and V_{DDIO} are both at their nominal levels.

2.7.3.2 Reset Configuration

The MSC8144 has two mechanisms for writing the reset configuration:

- Through the I^{2}C port
- Through external pins
- Through internal hard coded

Twenty-three signals (see **Section 1** for signal description details) are sampled during the power-on reset sequence to define the Reset Word Configuration Source and operating conditions:

- RCW_SRC[2–0]
- RC[16–0]

The RCFG_CLKIN_RNG pin must be valid during power-on or hard reset sequence. The STOP_BS pin must be always valid and is also sampled during power-on reset sequence for RCW loading from an I^{2}C EEPROM.

2.7.3.3 Reset Timing Tables

Table 24 and **Figure 8** describe the reset timing for a reset configuration.

Table 24. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Max	Min	Unit
1	Required external PORESET duration minimum	32/CLKIN			
	• 25 MHz <= CLKIN < 44 MHz		1280	727	ns
	• 44 MHz <= CLKIN < 66 MHz		728	484	ns
	• 66 MHz <= CLKIN < 100 MHz		485	320	ns
	• 100 MHz <= CLKIN < 133 MHz		320	241	ns
2	Delay from de-assertion of external PORESET to HRESET deassertion for external pins and hard coded RCW				
	• 25 MHz <= CLKIN < 66 MHz	15369/CLKIN	615	233	µs
	• 66 MHz <= CLKIN <= 133 MHz	34825/CLKIN	528	262	µs
	Delay from de-assertion of external PORESET to HRESET deassertion for loading RCW the I^{2}C interface				
	• 25 MHz <= CLKIN < 44 MHz	92545/CLKIN	3702	2103	µs
	• 44 MHz <= CLKIN < 66 MHz	107435/CLKIN	2441	1627	µs
	• 66 MHz <= CLKIN < 100 MHz	124208/CLKIN	1882	1242	µs
	• 100 MHz <= CLKIN < 133 MHz	157880/CLKIN	1579	1187	µs
3	Delay from HRESET deassertion to SRESET deassertion				
	• REFCLK = 25 MHz to 133 MHz	16/CLKIN	640	120	ns
Note:	Timings are not tested, but are guaranteed by design.				

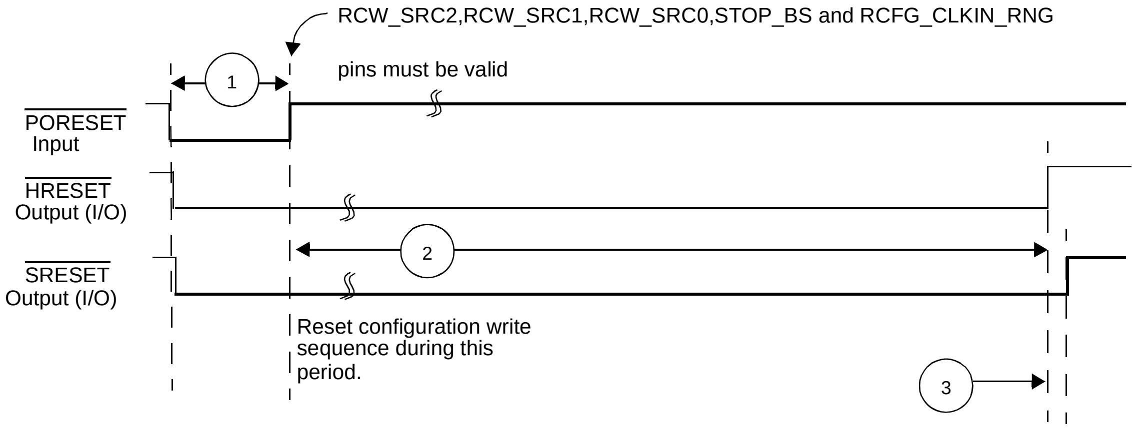


Figure 8. Timing for a Reset Configuration Write

See also Reset Errata for PLL lock and reset duration.

2.7.4 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.7.4.1 DDR SDRAM Input Timings

Table 22 provides the input AC timing specifications for the DDR SDRAM when V_{DD}(typ) = 2.5 V.

Table 22. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V
Note: At recommended operating conditions with V_{DD} of 2.5 ± 5%.				

Table 23 provides the input AC timing specifications for the DDR SDRAM when V_{DD}(typ) = 1.8 V.

Table 23. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	V_{REF} – 0.25	V
AC input high voltage	V_{IH}	V_{REF} + 0.25	—	V
Note: At recommended operating conditions with V_{DD} of 1.8 ± 5%.				

Table 24 provides the input AC timing specifications for the DDR SDRAM interface.

Table 24. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit
Controller Skew for MDQS—MDQ/MECC/MDM[1]	t_{CISKEW}			
• 400 MHz		–365	365	ps
• 333 MHz		–390	390	ps
• 266 MHz		–428	428	ps
• 200 MHz		–490	490	ps
Notes: **1.** t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget. **2.** At recommended operating conditions with V_{DD} (1.8 V or 2.5 V) ± 5%				

2.7.4.2 DDR SDRAM Output AC Timing Specifications

Table 25 provides the output AC timing specifications for the DDR SDRAM interface.

Table 25. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)[2]	t_{MCK}	3	10	ns
ADDR/CMD output setup with respect to MCK[3] • 400 MHz • 333 MHz • 266 MHz • 200 MHz	t_{DDKHAS}	 1.95 2.40 3.15 4.20	 — — — —	 ns ns ns ns
ADDR/CMD output hold with respect to MCK[3] • 400 MHz • 333 MHz • 266 MHz • 200 MHz	t_{DDKHAX}	 1.95 2.40 3.15 4.20	 — — — —	 ns ns ns ns
$\overline{\text{MCSn}}$ output setup with respect to MCK[3] • 400 MHz • 333 MHz • 266 MHz • 200 MHz	t_{DDKHCS}	 1.95 2.40 3.15 4.20	 — — — —	 ns ns ns ns
$\overline{\text{MCSn}}$ output hold with respect to MCK[3] • 400 MHz • 333 MHz • 266 MHz • 200 MHz	t_{DDKHCX}	 1.95 2.40 3.15 4.20	 — — — —	 ns ns ns ns
MCK to MDQS Skew[4]	t_{DDKHMH}	–0.6	0.6	ns
MDQ/MECC/MDM output setup with respect to MDQS[5] • 400 MHz • 333 MHz • 266 MHz • 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 700 900 1100 1200	 — — — —	 ps ps ps ps
MDQ/MECC/MDM output hold with respect to MDQS[5] • 400 MHz • 333 MHz • 266 MHz • 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 700 900 1100 1200	 — — — —	 ps ps ps ps
MDQS preamble start[6]	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns
MDQS epilogue end[6]	t_{DDKHME}	–0.6	0.6	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MSC8144 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. At recommended operating conditions with V_{DD} (1.8 V or 2.5 V) ± 5%.

Figure 9 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

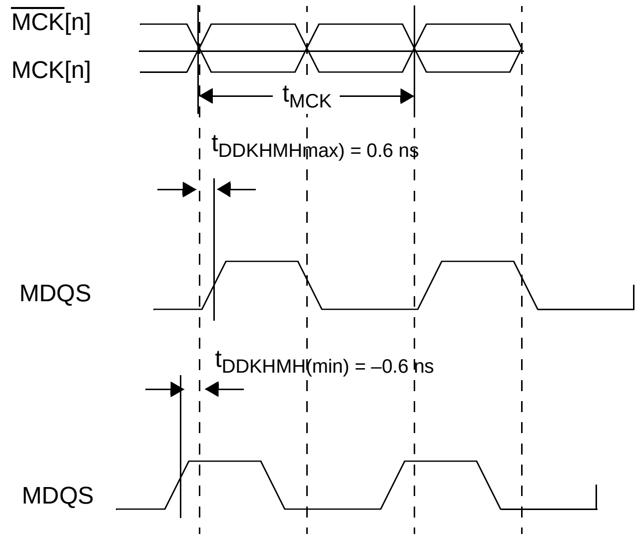


Figure 9. Timing for t_{DDKHMH}

Figure 10 shows the DDR SDRAM output timing diagram.

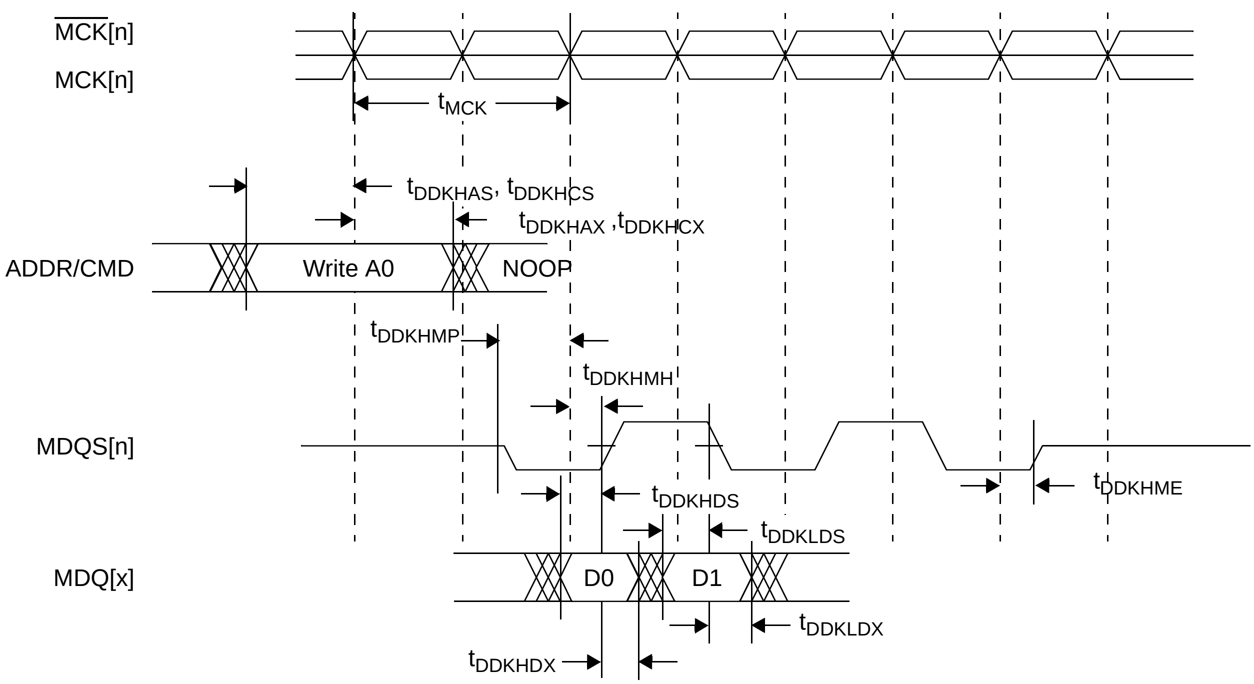


Figure 10. DDR SDRAM Output Timing

Figure 11 provides the AC test load for the DDR bus.

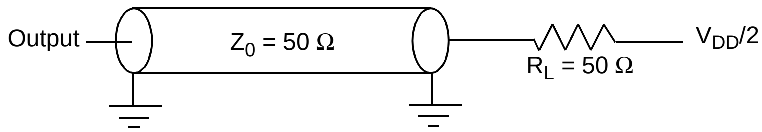


Figure 11. DDR AC Test Load

2.7.5 Serial RapidIO Timing and SGMII Timing

2.7.5.1 AC Requirements for SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$

Table 26 lists AC requirements.

Table 26. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Parameter Description	Symbol	Min	Typical	Max	Units	Comments
REFCLK cycle time	t_{REF}	—	10 (8, 6.4)	—	ns	8 ns applies only to serial RapidIO system with 125-MHz reference clock. 6.4 ns applies only to serial RapidIO systems with a 156.25 MHz reference clock. **Note:** SGMII uses the 8 ns (125 MHz) value only.
REFCLK cycle-to-cycle jitter	t_{REFCJ}	—	—	80	ps	Difference in the period of any two adjacent REFCLK cycles
Phase jitter	t_{REFPJ}	–40	—	40	ps	Deviation in edge location with respect to mean edge location

2.7.5.2 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. **Figure 12** shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between voltage levels A and B, where A > B.

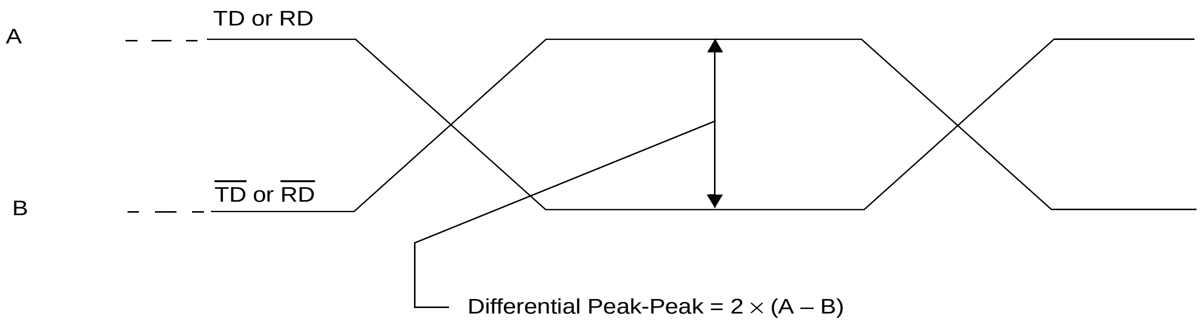


Figure 12. Differential V_{PP} of Transmitter or Receiver

Note: This explanation uses generic TD/$\overline{TD}$/RD/$\overline{RD}$ signal names. These correspond to SRIO_TXD/$\overline{SRIO\_TXD}$/ SRIO_RXD/$\overline{SRIO\_RXD}$ respectively.

Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD and $\overline{RD}$ each have a peak-to-peak voltage (V_{PP}) swing of A – B.
2. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} – V_{\overline{TD}}$.
3. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} – V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B).
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B.
6. The value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) V_{PP}.

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV_{PP}. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV_{PP}.

Note: AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described. The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of **IEEE™** Std 802.3ae-2002™. XAUI has similar application goals to serial RapidIO. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

2.7.5.3 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

2.7.5.4 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section. The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (baud frequency)/10 < freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ freq(f) ≤ baud frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from internal circuitry, packaging, and any external components related to the driver. The output impedance requirement applies to all valid output levels. It is recommended that the 20–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case. It is also recommended that the timing skew at the output of an LP-Serial transmitter between the two signals comprising a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Table 27. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 28. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple Output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 29. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

Table 30. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 31. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 32. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in **Figure 13** with the parameters specified in **Table 33** when measured at the output pins of the device and the device is driving a 100 Ω ±5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

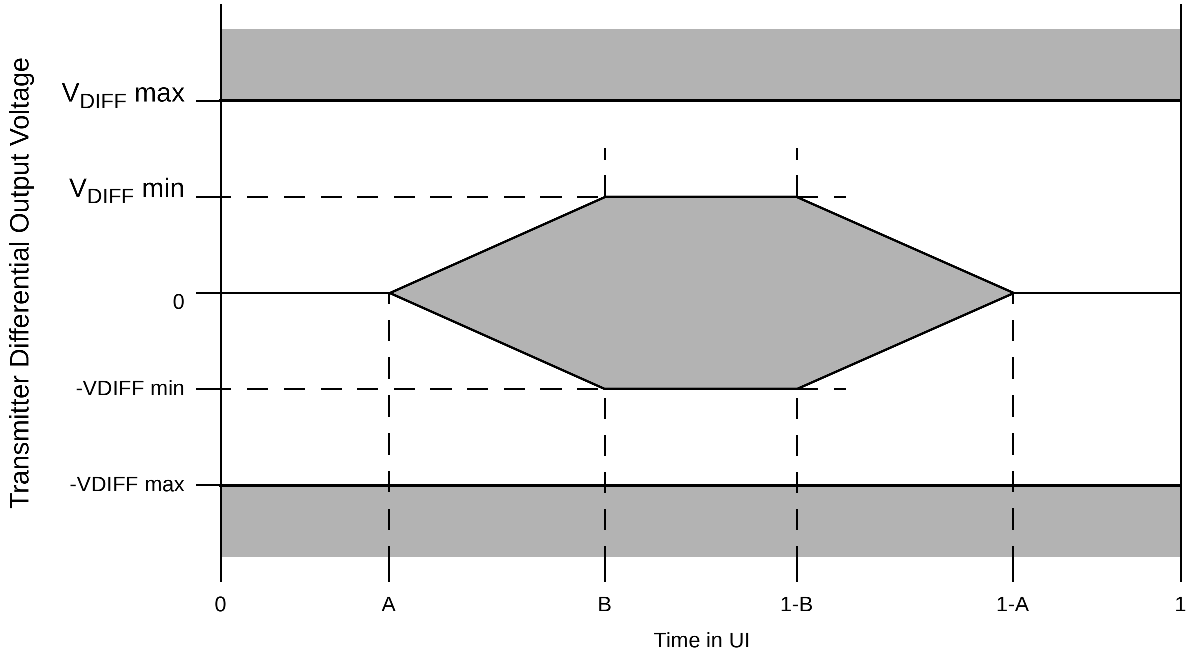


Figure 13. Transmitter Output Compliance Mask

Table 33. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

2.7.5.5 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section. Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to 0.8 × baud frequency. This includes contributions from internal circuitry, the package, and any external components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω resistive for differential return loss and 25 Ω resistive for common mode.

Table 34. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver

Table 34. Receiver AC Timing Specifications—1.25 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of **Figure 14**. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	800	800	ps	±100 ppm

Table 35. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of **Figure 14**. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	400	400	ps	±100 ppm

Table 36. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of **Figure 14**. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link

Table 36. Receiver AC Timing Specifications—3.125 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	±100 ppm

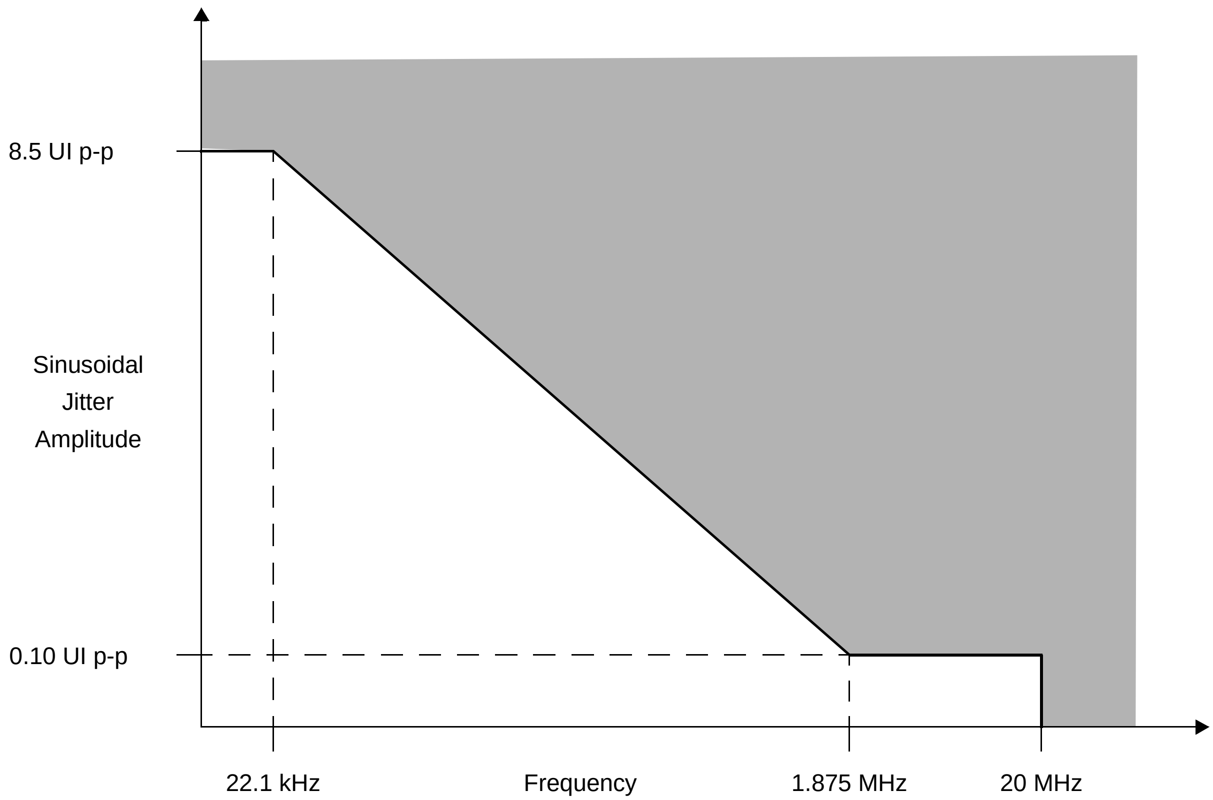


Figure 14. Single Frequency Sinusoidal Jitter Limits

2.7.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (**Table 34**, **Table 35**, and **Table 36**) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in **Figure 15** with the parameters specified in **Table 37**. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω ±5% differential resistive load.

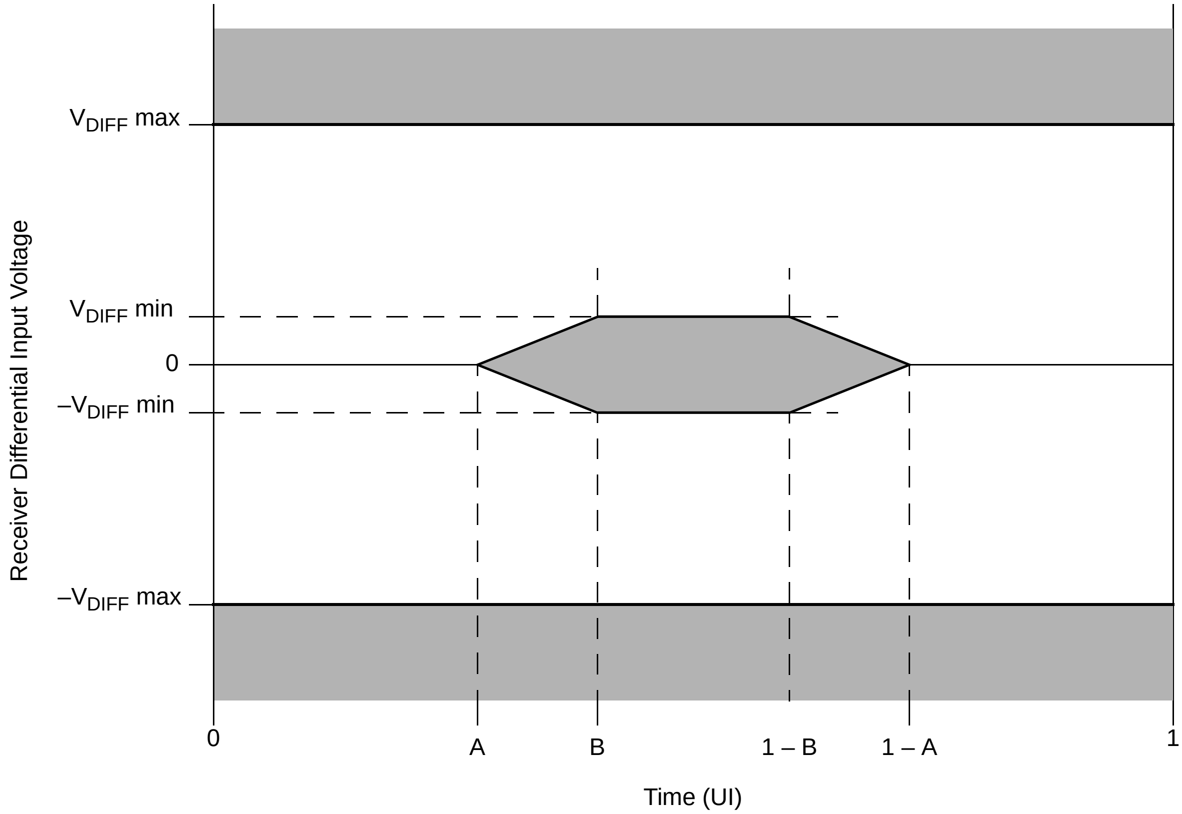


Figure 15. Receiver Input Compliance Mask

Table 37. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.7.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

2.7.5.8 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive ±5% differential to 2.5 GHz.

2.7.5.9 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of **IEEE** Std. 802.3ae.

2.7.5.10 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ±5% differential to 2.5 GHz.

2.7.5.11 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in **Section 2.7.5.9** and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in **Figure 15** and **Table 37**. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

2.7.6 PCI Timing

This section describes the general AC timing parameters of the PCI bus. **Table 38** provides the PCI AC timing specifications.

Table 38. PCI AC Timing Specifications

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Output delay	t_{PCVAL}	2.0	11.0	1.0	6.0	ns
High-Z to Valid Output delay	t_{PCON}	2.0	—	1.0	—	ns
Valid to High-Z Output delay	t_{PCOFF}	—	28	—	14	ns
Input setup	t_{PCSU}	7.0	—	3.0	—	ns
Input hold	t_{PCH}	0	—	0	—	ns
Reset active time after PCI_CLK_IN stable	$t_{PCRST-CLK}$	100	—	100	—	µs
Reset active to output float delay	$t_{PCRST-OFF}$	—	40	—	40	ns
Reset active time after power stable	t_{PCRST}	1	—	1	—	ms
$\overline{\text{HRESET}}$ high to first Configuration Access	t_{PCRHFA}	32M	—	32M	—	clocks

Notes:
1. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
2. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is in **Table 24** and **Figure 8**

Figure 16 provides the AC test load for the PCI.

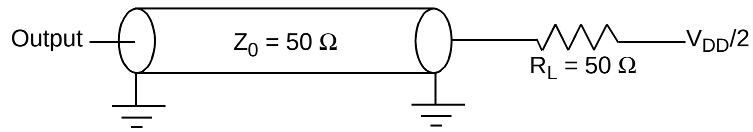


Figure 16. PCI AC Test Load

Figure 17 shows the PCI input AC timing conditions.

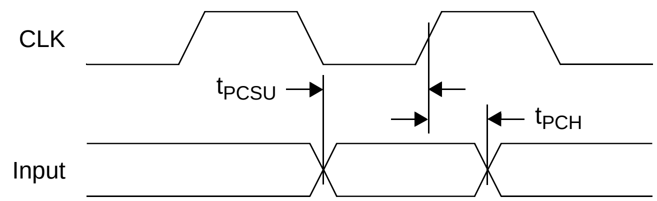


Figure 17. PCI Input AC Timing Measurement Conditions

Figure 18 shows the PCI output AC timing conditions.

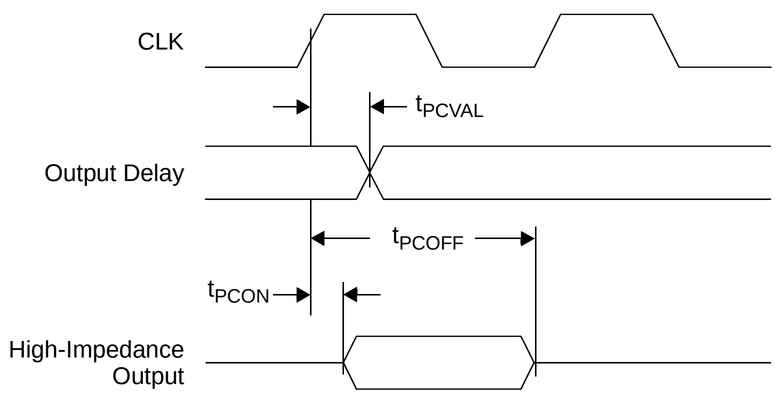


Figure 18. PCI Output AC Timing Measurement Condition

2.7.7 TDM Timing

Table 39. TDM Timing

Characteristic	Symbol	Expression	Min	Max	Units
TDMxRCLK/TDMxTCLK	t_{TDMC}	TC[1]	16	—	ns
TDMxRCLK/TDMxTCLK high pulse width	t_{TDMCH}	$(0.5 \pm 0.1) \times TC$	7	—	ns
TDMxRCLK/TDMxTCLK low pulse width	t_{TDMCL}	$(0.5 \pm 0.1) \times TC$	7	—	ns
TDM receive all input set-up time related to TDMxRCLK TDMxTSYN input set-up time related to TDMxTCLK in TSO=0 mode	t_{TDMVKH}		3.6	—	ns
TDM receive all input hold time related to TDMxRCLK TDMxTSYN input hold time related to TDMxTCLK in TSO=0 mode	t_{TDMXKH}		1.9	—	ns
TDMxTCLK high to TDMxTDAT output active[2]	$t_{TDMDHOX}$		2.5	—	ns
TDMxTCLK high to TDMxTDAT output valid[2]	$t_{TDMDHOV}$		—	9.8	ns
All output hold time (except TDMxTSYN) [3]	t_{TDMHOX}		2.5	—	ns
TDMxTCLK high to TDMxTDAT output high impedance[2]	$t_{TDMDHOZ}$		—	9.8	ns
TDMxTCLK high to TDMxTSYN output valid[2]	$t_{TDMSHOV}$		—	9.25	ns
TDMxTSYN output hold time[3]	$t_{TDMSHOX}$		1.6	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. Values are based on 10 pF capacitive load.

Figure 19 shows the TDM input AC timing.

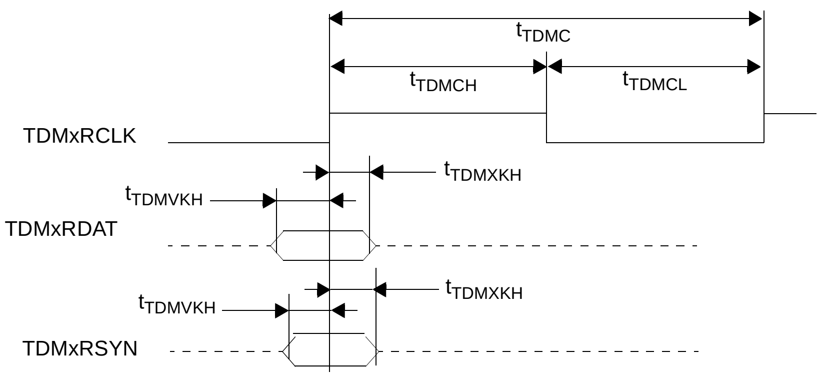


Figure 19. TDM Inputs Signals

Note: For some TDM modes receive data and receive sync are being input on other pins. This timing is valid for them as well. See the *MSC8144 Reference Manual*.

Figure 20 shows TDMxTSYN AC timing in TSO=0 mode.

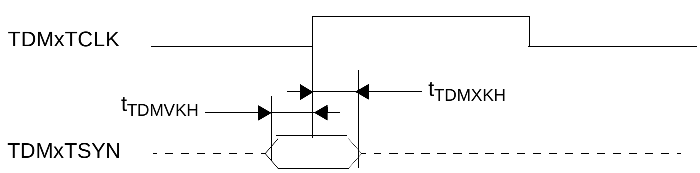


Figure 20. TDMxTSYN in TSO=0 mode

Figure 21 shows the TDM Output AC timing

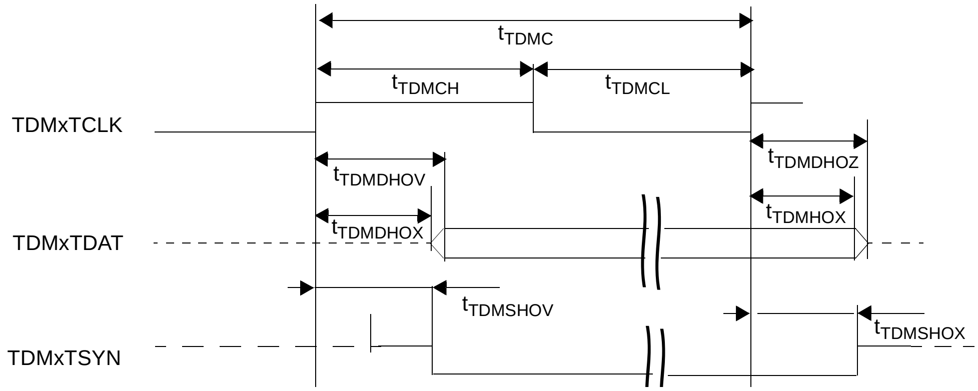


Figure 21. TDM Output Signals

Note: For some TDM modes transmit data is being output on other pins. This timing is valid for it as well. See the *MSC8144 Reference Manual*

2.7.8 UART Timing

Table 40. UART Timing

Characteristics	Symbol	Expression	Min	Max	Unit
URXD and UTXD inputs high/low duration	$T_{UREFCLK}$	$16 \times T_{REFCLK}$	160	—	ns
URXD and UTXD inputs rise/fall time	T_{UAVKH}			6	ns
UTXD output rise/fall time	T_{UAVXH}			5.5	ns
Note: $T_{UREFCLK} = T_{REFCLK}$ is guaranteed by design.					

Figure 22 shows the UART input AC timing

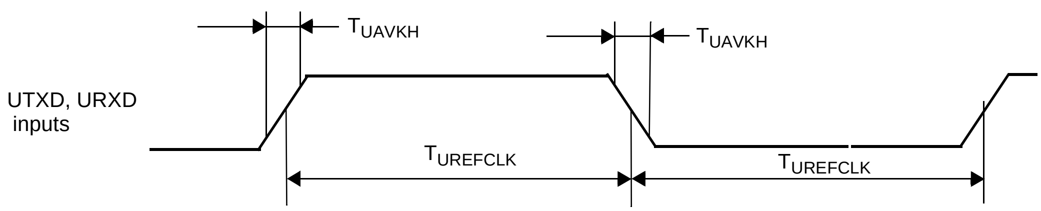


Figure 22. UART Input Timing

Figure 23 shows the UART output AC timing

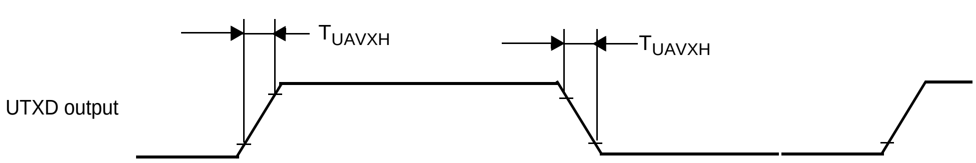


Figure 23. UART Output Timing

2.7.9 Timer Timing

Table 41. Timer Timing

Characteristics	Symbol	Min	Unit
TIMERx frequency	$T_{TMREFCLK}$	10.0	ns
TIMERx Input high phase	T_{TMCH}	4.0	ns
TIMERx Output low phase	T_{TMCL}	4.0	ns

Figure 24 shows the timer input AC timing

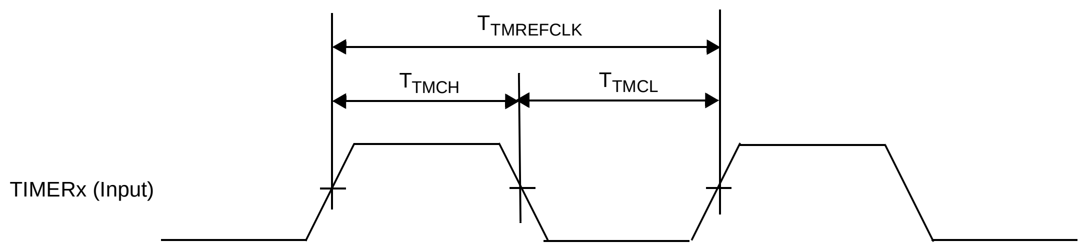


Figure 24. Timer Timing

2.7.10 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each Interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the MSC8144 Reference Manual.

2.7.10.1 Management Interface Timing

Table 42. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
ETHMDC clock pulse width high	t_{MDCH}	32	—	ns
ETHMDC to ETHMDIO delay[2]	t_{MDKHDX}	10	70	ns
ETHMDIO to ETHMDC rising edge set-up time	t_{MDDVKH}	5	—	ns
ETHMDC rising edge to ETHMDIO hold time	t_{MDDXKH}	0	—	ns
ETHMDC rise time.	t_{MDCR}	—	10	ns
ETHMDC fall time.	t_{MDHF}	—	10	ns

Notes:
1. Typical ETHMDC frequency (f_{MDC}) is 2.5 MHz with a 400 ns period (t_{MDC}). The value depends on the source clock. For example, for a source clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz. For a 375 MHz clock, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

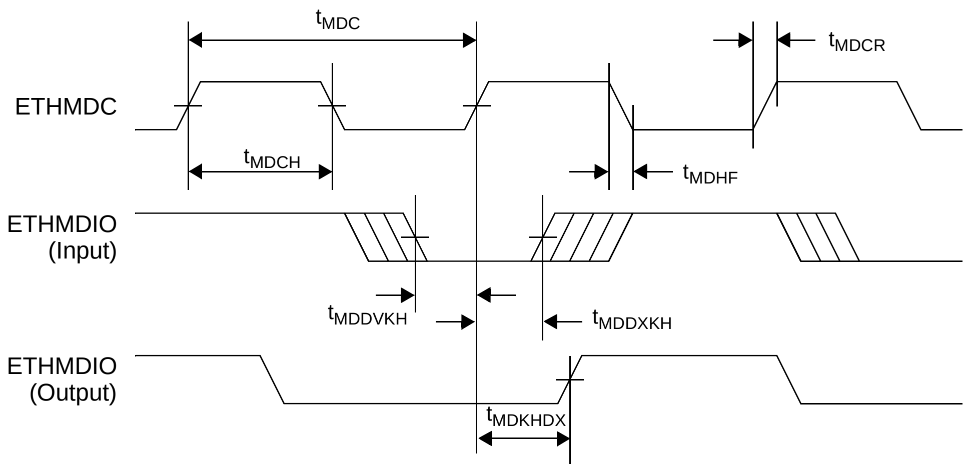


Figure 25. MII Management Interface Timing

2.7.10.2 MII Transmit AC Timing Specifications

Table 43 provides the MII transmit AC timing specifications.

Table 43. MII Transmit AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	25	ns
TX_CLK data clock rise	t_{MTXR}	1.0	4.0	ns
TX_CLK data clock fall	t_{MTXF}	1.0	4.0	ns

Notes:
1. Typical TX_CLK period (t_{MTX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns.
2. Program GCR4 as 0x00030CC3.

Figure 26 shows the MII transmit AC timing diagram.

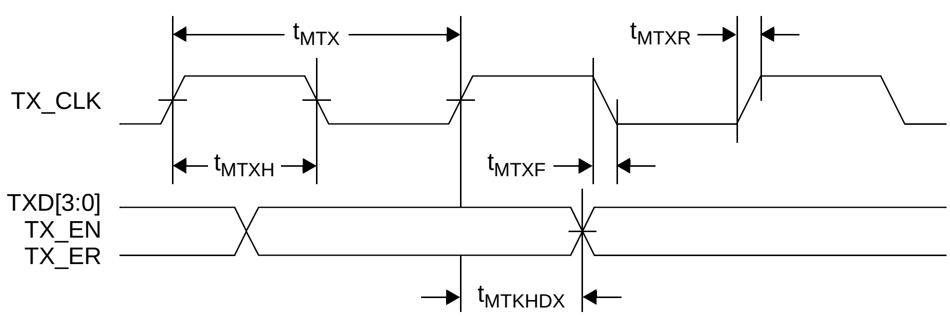


Figure 26. MII Transmit AC Timing

2.7.10.3 MII Receive AC Timing Specifications

Table 44 provides the MII receive AC timing specifications.

Table 44. MII Receive AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	65	%

Table 44. MII Receive AC Timing Specifications (continued)

Parameter/Condition	Symbol [1]	Min	Max	Unit
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	2	—	ns
RX_CLK clock rise	t_{MRXR}	1.0	4.0	ns
RX_CLK clock fall time	t_{MRXF}	1.0	4.0	ns
Notes: **1.** Typical RX_CLK period (t_{MRX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns. **2.** Program GCR4 as 0x00030CC3.				

Figure 27 provides the AC test load.

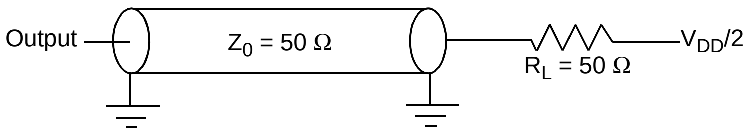


Figure 27. AC Test Load

Figure 28 shows the MII receive AC timing diagram.

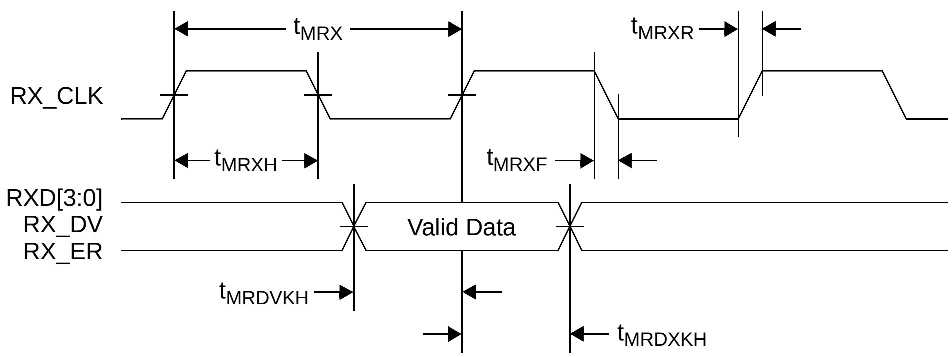


Figure 28. MII Receive AC Timing

2.7.10.4 RMII Transmit and Receive AC Timing Specifications

Table 45 provides the RMII transmit and receive AC timing specifications.

Table 45. RMII Transmit and Receive AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	65	%
REF_CLK to RMII data TXD[1–0], TX_EN delay	$t_{RMTKHDX}$	2	10	ns
RXD[1–0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	ns
RXD[1–0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	ns
REF_CLK data clock rise	t_{RMXR}	1.0	4.0	ns
REF_CLK data clock fall	t_{RMXF}	1.0	4.0	ns
Typical REF_CLK clock period (t_{RMX}) is 20 ns				
Notes: **1.** Typical REF_CLK clock period (t_{RMX}) is 20 ns **2.** Program GCR4 as 0x00001405				

Figure 29 shows the RMII transmit and receive AC timing diagram.

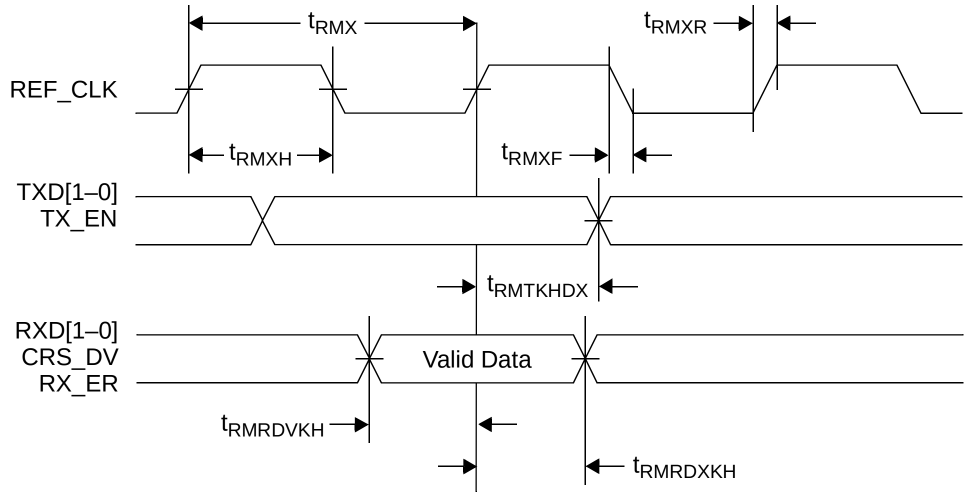


Figure 29. RMII Transmit and Receive AC Timing

Figure 30 provides the AC test load.

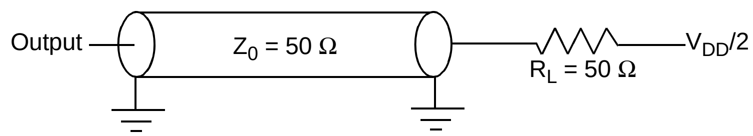


Figure 30. AC Test Load

2.7.10.5 SMII AC Timing Specification

Table 46. SMII Mode Signal Timing

Characteristics	Symbol	Min	Max	Unit
ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	t_{SMDVKH}	1.5	—	ns
ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	t_{SMDXKH}	1.0	—	ns
ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	t_{SMXR}	1.5	5.0	ns

Notes:
1. Typical REF_CLK clock period is 8ns
2. Measured using a 5 pF load.
3. Measured using a 15 pF load
4. REF_CLK duty cycle is TBD.
5. Program GCR4 as 0x00002008

Figure 31 provides the AC test load.

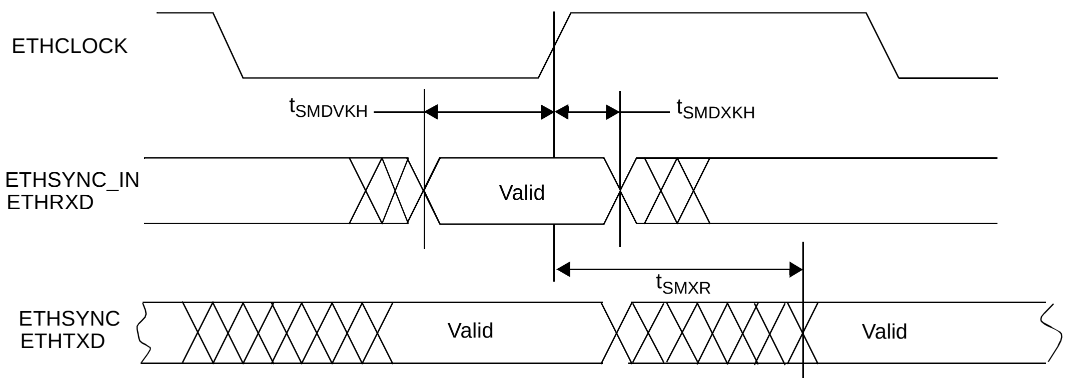


Figure 31. SMII Mode Signal Timing

2.7.10.6 RGMII AC Timing Specifications

Table 47 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 47. RGMII with On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) [2]	t_{SKEWR}	0.9	—	2.6	ns
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:
1. At recommended operating conditions with LV_{DD} of 2.5 V +/- 5%.
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns +/- 40 ns and 40 ns +/- 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $L_{Vdd}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. GCR4 should be programmed as 0x00001004.

Table 48 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 48. RGMII with No On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	0.9	—	2.6	ns
Data to clock input skew (at receiver) [2]	t_{SKEWR}	-0.5	—	0.5	ns
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns

Table 48. RGMII with No On-Board Delay AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:
1. At recommended operating conditions with LV_{DD} of 2.5 V +/- 5%.
2. This implies that PC board design will require clocks to be routed with no additional trace delay
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns +/- 40 ns and 40 ns +/- 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $L_{Vdd}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. GCR4 should be programmed as 0x00048120.

Figure 32 shows the RGMII AC timing and multiplexing diagrams.

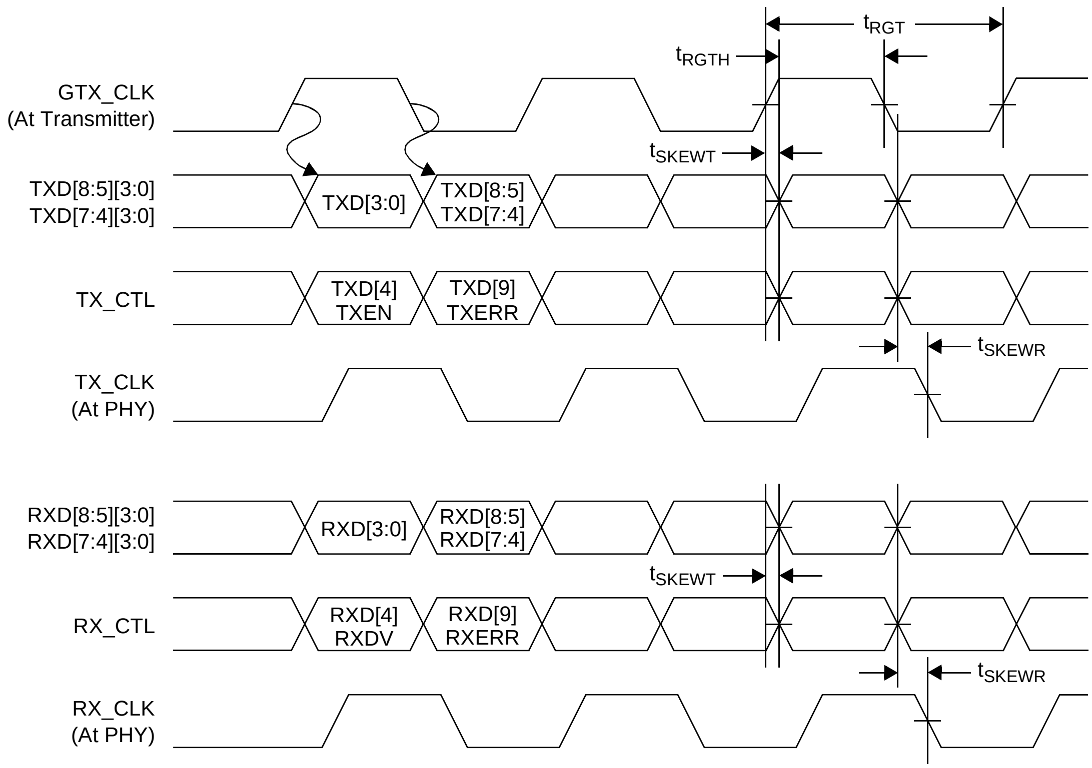


Figure 32. RGMII AC Timing and Multiplexing s

2.7.11 ATM/UTOPIA Timing

Table 49 provides the UTOPIA input and output AC timing specifications.

Table 49. UTOPIA AC Timing Specifications

Characteristic	Symbol	Min	Max	Unit
UTOPIA outputs—External clock delay	t_{UEKHOV}	1	9	ns
UTOPIA outputs—External clock High Impedance	t_{UEKHOX}	1	9	ns
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4		ns
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1		ns
Note: Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.				

Figure 33 provides the AC test load for the UTOPIA.

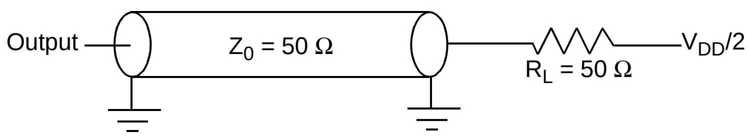


Figure 33. UTOPIA AC Test Load

Figure 34 shows the UTOPIA timing with external clock.

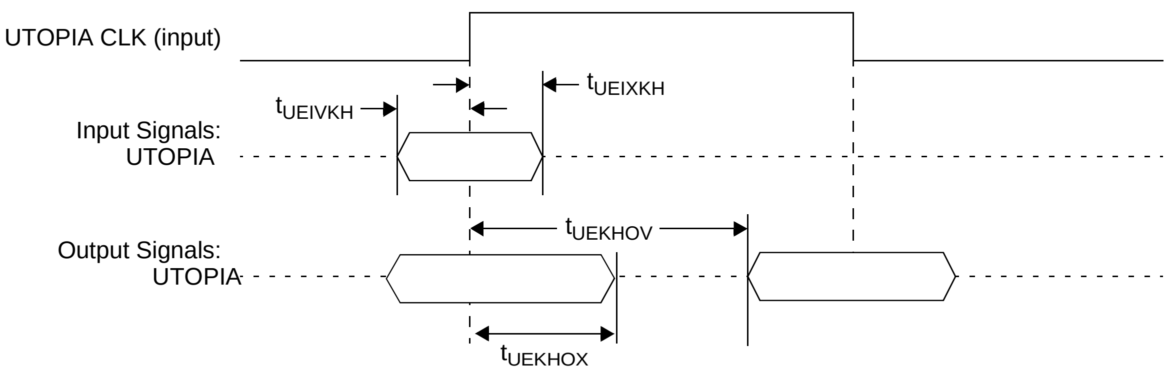


Figure 34. UTOPIA AC Timing (External Clock)

Figure 35 shows the UTOPIA timing with internal clock.

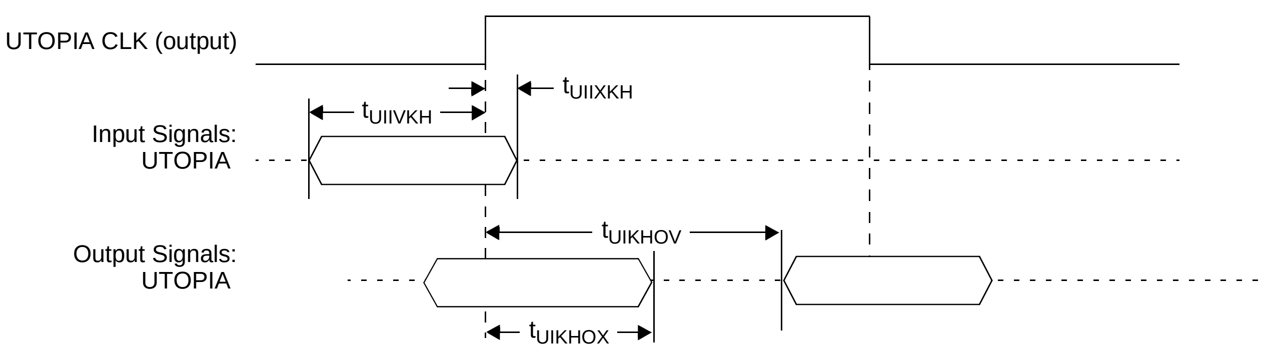


Figure 35. UTOPIA AC Timing (Internal Clock)

2.7.12 SPI Timing

Table 49 provides the SPI input and output AC timing specifications.

Table 50. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 36 provides the AC test load for the SPI.

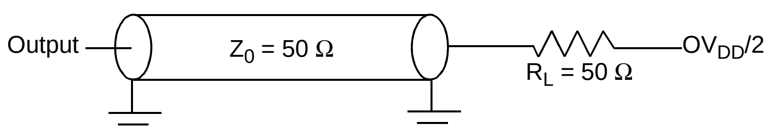
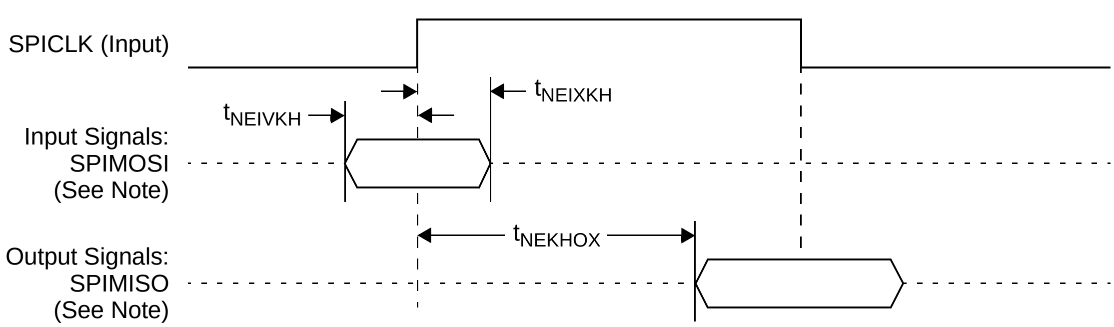


Figure 36. SPI AC Test Load

Figure 37 through Figure 38 represent the AC timings from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

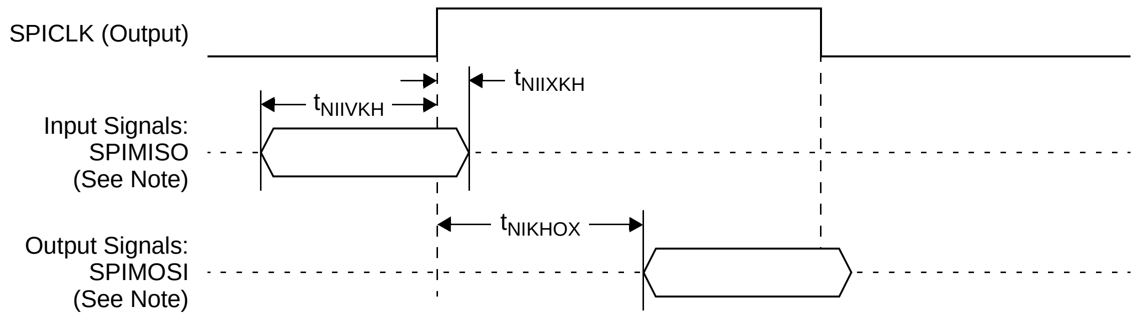
Figure 37 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 37. SPI AC Timing in Slave Mode (External Clock)

Figure 38 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 38. SPI AC Timing in Master Mode (Internal Clock)

2.7.13 GPIO Timing

Table 51. GPIO Timing

Characteristics	Symbol	Min	Max	Unit
REFCLK edge to GPIO out valid (GPIO out delay time)	t_{GPKHOV}	-	6.9	ns
REFCLK edge to GPIO out not valid (GPIO out hold time)	t_{GPKHOX}	1.3	-	ns
REFCLK edge to high impedance on GPIO out	t_{GPKHOZ}	-	6.2	ns
GPIO in valid to REFCLK edge (GPIO in set-up time)	t_{GPIVKH}	3.7	-	ns
REFCLK edge to GPIO in not valid (GPIO in hold time)	t_{GPIXKH}	0.5	-	ns

Figure 39 shows the GPIO timing.

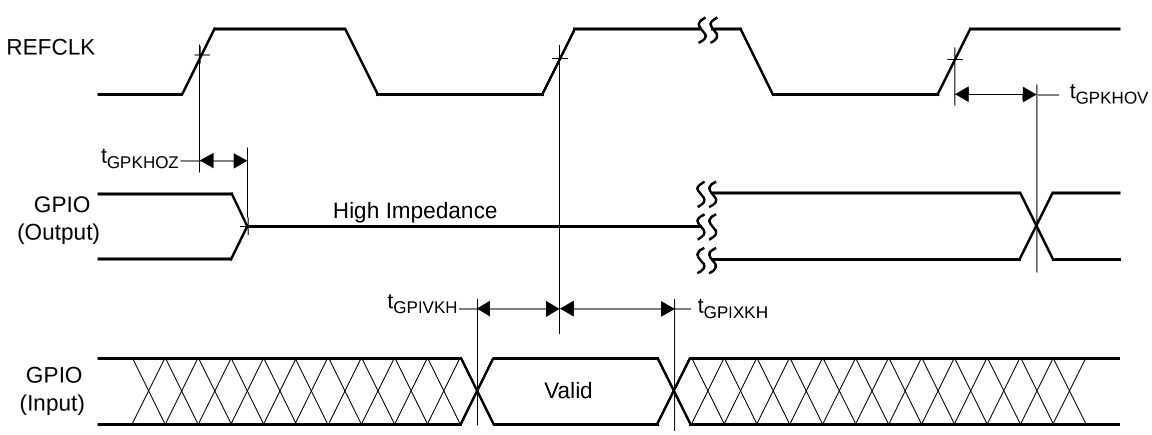


Figure 39. GPIO Timing

2.7.14 EE Signals

Table 52. EE Pin Timing

Characteristics	Symbol	Type	Min
EE (input)	t_{EEIN}	Asynchronous	4 core clock periods
EE (output)	t_{EEOUT}	Synchronous to Core clock	1 core clock period

Notes: **1.** The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Refer to **Table 1-4** on page 1-6 for details on EE pin functionality.

Figure 40 shows the signal behavior of the EE pins.

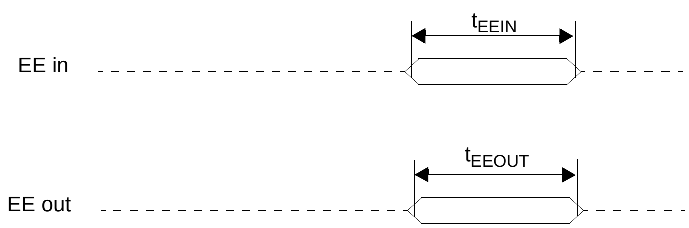


Figure 40. EE Pin Timing

2.7.14.1 JTAG Signals

Table 53. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	33.0	—	ns
TCK clock high phase measured at V_M = 1.6 V	t_{TCKH}	13.0	—	ns
TCK rise and fall times	t_{TCKR}	—	3.0	ns
Boundary scan input data set-up time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	10.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data set-up time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{\text{TRST}}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 41 Shows the Test Clock Input Timing Diagram

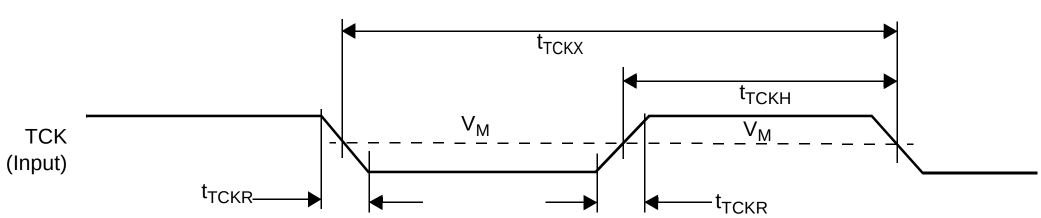


Figure 41. Test Clock Input Timing

Figure 42 Shows the boundary scan (JTAG) timing diagram.

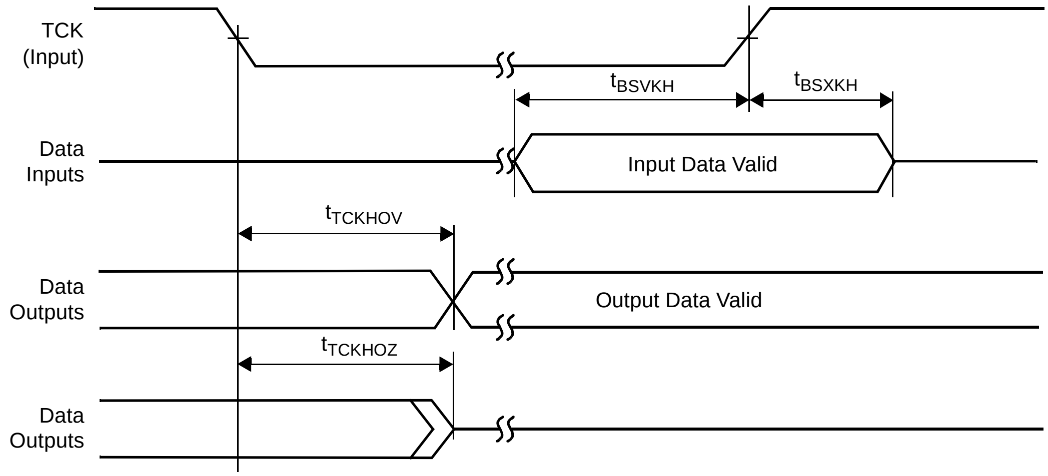


Figure 42. Boundary Scan (JTAG) Timing

Figure 43 Shows the test access port timing diagram

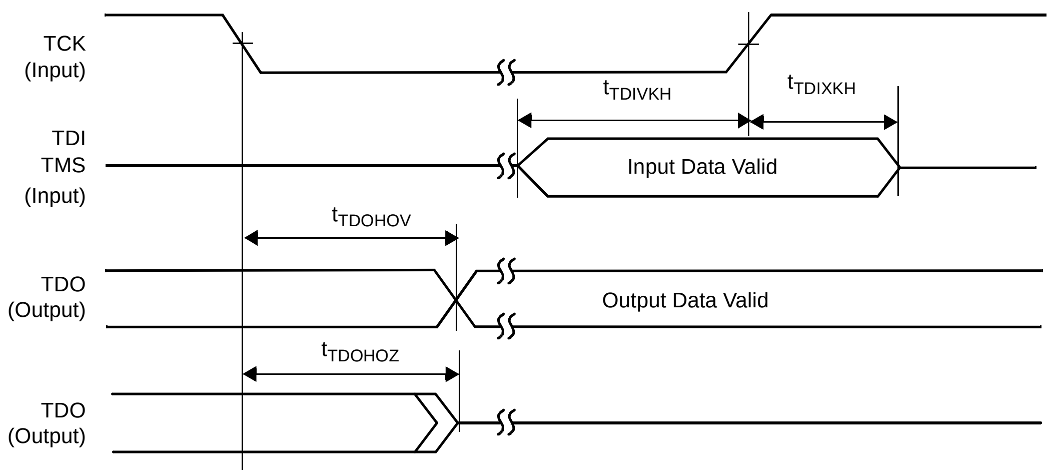


Figure 43. Test Access Port Timing

Figure 44 Shows the $\overline{\text{TRST}}$ timing diagram.

Figure 44. $\overline{\text{TRST}}$ Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8144 device is designed into a system.

3.1 Start-up Sequencing Recommendations

3.1.1 Power-on Sequence

Use the following guidelines for power-on sequencing:

- There are no dependencies in power-on/power-off sequence between V_{DDM3} and V_{DD} supplies.
- There are no dependencies in power-on/power-off sequence between RapidIO supplies: V_{DDSXC}, V_{DDSXP}, $V_{DDRIOPLL}$ and other MSC8144 supplies.
- V_{DDPLL} should be coupled with the V_{DD} power rail with extremely low impedance path.

External voltage applied to any input line must not exceed the related to this port I/O supply by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8144 device in the system during start-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4V/ns.

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see **Figure 45**):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR}.
- V_{DDM3IO}
- V_{25M3}

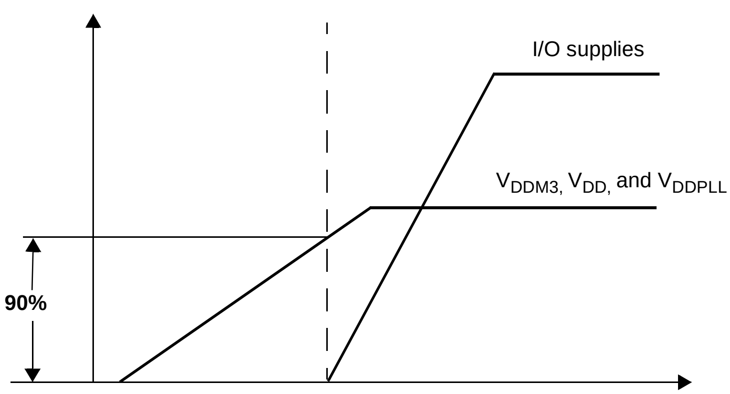


Figure 45. V_{DDM3}, V_{DDM3IO} and V_{25M3} Power-on Sequence

Note:
1. This recommended power sequencing is different from the MSC8122/MSC8126.
2. If no pins that require V_{DDGE1} as a reference supply are used (see **Table 1**), V_{DDGE1} can be tied to GND.
3. If no pins that require V_{DDGE2} as a reference supply are used (see **Table 1**), V_{DDGE2} can be tied to GND.
4. If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
5. If the M3 memory is not used, V_{DDM3}, V_{DDM3IO}, and V_{25M3} can be tied to GND.
6. If the RapidIO interface is not used, V_{DDSX}, V_{DDSXP}, and $V_{DDRIOPLL}$ can be tied to GND.

3.1.2 Start-Up Timing

Section 2.7.1 describes the start-up timing.

3.2 Power Supply Design Considerations

3.2.1 PLL Supplies

Each PLL supply must have an external RC filter for the V_{DDPLL} input. The filter is a 10 Ω resistor in series with two 2.2 µF, low ESL (<0.5 nH) and low ESR capacitors. All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately (see **Figure 46**). For optimal noise filtering, place the circuit as close as possible to its V_{DDPLL} inputs. These traces should be short and direct.

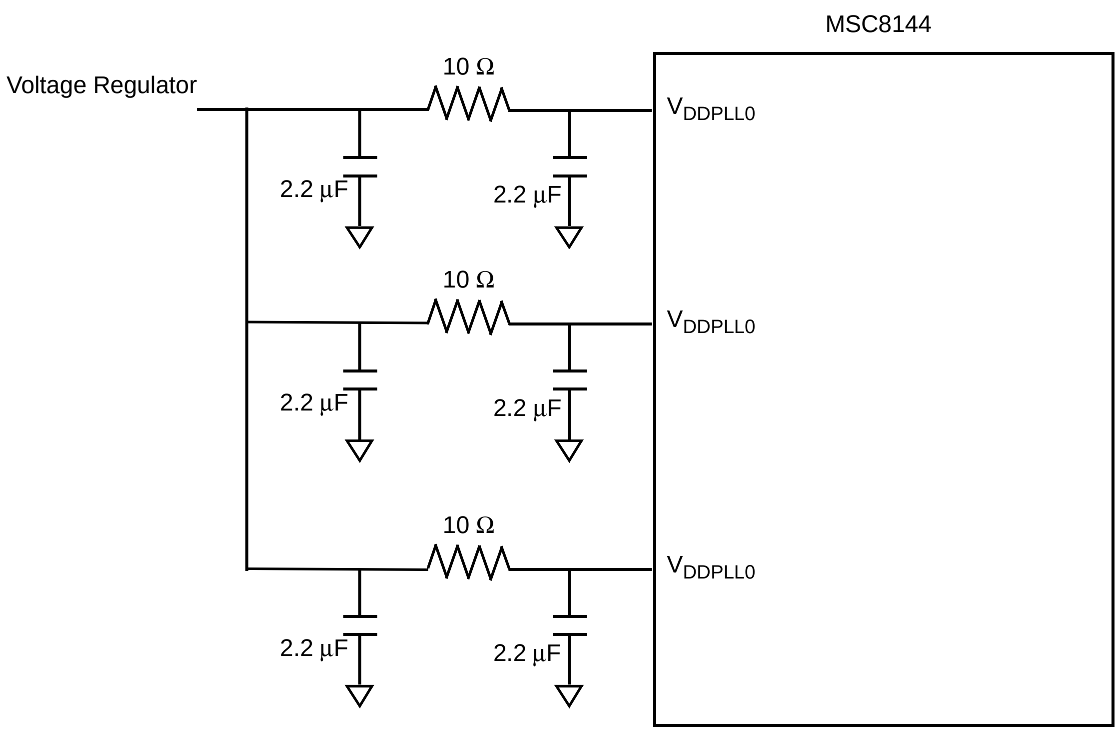


Figure 46. PLL Supplies

3.2.2 Other Supplies

TBD

3.3 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.

2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor it is clearly indicated as “pull-up/pull-down”.
4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.3.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with DDR1 and DDR2 memory.

Note: For information about unused differential/non-differential pins in DDR1/DDR2 modes (that is, unused negative lines of strobes in DDR1), please refer to **Table 54**.

3.3.1.1 DDR Interface Is Not Used

Table 54. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–31]	NC
MDQS[0–3]	NC
$\overline{\text{MDQS[0–3]}}$	NC
MA[0–15]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[0–1]}}$	NC
MDM[0–3]	NC
MBA[0–2]	NC
$\overline{\text{MCAS}}$	NC
MCKE[0–1]	NC
MODT[0–1]	NC
MDIC[0–1]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[0–7]	NC
ECC_MDM	NC
ECC_MDQS	NC
$\overline{\text{ECC\_MDQS}}$	NC
MV_{REF}	GND
V_{DDDDR}	GND
Note: If the DDR controller is not used, disable the internal DDR clock by writing a 1 to the CLK11DIS bit in the System Clock Control Register (SCCR[CLK!11DIS]). See **Chapter 7**, *Clocks*, in the **MSC8144 Reference Manual** for details.	

3.3.1.2 16-Bit DDR Memory Only

Table 55 lists unused pin connection when using 16-bit DDR memory. The 16 most significant data lines are not used.

Table 55. Connectivity of DDR Related Pins When Using 16-bit DDR Memory Only

Signal Name	Pin connection
MDQ[0–15]	in use
MDQ[16–31]	pull-up to V_{DDDDR}
MDQS[0–1]	in use
MDQS[2–3]	pull-down to GND
$\overline{\text{MDQS[0–1]}}$	in use
$\overline{\text{MDQS[2–3]}}$	pull-up to V_{DDDDR}
MA[0–15]	in use
MCK[0–2]	in use
$\overline{\text{MCK[0–2]}}$	in use
$\overline{\text{MCS[0–1]}}$	in use
MDM[0–1]	in use
MDM[2–3]	NC
MBA[0–2]	in use
$\overline{\text{MCAS}}$	in use
MCKE[0–1]	in use
MODT[0–1]	in use
MDIC[0–1]	in use
$\overline{\text{MRAS}}$	in use
$\overline{\text{MWE}}$	in use
MV_{REF}	$1/2 * V_{DDDDR}$
V_{DDDDR}	2.5 V or 1.8 V

3.3.1.3 ECC Unused Pin Connections

When the error code corrected mechanism is not used in any 32- or 16-bit DDR configuration, refer to **Table 56** to determine the correct pin connections.

Table 56. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[0–7]	pull-up to V_{DDDDR}
ECC_MDM	NC
ECC_MDQS	pull-down to GND
$\overline{\text{ECC\_MDQS}}$	pull-up to V_{DDDDR}

3.3.2 Serial RapidIO Interface Related Pins

3.3.2.1 Serial RapidIO interface Is Not Used

Table 57. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	GND
SRIO_IMP_CAL_TX	GND
$\overline{\text{SRIO\_REF\_CLK}}$	GND
SRIO_REF_CLK	GND
SRIO_RXD[0–3]	GND
$\overline{\text{SRIO\_RXD[0–3]}}$	GND
$\overline{\text{SRIO\_TXD[0–3]}}$	NC
SRIO_TXD[0–3]	NC
$V_{DDRIOPLL}$	GND
GND_{RIOPLL}	GND
GND_{SXP}	GND
GND_{SXC}	GND
V_{DDSXP}	GND
V_{DDSXC}	GND

3.3.2.2 Serial RapidIO Specific Lane Is Not Used

Table 58. Connectivity of Serial RapidIO Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	in use
SRIO_IMP_CAL_TX	in use
$\overline{\text{SRIO\_REF\_CLK}}$	in use
SRIO_REF_CLK	in use
SRIO_RXD***x***	GND_{SXC}
$\overline{\text{SRIO\_RXD}\boldsymbol{x}}$	GND_{SXC}
$\overline{\text{SRIO\_TXD}\boldsymbol{x}}$	NC
SRIO_TXD***x***	NC
$V_{DDRIOPLL}$	in use
GND_{RIOPLL}	in use
GND_{SXP}	GND_{SXP}
GND_{SXC}	GND_{SXC}
V_{DDSXP}	1.0 V
V_{DDSXC}	1.0 V
Note: The ***x*** indicates the lane number {0,1,2,3} for all unused lanes.	

3.3.3 M3 Memory Related Pins

Table 59. Connectivity of M3 Related Pins When M3 Memory Is Not Used

Signal Name	Pin Connection
$\overline{\text{M3\_RESET}}$	NC
V_{25M3}	GND
V_{DDM3}	GND
V_{DDM3IO}	GND

3.3.4 Ethernet Related Pins

3.3.4.1 Ethernet Controller 1 (GE1) Related Pins

Note: Table 60 and Table 61 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.3.4.1.1 GE1 Interface Is Not Used

Table 60 assumes that the GE1 signals are not used for any purpose (including any multiplexed functions) and that V_{DDGE1} is tied to GND.

Table 60. Connectivity of GE1 Related Pins When the GE1 Interface Is Not Used

Signal Name	Pin Connection
GE1_COL	NC
GE1_CRS	NC
GE1_RD[0–4]	NC
GE1_RX_ER	NC
GE1_RX_CLK	NC
GE1_RX_DV	NC
GE1_SGMII_RX	GND_{SXC}
$\overline{\text{GE1\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE1\_SGMII\_TX}}$	NC
GE1_SGMII_TX	NC
GE1_TD[0–4]	NC
GE1_TX_CLK	NC
GE1_TX_EN	NC
GE1_TX_ER	NC

3.3.4.1.2 Subset of GE1 Pins Required

When only a subset of the whole GE1 interface is used, such as for RMII, the unused GE1 pins should be connected as described in Table 61. This table assumes that the unused GE1 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE1} is tied to either 2.5 V or 3.3 V.

Table 61. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE1_COL	GND
GE1_CRS	GND
GE1_RD[0–3]	GND
GE1_RX_ER	GND
GE1_RX_CLK	GND
GE1_RX_DV	GND
GE1_SGMII_RX	GND_{SXC}
$\overline{\text{GE1\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE1\_SGMII\_TX}}$	NC

Table 61. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
GE1_SGMII_TX	NC
GE1_TD[0-3]	NC
GE1_TX_CLK	GND
GE1_TX_EN	NC
GE1_TX_ER	NC

3.3.4.2 Ethernet Controller 2 (GE2) Related Pins

Note: Table 62 and Table 64 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.3.4.2.1 GE2 interface Is Not Used

Table 62 assumes that the GE2 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE2} is tied to GND.

Table 62. Connectivity of GE2 Related Pins When the GE2 Interface Is Not Used

Signal Name	Pin Connection
GE2_RD[0-3]	NC
GE2_RX_CLK	NC
GE2_RX_DV	NC
GE2_RX_ER	NC
GE2_SGMII_RX	GND_{SXC}
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	Nc
GE2_TD[0–3]	Nc
GE2_TX_EN	NC

3.3.4.2.2 Subset of GE2 Pins Required

When only a subset of the whole GE2 interface is used, such as for RMII, the unused GE2 pins should be connected as described in Table 63. The table assumes that the unused GE2 pins are not used for any purpose (including any multiplexed functions) and that V_{DDGE2} is tied to either 2.5 V or 3.3 B.

Table 63. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE2_RD[0-3]	GND
GE2_RX_CLK	GND
GE2_RX_DV	GND
GE2_RX_ER	GND
GE2_SGMII_RX	GND_{SXC}

Table 63. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.3.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), Table 64 lists the recommended management pin connections.

Table 64. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

3.3.5 UTOPIA Related Pins

Table 65 lists the board connections of the UTOPIA pins when the entire UTOPIA interface is not used or subset of UTOPIA interface is used. For multiplexing options that select a subset of the UTOPIA interface, use the connections described in Table 65 for those signals that are not selected. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of UTOPIA Related Pins When UTOPIA Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V_{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
$\overline{\text{UTP\_REN}}$	V_{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V_{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
$\overline{\text{UTP\_TEN}}$	V_{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V_{DDIO}	3.3 V

3.3.6 TDM Interface Related Pins

Table 66 lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in Table 66 for those signals that are not selected. Table 66 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 66. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***x***RCLK	GND
TDM***x***RDAT	GND
TDM***x***RSYN	GND
TDM***x***TCLK	GND
TDMT***x***DAT	GND
TDM***x***TSYN	GND
V_{DDIO}	3.3 V
Notes: **1.** ***x*** = {0, 1, 2,3, 4, 5, 6, 7} **2.** In case of subset of TDM interface usage please make sure to disable unused TDM modules. See **Chapter 20**, *TDM*, in the **MSC8144 Reference Manual** for details.	

3.3.7 PCI Related Pins

Table 67 lists the board connections of the pins when PCI is not used. Table 67 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 67. Connectivity of PCI Related Pins When PCI Is Not Used

Signal Name	Pin Connection
PCI_AD[0–31]	GND
$\overline{\text{PCI\_CBE[0–3]}}$	GND
PCI_CLK_IN	GND
$\overline{\text{PCI\_DEVSEL}}$	V_{DDIO}
$\overline{\text{PCI\_FRAME}}$	V_{DDIO}
$\overline{\text{PCI\_GNT}}$	V_{DDIO}
PCI_IDS	GND
$\overline{\text{PCI\_IRDY}}$	V_{DDIO}
PCI_PAR	GND
$\overline{\text{PCI\_PERR}}$	V_{DDIO}
$\overline{\text{PCI\_REQ}}$	NC
$\overline{\text{PCI\_SERR}}$	V_{DDIO}
$\overline{\text{PCI\_STOP}}$	V_{DDIO}
$\overline{\text{PCI\_TRDY}}$	V_{DDIO}
V_{DDIO}	3.3 V

3.3.8 Miscellaneous Pins

Table 68 lists the board connections for the pins if they are required by the system design. Table 68 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 68. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ[0–15]}}$	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[0–16]	GND
$\overline{\text{RC\_LDF}}$	NC
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[0–4]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	GND
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
V_{DDIO}	3.3 V
Note: When using I/O multiplexing mode 5 or 6, tie the TDM7TSYN/PCI_AD4 signal (ball number AC9) to GND.	

Note: For details on configuration, see the *MSC8144 Reference Manual*. For additional information, refer to the *MSC8144 Design Checklist* (AN3202).

3.4 External DDR SDRAM Selection

TBD

3.5 Thermal Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$ **Equation 1**

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8144 are listed in **Table 5**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8144 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine T_J:

$$T_J = T_T + (\theta_{JA} \times P_D)$$ **Equation 2**

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)
θ_{JA} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8144	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	1.0 V	–40° to 105°C	800	TBD
				0° to 90°C	1000	TBD

5 Package Information

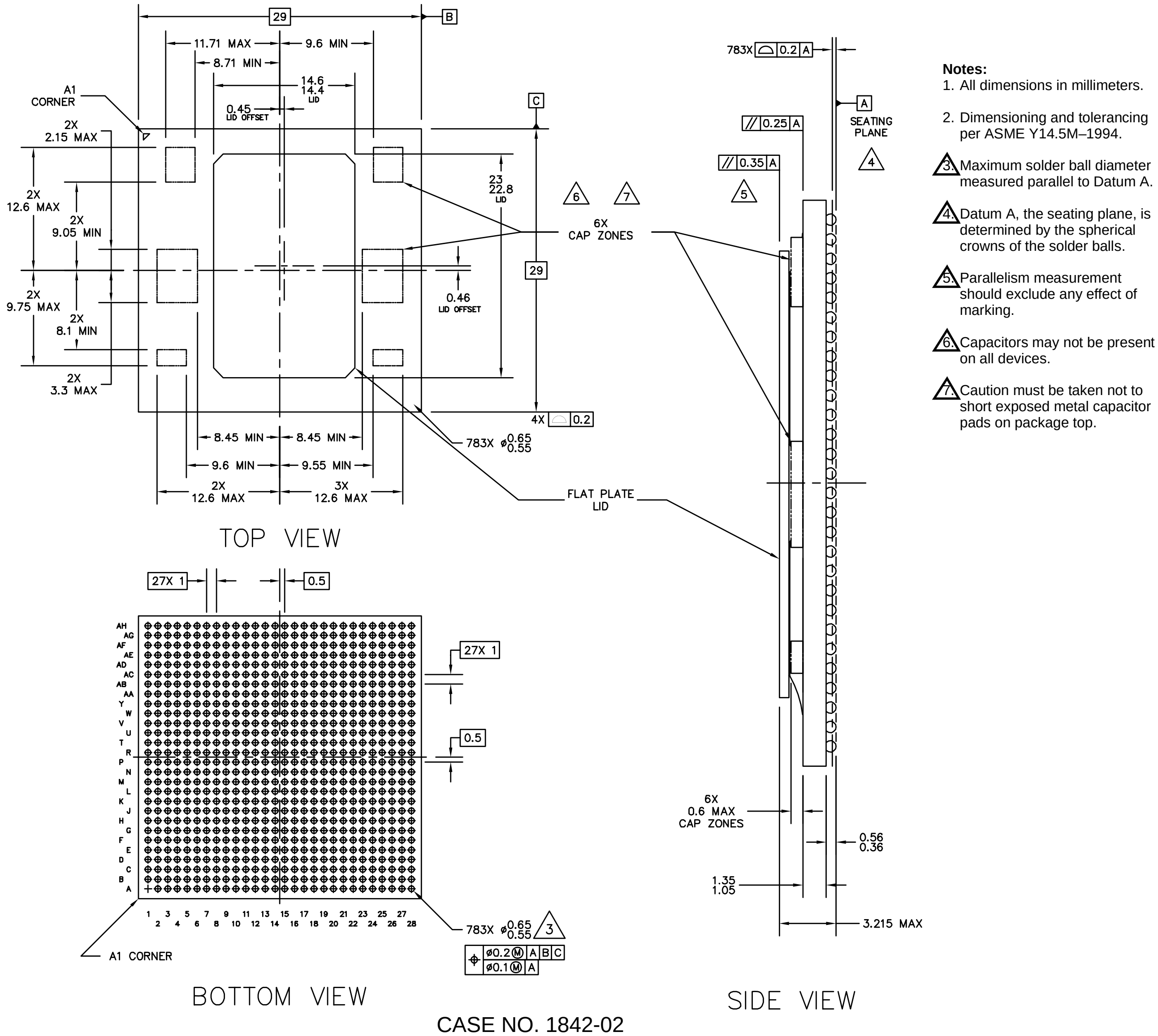


Figure 47. MSC8144 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144 Technical Data Sheet* (MSC8144). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144 device.
- *MSC8144 Reference Manual* (MSC8144RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8144 device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 69 provides a revision history for this data sheet.

Table 69. Document Revision History

Revision	Date	Description
0	Feb. 2007	• Initial public release.
1	Apr. 2007	• Adds new I/O multiplexing mode 7 that supports POS functionality. • Updates reference voltage supply for pins G5, H7, and H8 in Table 1. • Updates start-up timing recommendations with regard to $\overline{\text{TRST}}$ and $\overline{\text{M3\_RESET}}$ in Section 2.7.1. • Adds input clock duty cycles in Table 20. • Updates PCI AC timings in Table 38. • Removes UTOPIA internal clock specifications in Table 49. • Updates JTAG timings in Table 53. • Clarifies connectivity guidelines for Ethernet pins in Section 3.3.4. • Miscellaneous pin connectivity guidelines were updated in Table 68. • Updates name of core subsystem reference manual.

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