MSC2320A-xxYS9

262,144 Word BY 36 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2320A-xxYS9 is a fully decoded, 262,144 word × 36 bit CMOS dynamic random access memory composed of eight 1Mb DRAMs in SOJ (MSM514256AJS) and four 256 Kb DRAMs in PLCC (MSM51C256JS). The mounting of eight SOJs and four PLCCs together with twelve 0.2 μF decoupling capacitors on a 72 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2320A-xxYS9 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

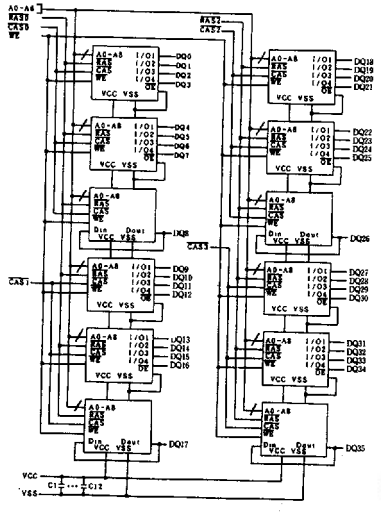
FEATURES

- 262,144 word × 36 bit organization
- JEDEC Compatible Dimensioning
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2320A-80YS9	80ns	40ns	20ns	160ns	4410mW	95mW (MOS level)
MSC2320A-10YS9	100ns	50ns	25ns	190ns	3780mW	

- Single + 5V supply, ±5% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh, and fast page mode capability
- Fast access and cycle times

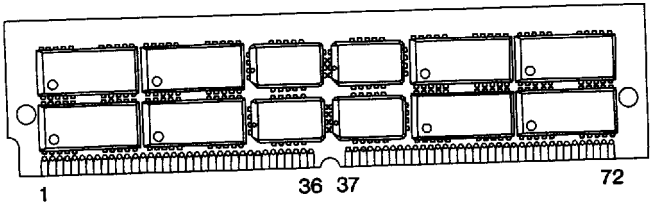
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

MSC2320A-xxYS9

TOP



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	VSS	16	A4	31	A8	46	NC	61	DQ14
2	DQ0	17	A5	32	NC	47	$\overline{WE}$	62	DQ33
3	DQ18	18	A6	33	NC	48	NC	63	DQ15
4	DQ1	19	NC	34	$\overline{RAS2}$	49	DQ9	64	DQ34
5	DQ19	20	DQ4	35	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	NC
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD0
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD1
9	DQ21	24	DQ6	39	VSS	54	DQ29	69	PD2
10	VCC	25	DQ24	40	$\overline{CAS0}$	55	DQ12	70	PD3
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ30	71	NC
12	A0	27	DQ25	42	$\overline{CAS3}$	57	DQ13	72	VSS
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	NC	44	$\overline{RAS0}$	59	VCC		
15	A3	30	VCC	45	NC	60	DQ32		

Pin No.	Pin Name	MSC2320A-80YS9	MSC2320A-10YS9
67	PD0	VSS	VSS
68	PD1	N.C.	N.C.
69	PD2	N.C.	VSS
70	PD3	VSS	VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	12	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.25	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±5%, Ta=0~+70°C)

Parameter	Symbol	Condition		MSC2320A-80YS9 Min.	MSC2320A-80YS9 Max.	MSC2320A-10YS9 Min.	MSC2320A-10YS9 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.25V : All other pins not under test=0V		−120	120	−120	120	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.25V		−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA		2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA		—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS0}$, $\overline{RAS2}$ cycling, $\overline{CAS0}$−$\overline{CAS3}$ cycling, t_{RC}=min		—	840	—	720	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS0}$, $\overline{RAS2}$=V_{IH} $\overline{CAS0}$−$\overline{CAS3}$=V_{IH}	TTL	—	30	—	30	mA	
			MOS	—	18	—	18	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS0}$, $\overline{RAS2}$ cycling, $\overline{CAS0}$−$\overline{CAS3}$=V_{IH} t_{RC}=min		—	840	—	720	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.		—	840	—	720	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS0}$, $\overline{RAS2}$=V_{IL}, $\overline{CAS0}$−$\overline{CAS3}$ cycling t_{PC}=min.		—	680	—	620	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(V_{CC}=5V±5%, f=1MHz, Ta=0~+70°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 — A8)	C_{IN1}	—	88	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	—	104	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN3}	—	57	pF
Input Capacitance ($\overline{CAS0}$—$\overline{CAS3}$)	C_{IN4}	—	36	pF
I/O Capacitance (DQ0—7, 9—16, 18—25, 27—34)	CDQ_1	—	17	pF
I/O Capacitance (DQ8, 17, 26, 35)	CDQ_2	—	22	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

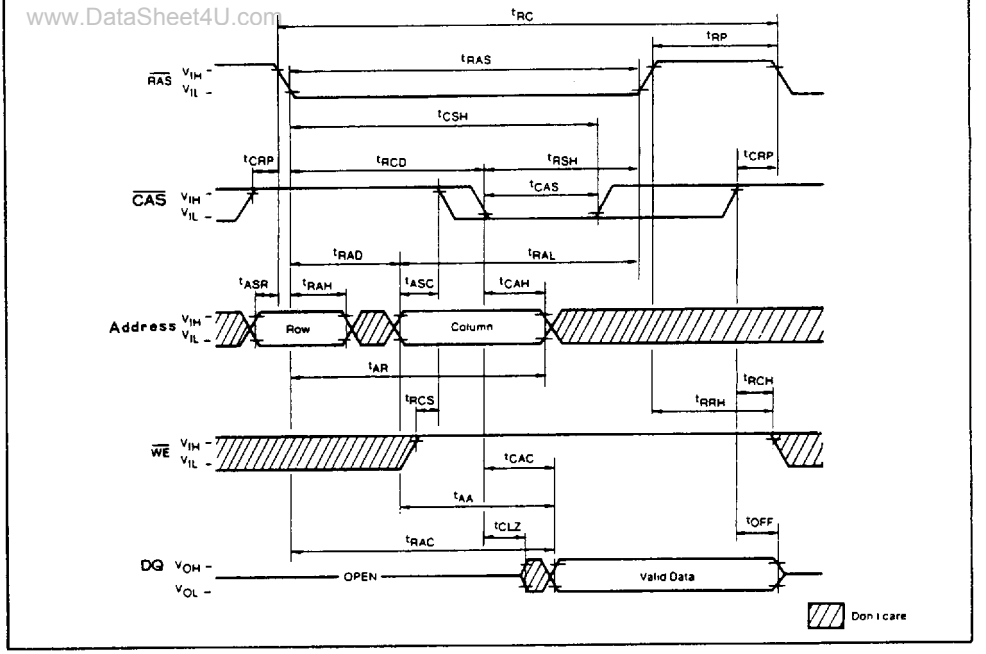
(V_{CC} = 5V ± 5%, Ta = 0 ~ +70°C)

Parameter	Symbol	MSC2320A-80YS9		MSC2320A-10YS9		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	2, 7
Access time from column address	t_{AA}	—	40	—	50	ns	2, 8
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	45	—	50	ns	2
$\overline{CAS}$ to output in Lo-Z	t_{CLZ}	0	—	0	—	ns	2
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	3
Transition time (Rise and Fall)	t_T	3	50	3	50	ns	1
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	7
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	8
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	ns	
Column address hold time refer. to $\overline{RAS}$	t_{AR}	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	ns	
Read command set-up	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	4
Read command hold time refer. to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	4
Write command hold time	t_{WCH}	15	—	20	—	ns	
Write command hold time refer. to $\overline{RAS}$	t_{WCR}	65	—	75	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	ns	
Date set-up time	t_{DS}	0	—	0	—	ns	5
Date hold time	t_{DH}	15	—	20	—	ns	5
Date hold time referenced to $\overline{RAS}$	t_{DHR}	65	—	75	—	ns	
Refresh period	t_{REF}	—	8	—	8	ms	
Write command set-up time	t_{WCS}	0	—	0	—	ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CHR}	30	—	30	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	ns	

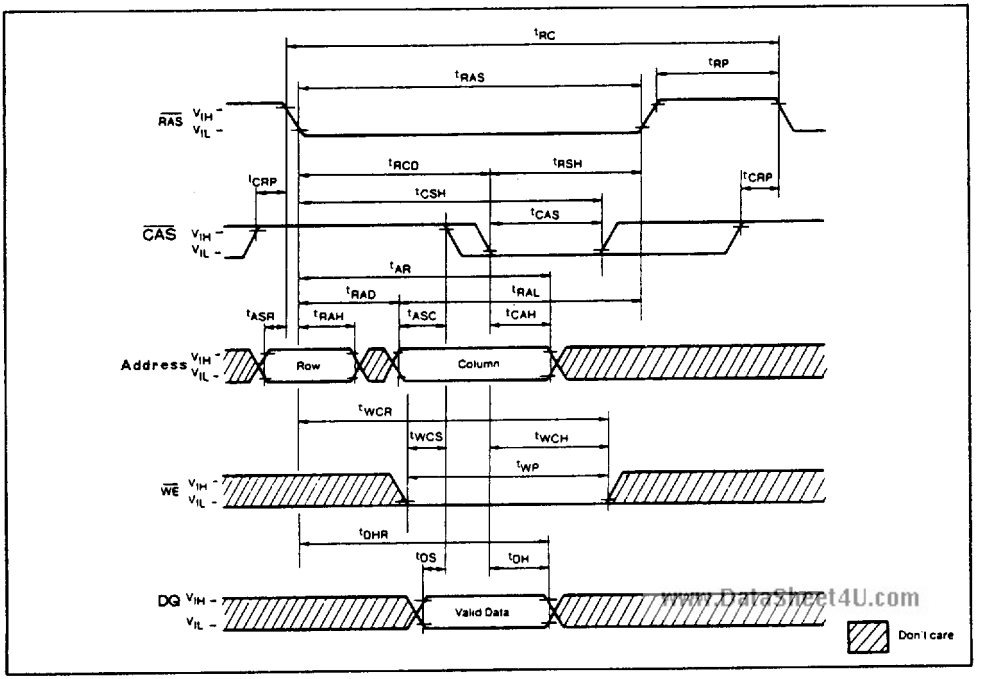
NOTES :

1) AC measurements assume t_T =5ns.
2) Measured with a load equivalent to 2 TTL loads and 100pf.
3) t_{OFF} (max) defines the time at which the output achieves an open circuit condition.
4) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5) These paramenters are referenced to $\overline{CAS}$ leading edge.
6) t_{WCS} is not a restictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is and early write cycle and the data out pin will remain as open circuit (Hi-Z)
7) Operation within the t_{RCD} (max) limit, insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only : if t_{RCD} is greater than the specified t_{RCD} (max) limit, them access time is controlled by t_{CAC}.
8) Operation within the t_{RAD} (max) limit, insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only : if t_{RAD} is greater than the specified t_{RAD} (max) limit, them access time is controlled by t_{AA}.

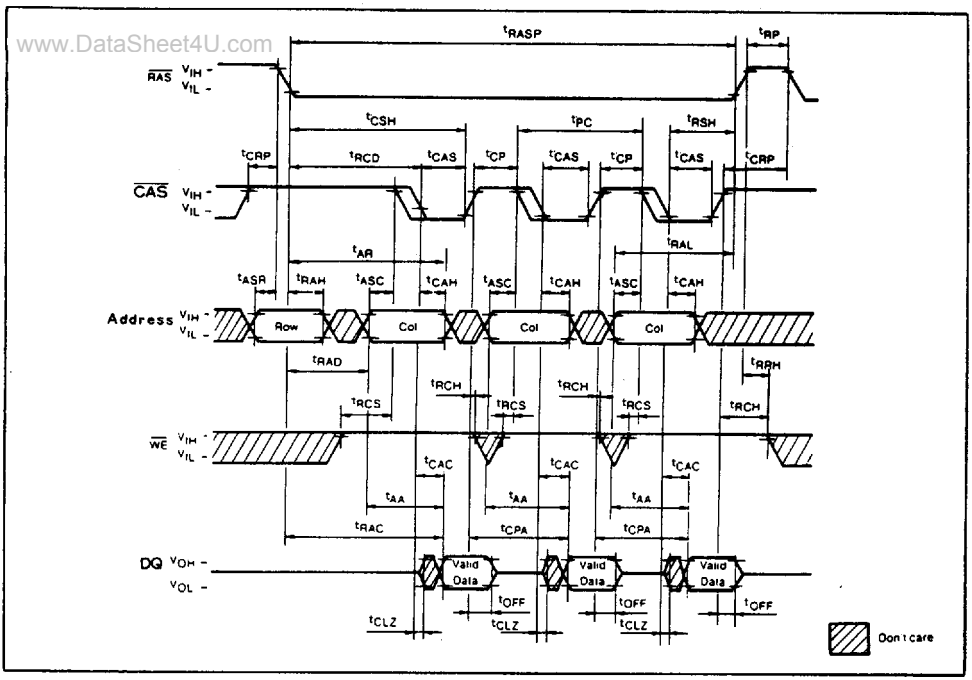
● READ CYCLE



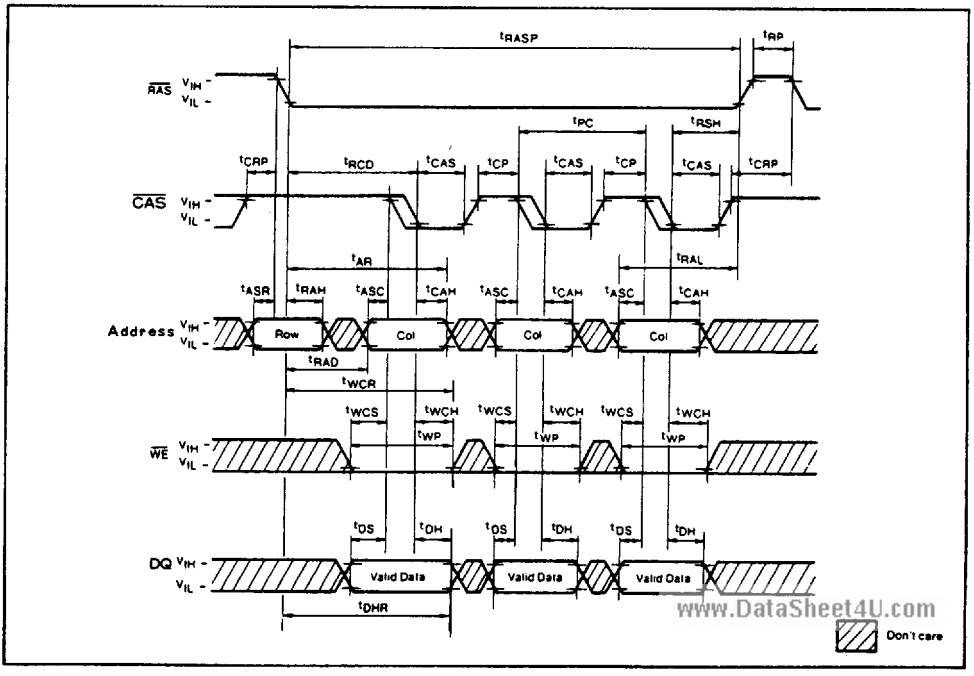
● WRITE CYCLE (EARLY WRITE)



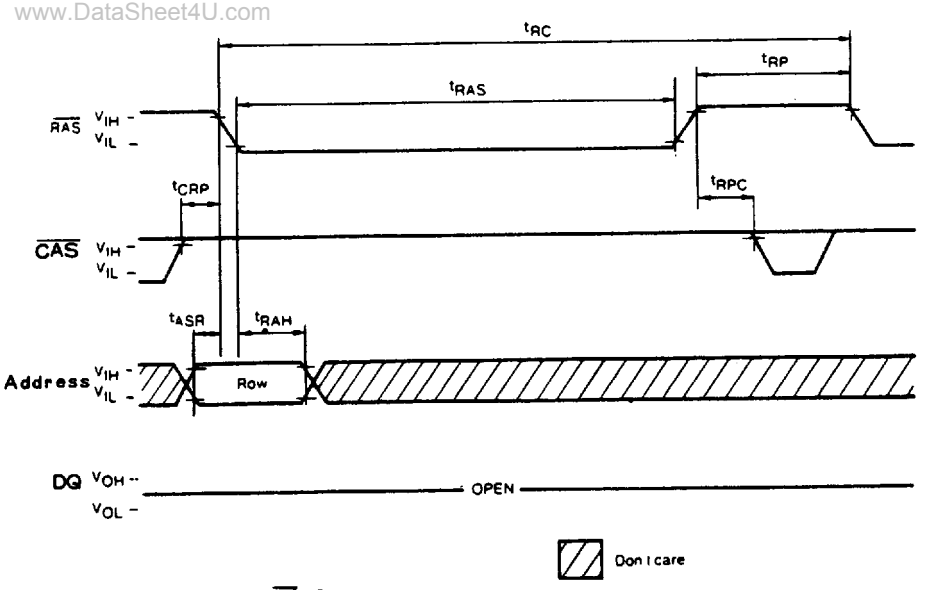
● FAST PAGE MODE READ CYCLE



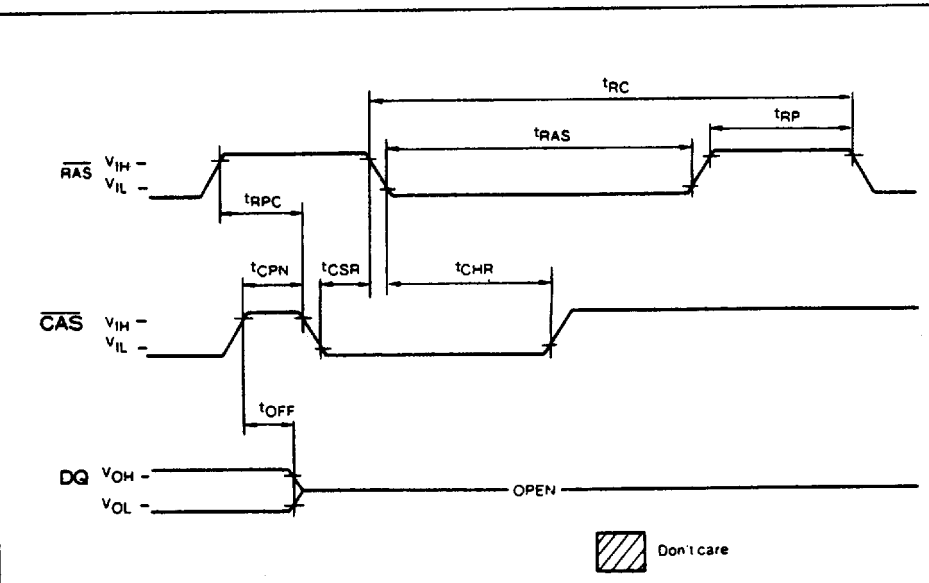
● FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



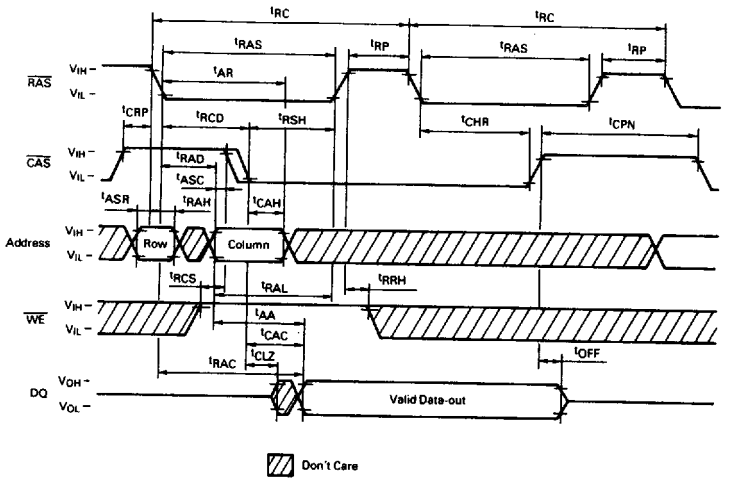
● $\overline{RAS}$ ONLY REFRESH CYCLE



● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



● HIDDEN REFRESH READ CYCLE



● HIDDEN REFRESH WRITE CYCLE