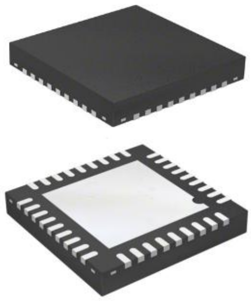
Glucometer Analog AFE

PRODUCT DESCRIPTION

The MS9912N is a glucometer analog AFE measurement chip, which integrates high-performance ADC, high-precision operational amplifier, low-impedance switch, high-precision reference voltage generating circuit and glucose test AC signal circuit. It also integrates I^2C communication protocol. These features make peripherals much less and users just need to operate and read data via interface, thus completing glucose acquisition.

The operating voltage ranges from 2.5V to 3.6V. The temperature range is from -40°C to +85°C. And the MS9912N is available in a QFN36 package.



QFN36

FEATURES

- Maximum 16bit No Missing Codes
- ADC INL : 0.01%
- Integrated Oscillator
- Continuous Conversion and Single Conversion
- Integrated Low Offset Operational Amplifier
- Optional Internal and External References
- I^2C Interface
- Low Power Dissipation : 1400µA
- QFN36 Package (Back Thermal Pad)

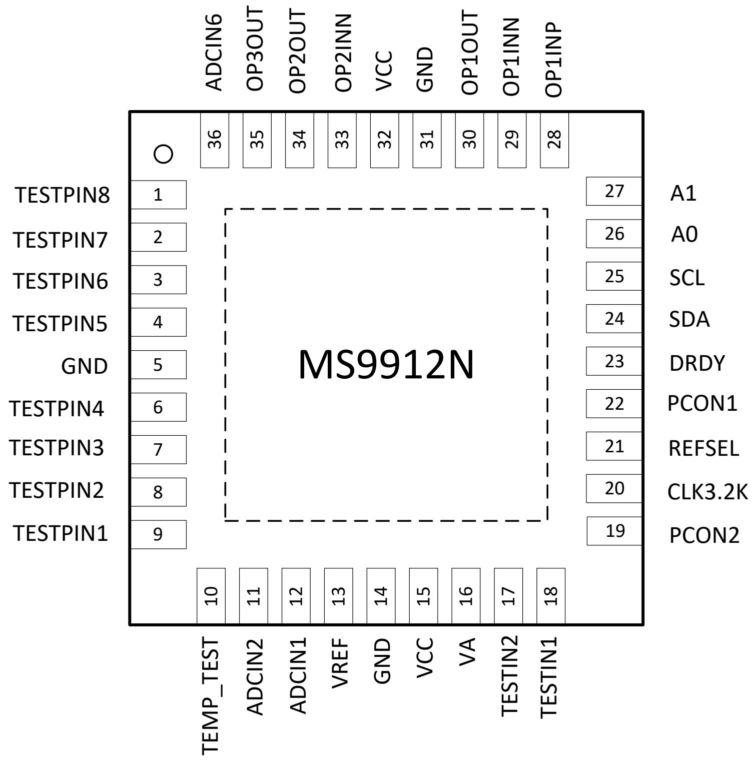
APPLICATIONS

- Glucose Measurement
- Industry Measurement

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS9912N	QFN36	MS9912N

PIN CONFIGURATION

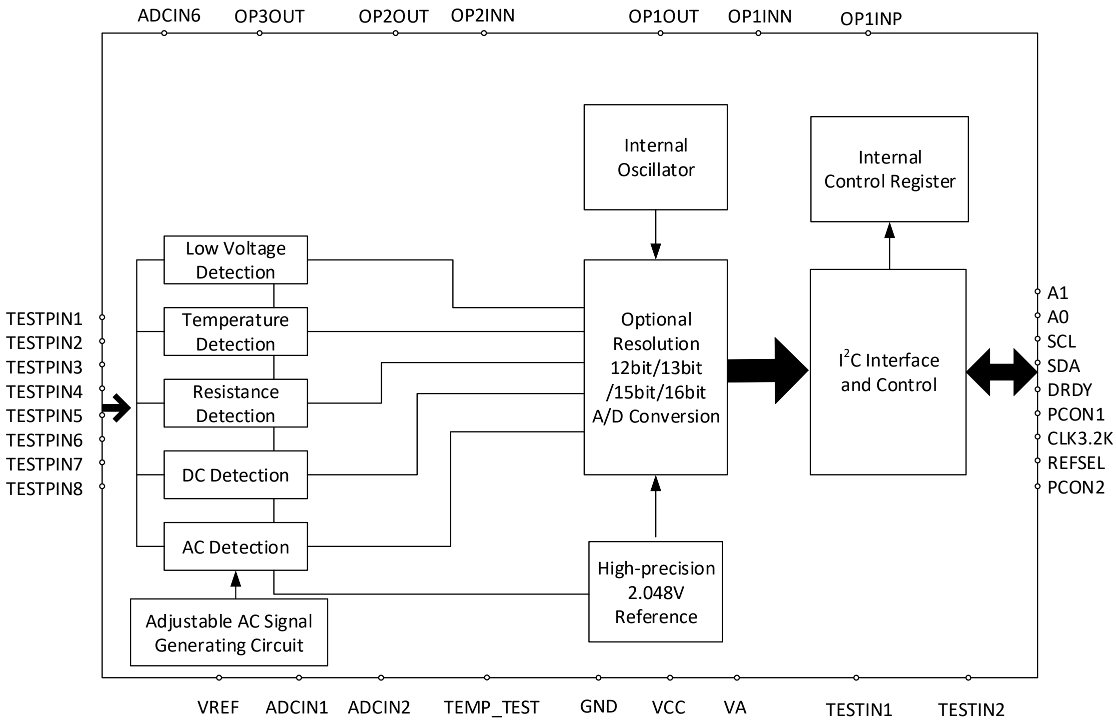


PIN DESCRIPTION

Pin	Name	Type	Description
1	TESTPIN8	I	Test Terminal 8. By register setting and peripherals, the resistance value between TESTPIN8 and TESTPIN7 can be measured
2	TESTPIN7	I/O	AC Small Signal Output and Resistor Test Terminal. By register setting and peripherals, the resistance value between TESTPIN7 and TESTPIN2, TESTPIN4, TESTPIN6, TESTPIN8 can be measured
3	TESTPIN6	I	Test Terminal 6. By register setting and peripherals, the resistance value between TESTPIN6 and TESTPIN7 can be measured
4	TESTPIN5	I	Current Test Terminal 5. By register setting and peripherals, the terminal current can be measured
5	GND	-	Ground
6	TESTPIN4	I	Test Terminal 4. By register setting and peripherals, the resistance value between TESTPIN4 and TESTPIN7 can be measured
7	TESTPIN3	I	Test Terminal 3. By register setting and peripherals, the resistance value between TESTPIN2 and TESTPIN3 can be measured
8	TESTPIN2	I	Test Terminal 2. By register setting and peripherals, the resistance value between TESTPIN2 and TESTPIN3 can be measured
9	TESTPIN1	I	AC Test Terminal. By register setting and peripherals, the peak value of AC signal can be measured
10	TEMP_TEST	I	Temperature Test Input, external shunt resistor and thermistor
11	ADCIN2	I	ADC Input Terminal 2
12	ADCIN1	I	ADC Input Terminal 1
13	VREF	I/O	2.048V Reference Voltage Input/Output
14	GND	-	Ground
15	VCC	I/O	Internal Voltage Decouple Terminal, external 10μF capacitor
16	VA	-	Power Supply
17	TESTIN2	I	Internal Test Terminal 2
18	TESTIN1	I	Internal Test Terminal 1
19	PCON2	I	Internal Power Switch Control Terminal, Active Low
20	CLK3.2K	I	3.2kHz Square Wave Signal Input
21	REFSEL	I	Reference Voltage Select Terminal. Low selecting external reference; High selecting internal reference

Pin	Name	Type	Description
22	PCON1	O	Output low level after detecting test paper inserted
23	DRDY	O	Output pulse after one conversion
24	SDA	I/O	I^2C SDA Signal
25	SCL	I	I^2C Clock Signal
26	A0	I	Address Select 0
27	A1	I	Address Select 1
28	OP1INP	I	Positive Input Terminal for Amplifier 1
29	OP1INN	I	Negative Input Terminal for Amplifier 1
30	OP1OUT	I/O	Output for Amplifier 1
31	GND	-	Ground
32	VCC	-	Power Decouple Pin, external capacitor
33	OP2INN	I	Negative Input Terminal for Amplifier 2
34	OP2OUT	I/O	Output for Amplifier 2
35	OP3OUT	O	Output for Amplifier 3, external detection capacitor
36	ADCIN6	O	Detection Output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn’t represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VA	-0.3 ~ +6.0	V
Operating Temperature	TA	-40 ~ +85	°C
Storage Temperature	Tstg	-60 ~ +150	°C
ESD	HBM	>±3k	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Norm	Max	
Power Supply	VA	2.5	3.3	3.6	V
Operating Temperature	TA	-40		85	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, TA=25°C, VA=3.3V.

Parameter	Condition	Min	Typ	Max	Unit
Reference					
Reference Output Voltage		2.043	2.048	2.053	V
System Performance					
Resolution and No Missing Codes	DR=00	12		12	Bits
	DR=01	13		13	Bits
	DR=10	15		15	Bits
	DR=11	16		16	Bits
Output Rate	DR=00		480		SPS
	DR=01		240		SPS
	DR=10		60		SPS
	DR=11		30		SPS
Integral Nonlinearity	DR=11, PGA=1, End Point		±0.004	±0.010	% of FSR
Offset Error	PGA=1		3.9	8	mV
	PGA=2		3.8	5	mV
	PGA=4		3.8	4.5	mV
	PGA=8		3.5	4.5	mV
Amplifier Performance					
Input Offset Voltage	-0.3V<VCM<+3.5V		0.4	1	mV
	-40°C≤TA≤85°C			1	
Input Bias Current	25°C		0.2	1	pA
	-40°C≤TA≤85°C			780	pA
Input Offset Current	25°C		0.1	0.5	pA
	-40°C≤TA≤85°C			50	pA
Common-mode Rejection Ratio	0V<VCM<+3.5V		75		dB
	-40°C≤TA≤85°C	68			
Large Signal Gain	RL=10kΩ, Vo=0.5V~2.8V	100	105		dB
Input Offset Voltage Drift	-40°C≤TA≤85°C		5	10	μV/°C
Input Capacitance	Cdiff		1.9		pF
	Ccm		2.5		pF
Output High	I_L=1mA	3.25	3.26		V
	-40°C≤TA≤85°C	3.2			
	I_L=10mA		3.1		V
	-40°C≤TA≤85°C	2.9			

Parameter	Condition	Min	Typ	Max	Unit
Output Low	I_L=1mA		20	30	mV
	-40°C≤TA≤85°C			50	
	I_L=10mA		190	275	mV
	-40°C≤TA≤85°C			335	
Output Short-circuit Current			±80		mA
Closed-loop Output Impedance	f=10kHz, AV=1		15		Ω
Power Supply Rejection Ratio	1.8V<VCM<+3.5V	67	90		dB
	-40°C≤TA≤85°C	64			dB
Static Current	Vo=VA/2		40		µA
	-40°C≤TA≤85°C			50	
Gain Bandwidth Product	R_L=100kΩ		0.4		MHz
	R_L=10kΩ		0.4		MHz
Slew Rate	R_L=10kΩ		0.3		V/µs
Setup Time 0.1%	G=±1,2Vstep, C_L=20pF,R_L=1kΩ		23		µs
Phase Margin	R_L=100kΩ,R_L=10kΩ,C_L=20pF		65		Deg
Peak-to-Peak Noise			2.3	3.5	µV
Voltage Noise Density	f=1kHz		26		$nV/\sqrt{Hz}$
	f=10kHz		24		$nV/\sqrt{Hz}$
Current Noise Density	f=1kHz		0.05		$pA/\sqrt{Hz}$
Digital input/Output					
Input High Level		0.7·VA		3.6	V
Input Low Level		GND-0.5		0.3×VA	V
Output Low Level	I_{OL}=3mA	GND		0.4	V
Input High Peak Current				10	µA
Input Low Peak Current		-10			µA
Power Performance					
Operating Voltage	VA	2.5		3.6	V
Power Supply Current	Off-state		0.05	2	µA
	Operation state		1400	1600	µA

FUNCTION DESCRIPTION

The MS9912N integrates high-performance ADC, high-precision operational amplifier, low-impedance switch, high-precision reference voltage generating circuit and glucose AC signal test circuit, and also integrates I^{2}C communication protocol.

ADC

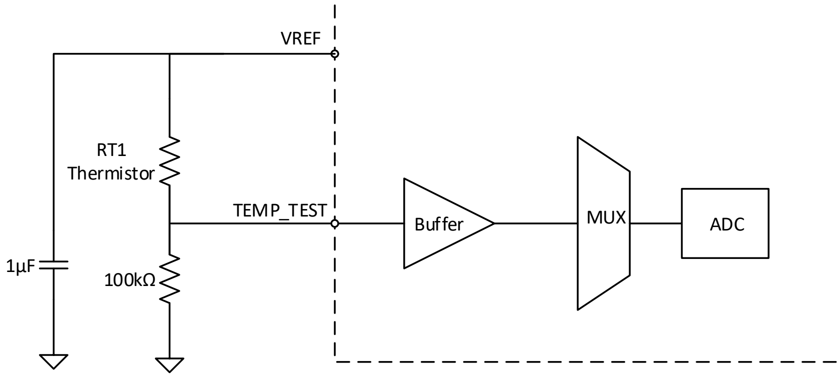
The analog-to-digital converter consists of a switched-capacitor Σ-Δ modulator and a digital filter. The modulator measures analog input voltage and outputs digital stream. The digital filter receives high-speed bit stream from the modulator and converts to digital code, which is a number proportional to input voltage.

Low Voltage Detection

The MS9912N judges whether power supply is in low voltage state, by detecting the value after divided the internal power supply.

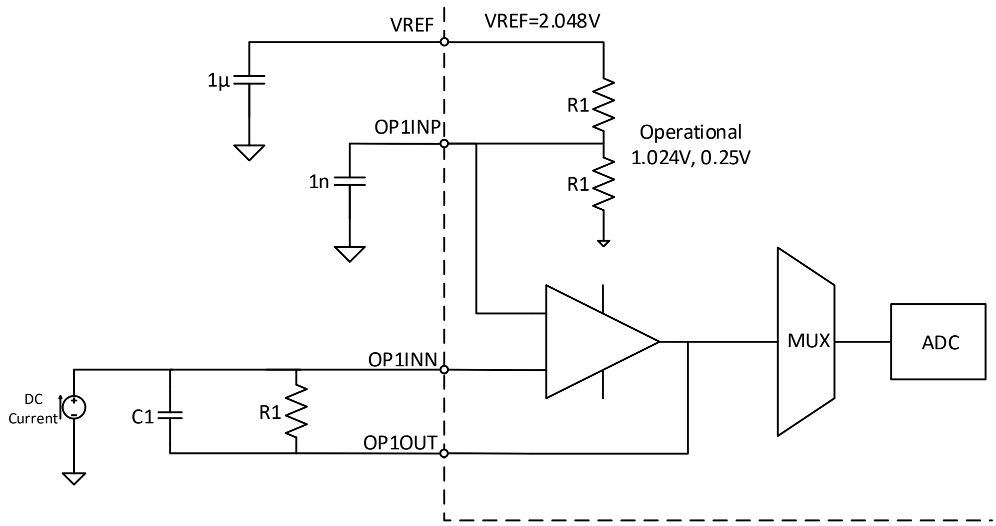
Temperature Detection

The voltage divided by peripheral thermistor is input to ADC test channel via internal buffer, so as to detect ambient temperature. The test principle is as follows:



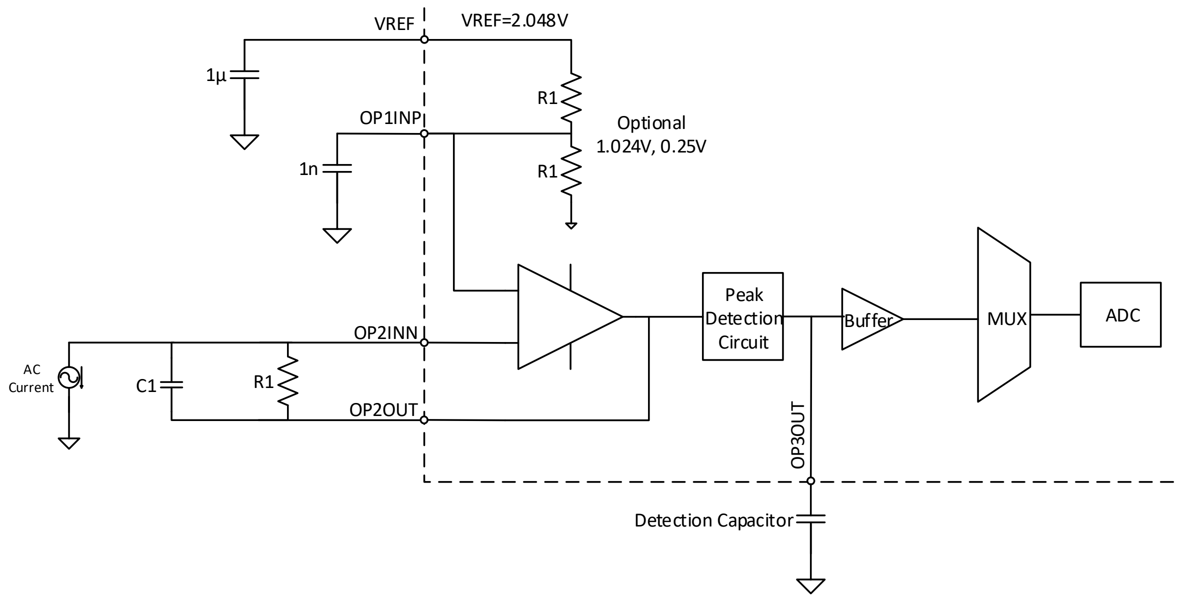
DC Current Detection Channel

The MS9912N integrates DC detection channel. External current signal is converted by current-voltage and amplified, then input to ADC to convert as digital signal. The test principle is as follows:

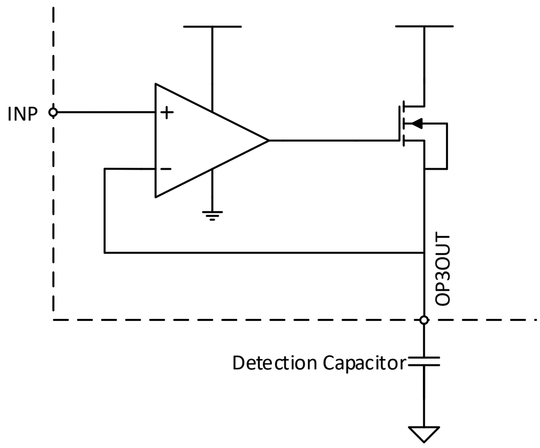


AC Detection Channel

The MS9912N integrates AC detection channel. External current signal is converted by current-voltage and amplified, then input to ADC to convert as digital signal. The test principle is as follows:



Peak detection circuit is as follows:



Voltage Reference

The MS9912N integrates a 2.048V on-chip voltage reference, which is used as the voltage reference of amplifier and ADC. The reference voltage of amplifier can also be connected externally. ADC can only use internal voltage reference.

Output Code Calculation

The output code is a scaled value that is proportional to the voltage on analog input when input is in full-scale range. The output code is confined to a finite numbers range. And the range depends on the number of bits needed to represent the code, which of the ADC is decided by the data rate, as shown in Table 1.

Table 1. Output Code

Data Rate	Number Of Bits	Output Code
30SPS	16	32767
60SPS	15	16383
240SPS	13	4095
480SPS	12	2047

The format of ADC output code is binary two's complement.

Clock Oscillator

The MS9912N integrates clock oscillator, which drives the operation of the modulator and digital filter.

Operation Mode

The MS9912N includes two operation modes: continuous conversion or single conversion.

In continuous conversion mode, once a conversion has been completed, the MS9912N immediately places the result in the output register and begins another conversion.

In single conversion mode, the MS9912N waits until the ST/DRDY bit in the configuration register is set as 1. After the conversion is completed, the MS9912N places the result in the output register, resets the ST/DRDY bit to 0 and powers down. While a conversion is in progress, writing 1 to ST/DRDY has no effect.

When switched from continuous conversion mode to single conversion mode, the MS9912N completes the current conversion, resets the ST/DRDY bit to 0 and powers down.

Reset and Power-up

When the MS9912N powers up, it automatically performs one reset. The MS9912N sets all of the bits as default settings.

I²C Interface

The MS9912N interface adopts I²C communication protocol. I²C interface is a two-wire open drain output interface, which supports several devices share one bus with master. Devices on the I²C bus only drive the bus low by connecting them to ground, and they can't drive the bus high. Thus, the bus is pulled high by pull-up resistors.

Communication on the I²C bus usually takes place between two devices, one acting as the master and the other as the slave. The MS9912N can only act as a slave device.

The timing diagram for the MS9912N I²C is shown in Figure 1. The related parameters for this diagram are given in Table 2.

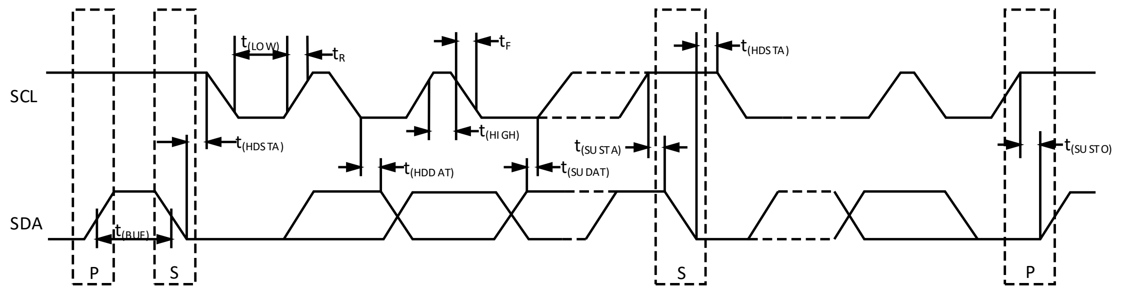


Figure 1. I²C Timing Diagram

Table 2. Related Parameters for Timing Diagram

Parameter		Fast-Speed Mode		High-Speed Mode		Unit
		Min	Max	Min	Max	
$t_{(SCLK)}$	SCLK Operating Frequency		0.4		3.4	MHz
$t_{(BUF)}$	Bus START to STOP Idle Time	600		160		ns
$t_{(HDSTA)}$	START Hold Time	600		160		ns
$t_{(SUSTA)}$	Repeated START Setup Time	600		160		ns
$t_{(SUSTO)}$	STOP Setup Time	600		160		ns
$t_{(HDDAT)}$	Data Hold Time	0		0		ns
$t_{(SUDAT)}$	Data Setup Time	100		10		ns
$t_{(LOW)}$	SCLK Clock Low Level Period	1300		160		ns
$t_{(HIGH)}$	SCLK Clock High Level Period	600		60		ns
t_F	Clock/Data Fall Time		300		160	ns
t_R	Clock/Data Rise Time		300		160	ns

Serial Bus Address

In order to read from and write to the MS9912N, the master must first address to the slave through address bit. The slave address includes three address bits and one operation bit to indicate read or write operation. The MS9912N has two address pins, A0 and A1, setting I^2C address. A0 and A1 could be set as logic ground, logic high or Float. Eight different addresses can be set through the two pins, as shown in table 3.

Table 3. MS9912N Address Pins and Slave Address

A0	A1	Slave Address
0	0	000
0	1	001
0	Float	010
1	0	100
1	1	101
1	Float	110
Float	0	011
Float	1	111
Float	Float	Invalid

Register

The MS9912N registers can are accessible via its I^2C interface. The output register contains the result of the last conversion. The configuration register allows the user to change the operation mode of the MS9912N and query device status.

Output Register

The 16-bit output register contains the result of the last conversion in binary two's complement format. After reset or power-up, the output register is cleared and remains zero until the first conversion is completed. The output register format is shown in Table 4.

Table 4. Output Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Analog-to-Digital Conversion Configuration (Address 90hRegister)

User can use 8-bit configuration register to control the operation mode, data rate and PGA setting. The configuration register format is shown in Table 5. The default setting is 80_H.

Table 5. ADC Configuration Register

Bit	7	6	5	4	3	2	1	0
Name	ST/DRDY	-	-	SC	DR1	DR0	PGA1	PGA0
Default	1	0	0	0	0	0	0	0

Bit 7: ST/DRDY

ST/DRDY bit indicates the data is written to or read from.

In single conversion mode, writing 1 to the ST/DRDY bit indicates starting a conversion, and writing 0 has no effect. In continuous conversion mode, the MS9912N ignores the value written to ST/DRDY. When performing read operation, ST/DRDY indicates whether the data in the output register is new data. If ST/DRDY is 0, the data read from the output register has not been read before. If ST/DRDY is 1, the data has been read before.

In continuous conversion mode, use ST/DRDY to determine when conversion data is ready. If ST/DRDY is 1, the data in the output register has already been read. If ST/DRDY is 0, the data in the output register has not yet been read.

In single conversion mode, use ST/DRDY to determine whether a conversion has completed. If ST/DRDY is 1, the conversion is in process. if it is 0, conversion is completed.

Bit 4: SC

SC bit controls whether the MS9912N operates in continuous or single conversion mode. When SC is 1, the MS9912N operates in single conversion mode. When SC is 0, it operates in continuous conversion mode. The default setting is 0.

Bit 3-2: DR

Bit 3 and 2 control the data rate of the MS9912N, as shown in Table 6.

Table 6. DR Bit

DR1	DR0	Data Rate	Resolution
0[1]	0[1]	480SPS	12Bit
0	1	240SPS	13Bit
1	0	60SPS	15Bit
1	1	30SPS	16Bit

Note 1: Default setting

Bit 1-0: PGA

Bit 1 and 0 control the gain setting of the MS9912N, as shown in Table 7.

Table 7. PGA Bit

PGA1	PGA0	Gain
0[1]	0[1]	1
0	1	2
1	0	4
1	1	8

Note 1: Default setting

Test Control Register (Default 0)

Address A0 Register	bit7	1: Turn on switch from 3.2kHz AC signal to TESTPIN5 (test AC impedance between TESTPIN5 and TESTPIN1); 0: Turn off switch from 3.2kHz AC signal to TESTPIN5
	bit6	1: Turn on switch from ADCIN1 to TESTPIN3 (test resistance between TESTPIN2 and TESTPIN3); 0: Turn off switch from ADCIN1 to TESTPIN3
	bit5	1: Turn on switch from TESTPIN8 to GND (test resistance between TESTPIN8 and TESTPIN7); 0: Turn off switch from TESTPIN8 to GND
	bit4	1: Turn on switch from TESTPIN6 to GND (test resistance between TESTPIN6 and TESTPIN7); 0: Turn off switch from TESTPIN6 to GND
	bit3	1: Turn on switch from TESTPIN3 to GND (detect test paper whether is inserted) 0: Turn off switch from TESTPIN3 to GND
	bit2	1: Turn on switch from TESTPIN5 to OP1INN (test paper DC test); 0: Turn off switch from TESTPIN5 to OP1INN

	bit1	1: Turn on switch from TESTPIN4 to GND (test resistance between TESTPIN4 to TESTPIN7); 0: Turn off switch from TESTPIN4 to GND
	bit0	1: Turn on switch from 3.2kHz AC signal to TESTPIN7 (test AC impedance between TESTPIN7 to TESTPIN1); 0: Turn off switch from 3.2kHz AC signal to TESTPIN7
Address B0 Register	bit7	1: Turn on switch from ADCIN2 to TESTPIN7 (test resistance between TESTPIN2,4,6,8 to TESTPIN7); 0: Turn off switch from ADCIN2 to TESTPIN7
	bit6	1: Turn on switch from TESTPIN2 to GND (test resistance between TESTPIN2 to TESTPIN7); 0: Turn off switch from TESTPIN2 to GND
	bit5	1: Turn on switch from TESTPIN2 to TOMCU (test test paper whether is inserted) (default); 0: Turn off switch from TESTPIN2 to TOMCU
	bit4	1: Turn on switch from TESTPIN1 to OP2INN (test paper AC test); 0: Turn off switch from TESTPIN1 to OP2INN
	bit3	1: OP1INN input terminal connects 20kΩ resistor to GND (test paper DC test); 0： OP1INN input terminal disconnects 20kΩ resistor to GND
	bit2	1: VREF 1.024V connects 100kΩ resistor to GND (amp bias 0.25V); 0: VREF 1.024V disconnects 100kΩ resistor to GND (amp bias 1.024V)
	bit1	1: OP2INN input terminal connects 240kΩ resistor to GND (backup); 0: OP2INN input terminal disconnects 240kΩ resistor to GND
	bit0	Set 0 at temperature measurement; Must set 1 in other modes
Address C0 Register	bit7	1: Turn on discharge channel of peak detection circuit (discharge resistance is about 1MΩ); 0: Turn off discharge channel of peak detection circuit
	bit6	1: Turn on switch from TESTPIN7 to GND (When test the resistance between TESTPIN 2,4,6,8 and 7); 0: Turn off switch from TESTPIN7 to GND
	bit5 bit4	ADC Input Select: (1) 000: Detect power supply; (2) 001: Detect reference voltage 2.048V; (3) 010: Detect temperature; (4) 011: Detect the resistance between TESTPIN2 and TESTPIN3

	bit3	(5)100: Detect the resistances between TESTPIN2,4,6,8 and TESTPIN7; (6) 101: Test paper DC detect input; (7) 110: Backup; (8) 111: Test paper AC detect input
	bit2	1: Turn on discharge channel of peak detection circuit (discharge resistance is about 750Ω); 0: Turn off discharge channel of peak detection circuit
	bit1	-
	bit0	-

Reading from the MS9912N

To read the contents in the output register and configuration register from the MS9912N, first address the MS9912N, then read three bytes from the device. The first two bytes are the output register's contents, and the third is the configuration register's contents. It is allowed to read less than three bytes during read operation.

The typical timing diagram of the MS9912N read operation is shown in Figure 2.

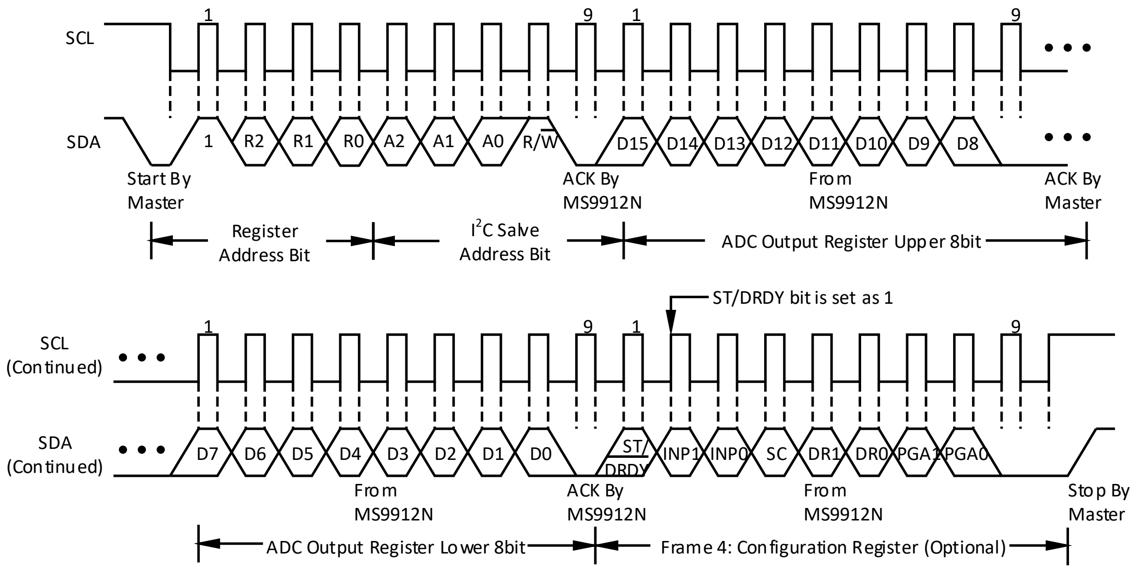


Figure 2. Timing Diagram of the MS9912N Read Operation

Writing to the MS9912N

To write to the configuration register, first address the MS9912N. Note that output register can't be written. Writing more than one byte to the MS9912N has no effect. The MS9912N will ignore any input bytes following the first byte. The typical timing diagram of the MS9912N write operation is shown in Figure 3.

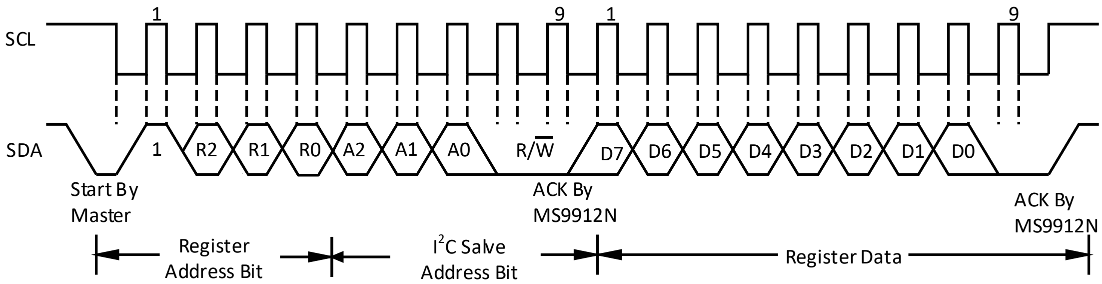


Figure 3. Timing Diagram of the MS9912N Write Operation

Glucose Test Process

The following is the glucose test flowchart:

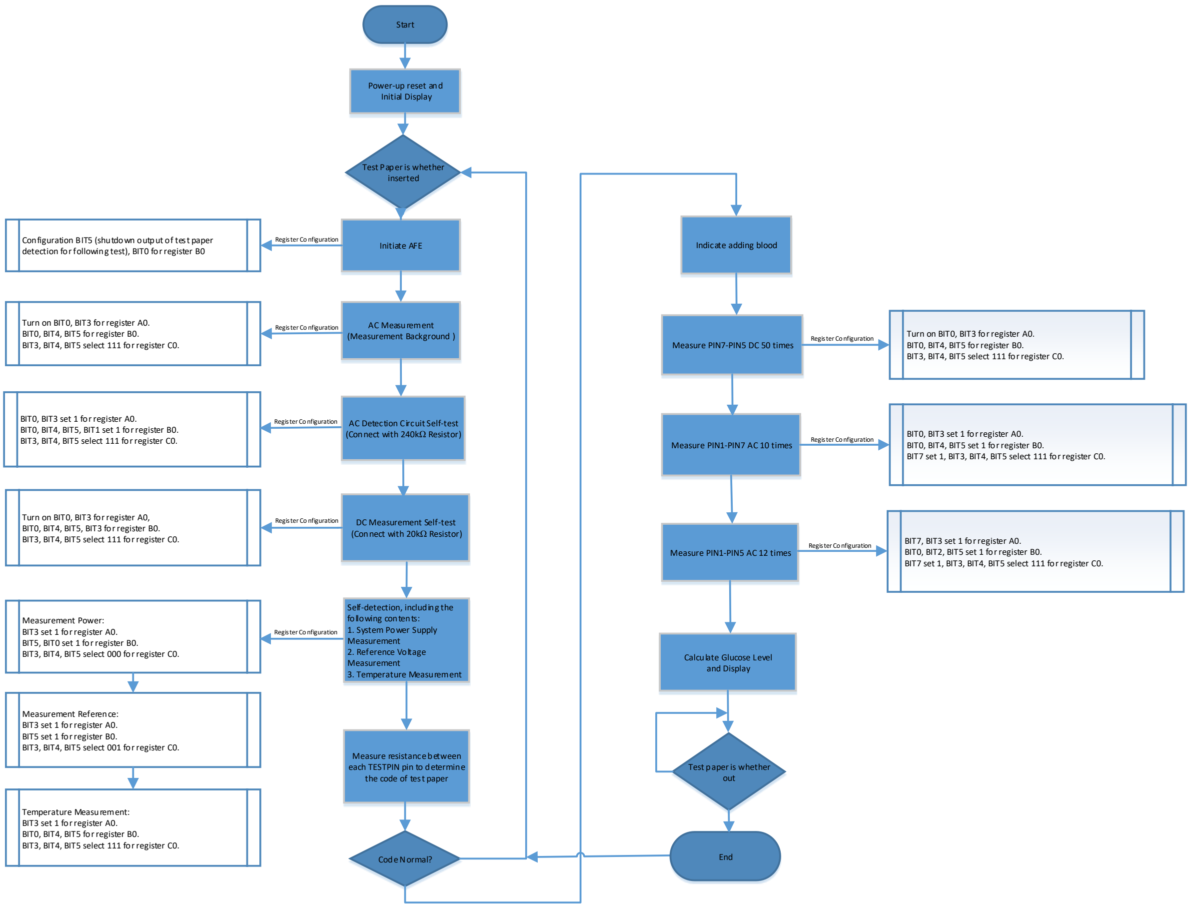
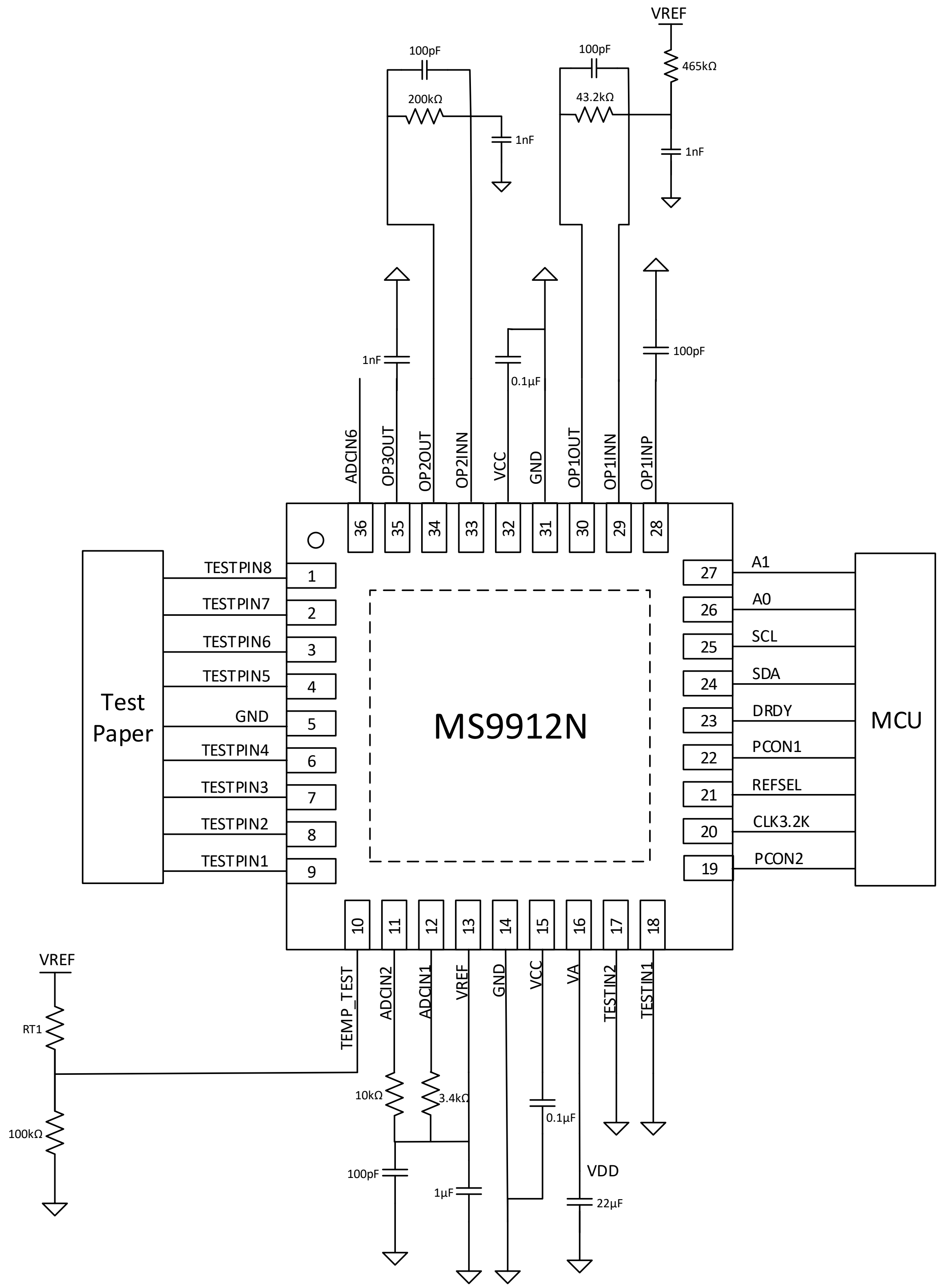


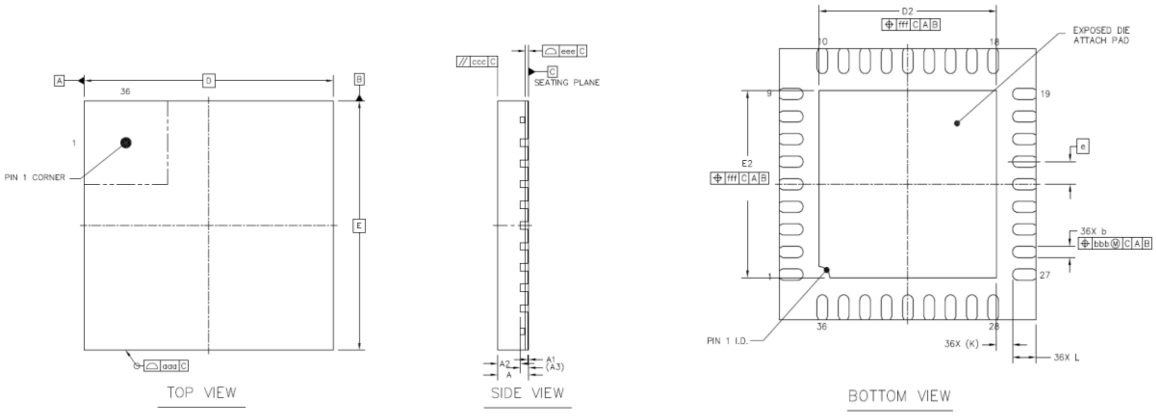
Figure 4. Glucose Test Flowchart

TYPICAL APPLICATION DIAGRAM



PACKAGE OUTLINE DIMENSIONS

QFN36



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.8
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203REF		
b	0.2	0.25	0.3
D	6BSC		
E	6BSC		
e	0.5BSC		
D2	4.05	4.15	4.25
E2	4.05	4.15	4.25
L	0.45	0.55	0.65
k	0.375REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS9912N

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS9912N	QFN36	2000	1	2000	8	16000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don’t release additional notice.
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- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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