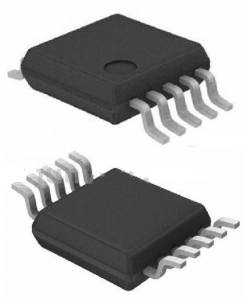
Configurable AFE for Non-Dispersive Infrared Sensor

PRODUCT DESCRIPTION

The MS91050 is a single channel non-dispersive infrared (NDIR) sensor analog front end. The output voltage is directly proportional to thermopile voltage. And the programmable ability can support several thermopile sensors. The MS91050 has programmable gain amplifier, dark phase offset canceling, and adjustable common-mode generator (1.15V or 2.59V), increasing output dynamic range. The MS91050 could realize extra signal filtering (high-pass, low-pass or band-pass) by A0 and A1 pins, in order to eliminate the noise out of band. And the user can program through SPI interface. The operation voltage is from 2.7V to 5.5V.



MSOP10

FEATURES

- Single Channel Input
- Programmable Gain Amplifier
- Dark Phase Offset Canceling
- Support External Filtering
- Common-mode Generator and 8-bit ADC
- MSOP10 Package

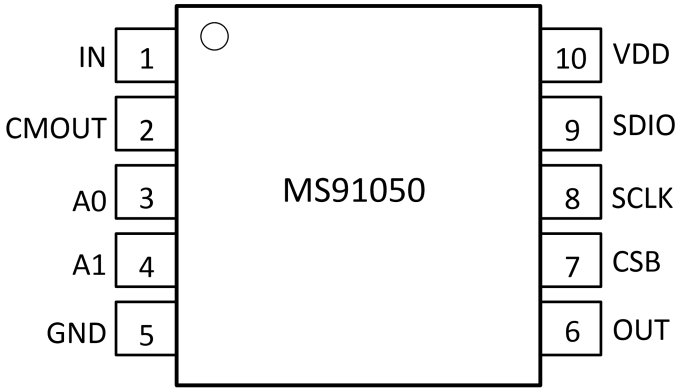
APPLICATIONS

- NDIR Sensor
- Demand Control Ventilation
- Building Monitoring
- Automobile CO_2 Cabin Control
- Automobile Alcohol Detection
- Industry Safety and Insure
- Greenhouse Gases and Freon Detection Platform

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS91050	MSOP10	MS91050

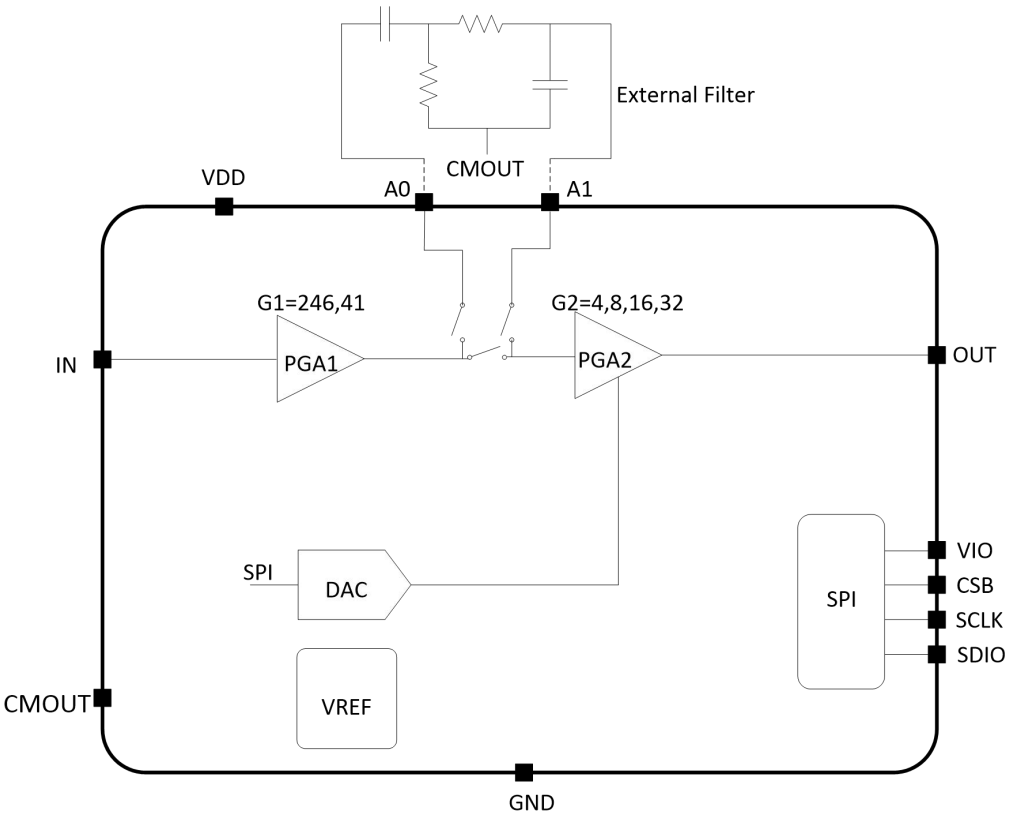
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	IN	I	Analog Input
2	CMOUT	O	Output Common-mode Voltage
3	A0	O	First Stage Analog Output
4	A1	I	Second Stage Analog Input
5	GND	POWER	Ground
6	OUT	O	Output
7	CSB	I	Chip Select, Active Low
8	SCLK	I	Interface Clock
9	SDIO	I/O	Serial Data Input/Output
10	VDD	POWER	Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Ratings	Unit
Power Supply	-0.3 ~ +6.0	V
Pin Voltage	-0.3 ~ VDD+0.3	V
Input Current	5	mA
Storage Temperature	-65 ~ 150	°C
Junction Temperature	150	°C
ESD(HBM)	5000	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Condition	Min	Typ	Max	Unit
Power Supply		2.7		5.5	V
Operation Temperature		-40		125	°C
Package Thermal Resistance ,θ_{JA}	MSOP10 package	95	150	231	°C /W

ELECTRICAL CHARACTERISTICS

VDD=3.3V, VCM=1.15V, unless otherwise noted, $T_A = T_J = 25°C$.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply						
Power Supply	VDD		2.7	3.3	5.5	V
Power Supply Current	IDD	All analog modules open	3.1	3.9	4.2	mA
Shutdown Power Supply Current		All analog modules closed	45	75	121	μA
Digital Power Supply Current				8		μA
Offset Voltage Cancellation (Offset DAC)						
Conversion Rate				256		step
Least Significant Bit	LSB	All gains		33.8		mV
Differential Non-linearity	DNL		-1		+2	LSB
Error		Output offset error, all gains		±100		mV
Offset Range		Reference output, all gains	0.2		VDD-0.2	V
Setup Time				480		μs
Programmable Gain Amplifier PGA1, R_L=10kΩ, C_L =15pF						
Bias Current	IBIAS	T_A =25°C		5	20	pA
		T_A =-40°C~125°C			200	
Maximum Input Signal in High Gain Mode	VINMAX _HGM	Referenced to CMOUT, represents the maximum voltage on pin before limiting magnitude, including the thermopile dark voltage and signal voltage.		±2		mV
Maximum Input Signal in Low Gain Mode	VINMAX _LGM			±12		mV
Input Offset Voltage	VOS			-165		μV
High Gain Mode	G_HGM			246		V/V
Low Gain Mode	G_LGM			41		V/V
Gain Error	GE	All gains		2.5		%
Output Voltage	VOUT		0.5		VDD-0.5	V
Phase Delay	PhDly	1mV Input, HGM, measured at VDD/2		6		μs
Phase Delay Change with Temperature	TcPhDly	1mV Input, HGM, measured at VDD/2		416		ns
Small Signal Bandwidth	SSBW	Vin = 1mVpp,Gain = 246		18		kHz
Input Capacitance	Cin			100		pF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Programmable Gain Amplifier PGA2, R_S =1kΩ, C_L =1μF						
Maximum Input Signal	VINMAX	Gain=4		1.65		V
Minimum Input Signal	VINMAN			0.82		V
Gain	G	Programmable gain in four steps	4		32	dB
Gain Error	GE	All gains		2.5		%
Output Voltage	VOUT		0.2		VDD-0.2	V
Phase Delay	PhDly	100mV Input, 35kHz sine signal, gain=8, measured at 1.65V, RL=10kΩ		1		μs
Phase Delay Change with Temperature	TcPhDly	250mV Input, 35kHz sine signal, gain=8, measured at VDD/2		84		ns
Small Signal Bandwidth	SSBW	Gain = 32		360		kHz
Input Capacitance	Cin			5		pF
Output Load Capacitance	CL, OUT	RC in series		1		μF
Output Load Resistance	RL, OUT	RC in series		1		kΩ
PFA1 and PGA2 Combined						
Input Noise Density	en	86kΩ, 5Hz, Gain=7840		30		nV√Hz
Input Reference Integrated Noise		Including current, voltage noises. Output 86kΩ, 0.1-10Hz, Gain=7840		0.1	0.12	μVrms
Gain	GAIN	PGA1 GAIN=41,PGA2 GAIN=4		163		V/V
		PGA1 GAIN=41,PGA2 GAIN=8		327		
		PGA1 GAIN=41,PGA2 GAIN=16		653		
		PGA1 GAIN=41,PGA2 GAIN=32		1303		
		PGA1 GAIN=246,PGA2 GAIN=4		980		
		PGA1 GAIN=246,PGA2 GAIN=8		1960		
		PGA1 GAIN=246,PGA2 GAIN=16		3920		
		PGA1 GAIN=246,PGA2 GAIN=32		7840		
Gain Error	GE	All gains		5		%
Gain Temperature Coefficient [1]	TCCGE	Gain = 163, 327, 653, 1303		6		ppm/°C
		Gain = 980, 1960, 3920, 7840		20		
Power Supply Rejection Ratio	PSRR	DC, 3.0V to 3.6V supply, gain = 980	90	110		dB
Phase Delay	PhDly	1mV Input, gain=980, measured at VDD/2		9		μs

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Phase Delay Change with Temperature [2]	TCPhDly	1mV Input, gain=980, measured at VDD/2		300		ns
Output Offset Voltage Temperature Drift [1]	TCVOS	GAIN=163		70		µV/°C
		GAIN=327		100		
		GAIN=653		160		
		GAIN=1303		290		
		GAIN=980		230		
		GAIN=1960		420		
		GAIN=3920		800		
		GAIN=7840		1550		
Comm-mode Generator						
Comm-mode Voltage	VCM	VDD=3.3V		1.15		V
		VDD=5V		2.59		
Common-mode Voltage Accuracy				2		%
CMOUT Load Capacitance	CLOAD			10		nF

Note :

1. TCCGE and TCVOS are the maximum slopes between -40°C and 25°C, 25°C and 85°C.
2. The phase delay change with temperature is the maximum phase delay between -40°C and +25°C, 25°C and 85°C.

SPI Interface

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Logic Input High Level	V_{IH}		0.7×VDD			V
Logic Input Low Level	V_{IL}				0.8	V
Logic Output High Level	V_{OH}		2.6			V
Logic Output Low Level	V_{OL}				0.4	V
Digital Input Leakage Current	IIH/IIL		-100 -200		100 200	nA

Timing Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Wake-up Time	t_{WU}			1		ms
Continuous Clock Frequency	f_{SCLK}				10	MHz
SCLK High-level Pulse Width	t_{PH}		$0.4/f_{SCLK}$			ns
SCLK Low-level Pulse Width	t_{PL}		$0.4/f_{SCLK}$			ns
CSB Setup Time	t_{CSS}		10			ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CSB Hold Time	t_{CSH}		10			ns
SDI Setup Time before SCLK Rise Edge	t_{SU}		10			ns
SDI Hold Time before SCLK Rise Edge	t_{SH}		10			ns
SDO Disable Time after CSB Rise Edge	t_{DOD1}				45	ns
SDO Disable Time after the 16th of SCLK Rise Edge	t_{DOD2}				45	ns
SDO Enable Time when the 8th of SCLK Fall Edge	t_{DOE}				35	ns
SDO Access Time after SCLK Fall Edge	t_{DOA}				35	ns
SDO Hold Time after SCLK Fall Edge	t_{DOH}		5			ns
SDO Rise Time	t_{DOR}			5		ns
SDO Fall Time	t_{DOF}			5		ns

Timing Diagram

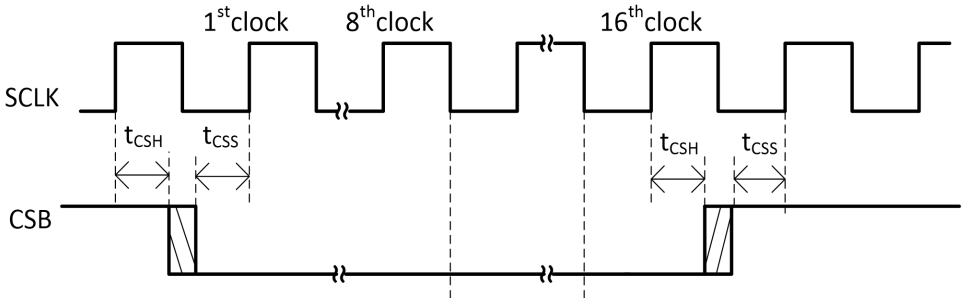


图1. SPI Timing Diagram

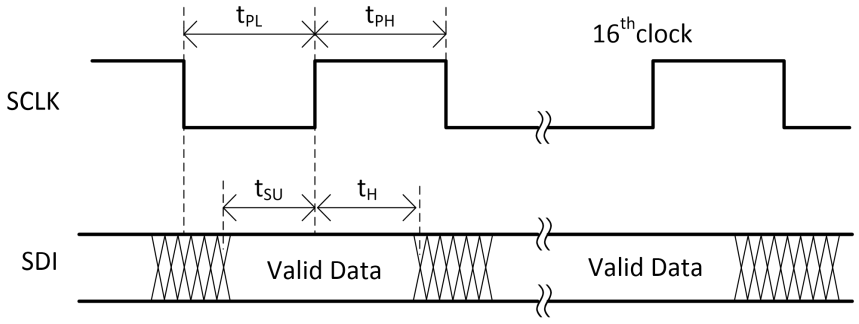


图2. SPI Setup Hold Time

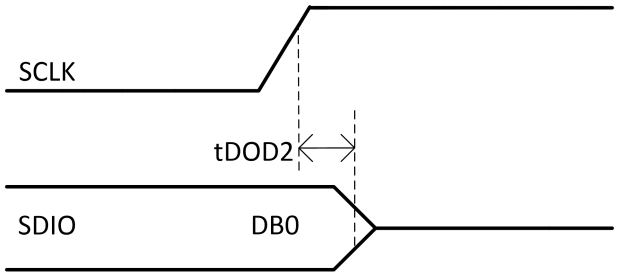


Figure 3. SDO Disable Time after the 16th of SCLK Rise Edge

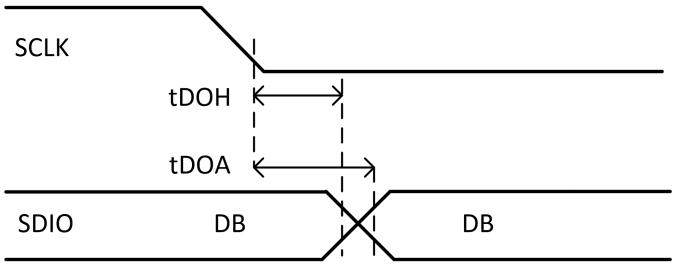


Figure 4. SDO Access Time after SCLK Fall Edge (tDOA)and Hold Time (tDOH)

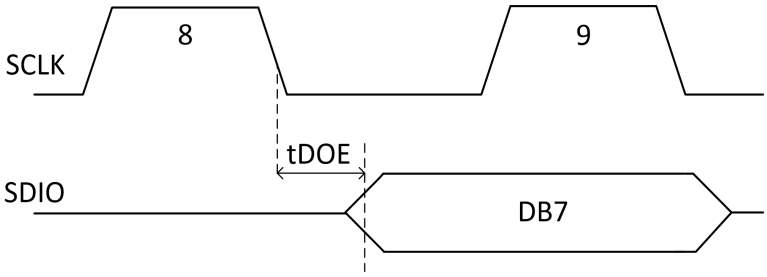


Figure 5. SDO Enable Time when the 8th of SCLK Fall Edge

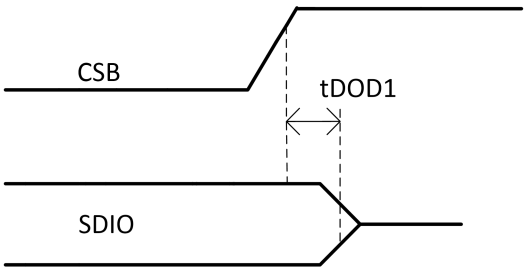


Figure 6. SDO Disable Time after CSB Rise Edge

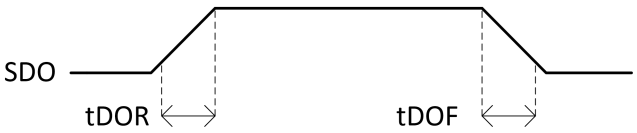


Figure 7. SDO Rise Time and Fall Time

FUNCTION DESCRIPTION

Programmable Gain Amplifier

The MS91050 has two gain modes, in order to make the thermopile having larger dark voltage. All gains are set by GAIN1and GAIN2[1:0]. The low gain range is from 163 to 1303, while high gain range is from 980 to 7840. The PGA needs to refer to VCM generated internally. In high gain mode, the input voltage signal is +/-2mV. In the first stage, the low gain is 41, the high gain is 246, and the the maximum allowable input signal is +/-12mV.

Table 1. Gain Mode

Bit	Gain
GAIN1	0: 246 (default) 1: 41
GAIN2[1:0]	00: 4 (default) 01: 8 10: 16 11: 32

External Filter

The EXT_FILT bit is in the configure register and is programmed through SPI.

Table 2. Measurement Mode

Bit	Measurement Mode
EXT_FILT	0 : Internal PGA processes the signal from the thermopile and don't need extra decoupling and filtering(default)
	1 : The signal from thermopile is processed by PGA of internal first stage and is provided to A0. External low-pass, high-pass, band-pass filter can be connected through A0 and A1.

When EXT_FILT=1, a external filter can be connected. The following diagram is typical band-pass filter, which connect with resistance and capacitance by CMOUT pin. And add discrete components for reference.

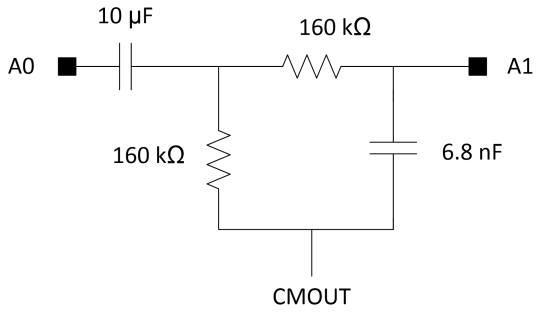


Figure 8. Typical Band-pass Filter

Offset Adjustment Range

The offset adjustment process is as followed. First, measure dark signal, next adjust through DAC, and then measure the residual of dark signal in the second period, in order to further measurement by micro-controller. It's estimated that the the offset component (dark signal) is larger than actual signal. During the dark phase, when the light isn't detected by sensor, the micro-controller could program internal DAC, in order to compensate for the offset. The low output offset varied with temperature (TCVOS) ensures the system accuracy in temperature.

Common-mode Generator

Because the sensor offset is bipolar, VCM voltage is provides to sensor. Here 1.15V or 2.59V is supplied(at 3.3V or 5V power supply). And when powers supply is 3.3V, VCM voltage is 1.15V, prohibit ed from 2.59V.

SPI Interface

The SPI interface could be program the device parameters (such as PGA gains of two stages), enabling external filter and PGA, offset adjustment and controlling comm-mode voltage.

Interface Pin

The serial interface consists of SDIO (serial data I/O), SCLK (serial interface clock) and CSB (chip select). And the default is the writ-only state. SDIO is enable by programming SDIO_MODE_EN, and then read operation is executed. Detailed description is discussed as followed.

CSB

Chip select is active low signal, and is asserted throughout the process. CSB shouldn't generate pulse between instruction byte and data byte of signal mode.

It's noted that if a programme is in process, canceling CSB assertion would finish the programme. Similarly, regardless of the previous finish state, CSB assertion will make the device into a state, ready for next mode.

For 2-wire SPI communication protocol, CSB is connected to low level permanently.

SCLK

SCLK could be idle high-level or low-level for written mode. However, for read mode, SCLK should be idle high-level. SCLK has a feature that input terminal has a schmitt trigger, even though hysteresis exists . It's recommended to clear SCLK to prevent fault from destroying SPI frame.

Communication Protocol

SPI communication protocol includes read and write operations. The write mode consists of single write instruction followed by single data byte. The write mode of SPI serial interface is as followed.

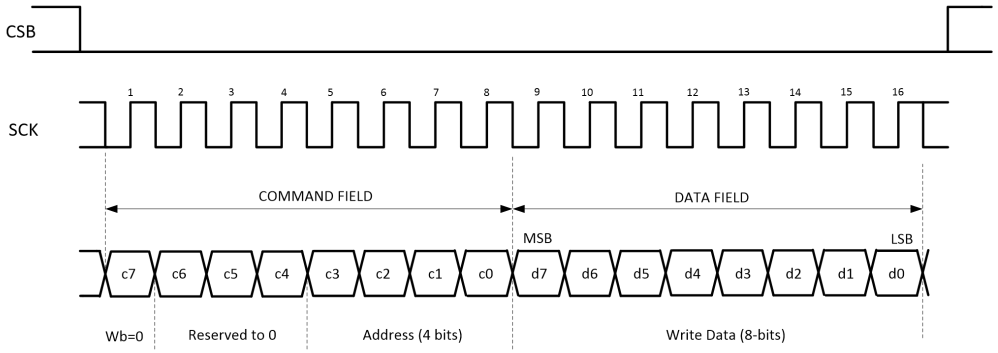


Figure 9. SPI Serial Interface Protocol

For read mode, the user needs to write to SDIO mode enable register to enable read mode. Then in data field of read mode, the data is driven on SDIO terminal. Therefore, SDIO is designed as bidirectional terminal. Read mode is shown in figure 10. In figure 11, SPI master issues the command sequence, which enables read mode.

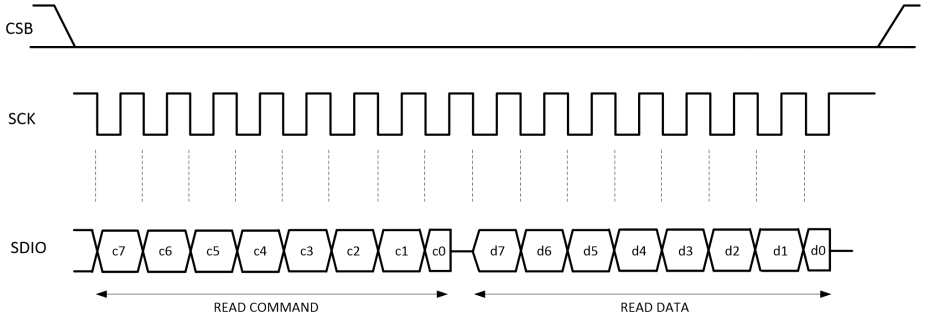


Figure 10. Read Mode

It's noted that read command is issued by SPI master. After c0 (LSB of command byte) is issued, it should give up data line (high impedance) and stop SCLK idle high after meeting hold time (10ns).

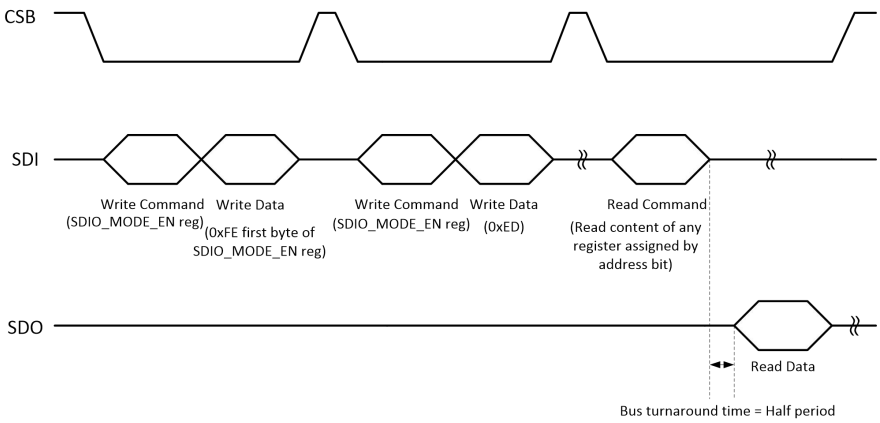


Figure 11. Enable SDIO Mode for Reading SPI Register

Note : 1. Once unlock SDIO_mode, as long as no other contents are written to SDIO_mode_en register to disturb SDIO_mode state, user could read as many registers as possible.

2. In order to easy to understand, the figure lists separate SDI and SDO signals, while SDIO signal only exists in design.

Register Organization

Realize device configuration by using "write"of specified register. All registers are organized as the byte-long register which could access address alone and have a unique address. The write/read instruction format is as followed.

BIT[7]	BIT[6:4] [1]	BIT[3:0]
0: Write Mode; 1: Read Mode	Reserve 0	Address

Note 1 : Bit[6:4] is specified as only zero, and other values are prohibited.

Register

The part describes programmable register and relevant programme sequence. The following table is the abstract list of available all registers and power-up values for user.

Title	Address (Hex) [1]	Type	Power-up/Reset (Hex)
Device Configuration	0×0	Read-Write (allowable read in SDIO mode)	0×0
DAC Configuration	0×1	Read-Write (allowable read in SDIO mode)	0×80
SDIO Mode Enable	0×F	Write-only	0×0

Note 1: The recommended value must be programmed in specified position to avoid other conditions. Don't write into the unmentioned address in document, otherwise it may cause incidents.

Device Configuration - Device Configuration Register (Address 0×0)

Bit	Bit Name	Description
7	Reserved	0
[6:5]	EN	00: PGA1 OFF, PGA2 OFF (default) 01: PGA1 OFF, PGA2 ON 10: PGA1 ON, PGA2 OFF 11: PGA1 ON, PGA2 ON
4	EXT_FILT	0: PGA1 to PGA2 (default) 1: PGA1 to PGA2 through external filter
3	CMN_MODE	0 : 1.15V(default); 1 : 2.59V
[2:1]	GAIN2	00: 4 (default); 01: 8; 10: 16; 11: 32
0	GAIN1	0: 246 (default); 1: 41

DAC Configuration - DAC Configuration Register (Address 0×1)

According to formula, the output DC is as followed: Vout_shift=–33.8mV×(NDAC–128).

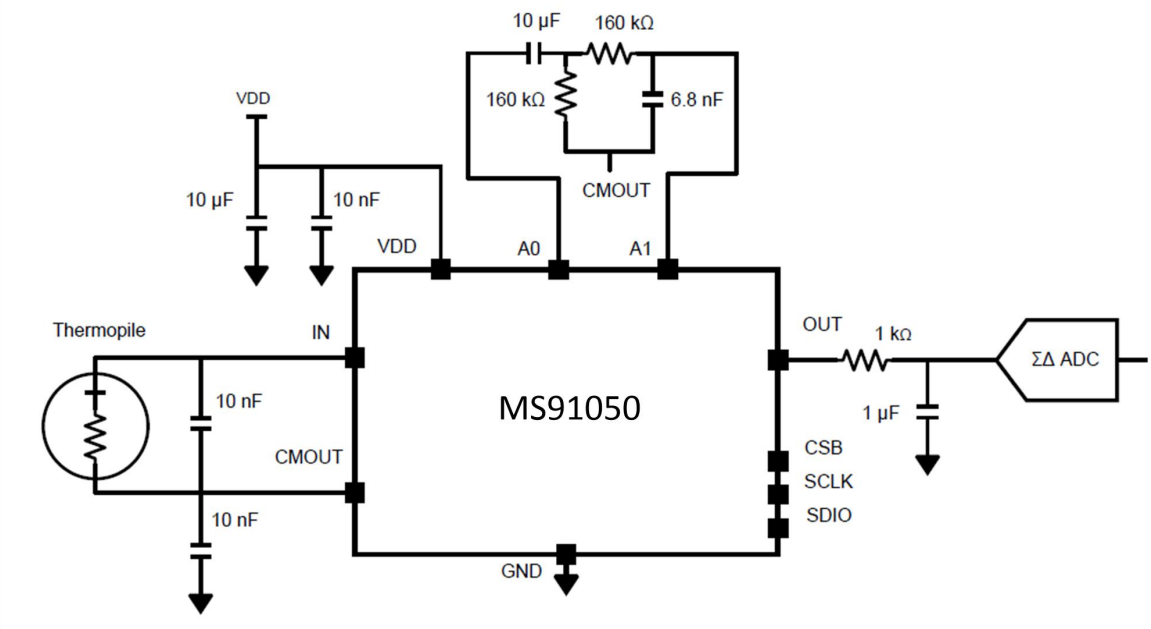
Bit	Bit Name	Description
[7:0]	NDAC	128(0×80): Vout_shift=–33.8mV×(128–128)=0mV(default)

SDIO Mode - SDIO Mode Enable Register (Address 0×f)

Write-only

Bit	Bit Name	Description
[7:0]	SDIO_MODE_EN	Write into continuous sequence 0×FE and 0×ED to enter SDIO mode. Write anything other than the sequence to exit the mode

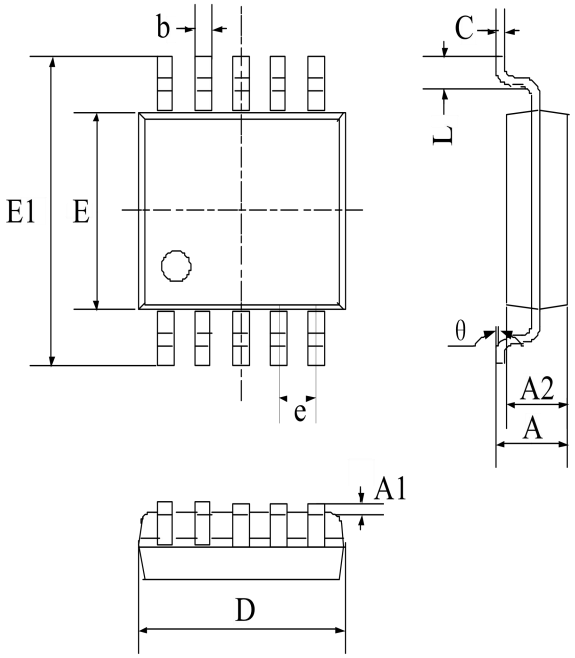
TYPICAL APPLICATION DIAGRAM



NDIR Sensor Typical Application Diagram

PACKAGE OUTLINE DIMENSIONS

MSOP10



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.800	1.200
A1	0.000	0.200
A2	0.760	0.970
b	0.30 TYP	
c	0.152 TYP	
D	2.900	3.100
e	0.50 TYP	
E	2.900	3.100
E1	4.700	5.100
L	0.410	0.650
θ	0°	6°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name： MS91050

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS91050	MSOP10	3000	1	3000	8	24000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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