MS90C365

——+3.3V LVDS 18-Bit Flat Panel Display Transmitter-150 MHz

General Description

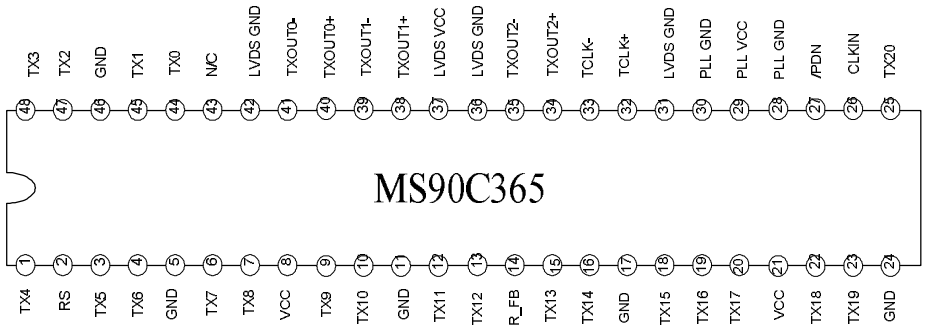
The MS90C365 transmitter converts 21 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams. At a transmit clock frequency of 150MHz, 18 bits of RGB data and 3 bits of LCD timing and control data are transmitted at a rate of 1050 Mbps per LVDS data channel. Using a 150 MHz clock, the data throughput is 525 Mbytes/sec. The MS90C365 can be programmed for Rising edge strobe or Falling edge strobe through the R_FB pin.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- Frequency Range：20-150MHz
- Single Supply:3.3V
- I/O power supply compatible with 1.8V, 3.3V
- Power-down mode < 200µW (max)
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- Up to 525 Megabytes/sec bandwidth
- reduced swing LVDS to reduce EMI（200mV or 345mV Optional）
- Internal PLL
- Low profile 48 lead TSSOP package
- Compatible with TIA/EIA-644 LVDS standard

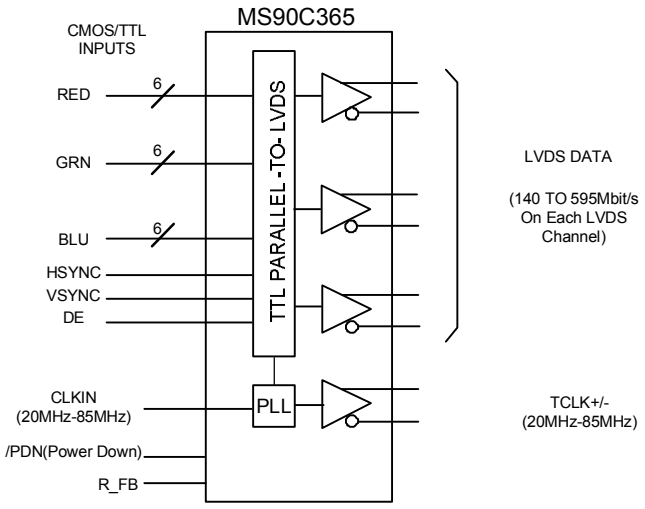
Pin Definition



MS90C365 Pin Description

Pin name	Pin number	type	Description
TXOUT0-,TXOUT0+	40, 41	LVDS outputs	LVDS differential data output
TXOUT1-, TXOUT1+	38, 39	LVDS outputs	
TXOUT2-, TXOUT2+	34, 35	LVDS outputs	
TCLK+, TCLK-	32, 33	LVDS outputs	LVDS differential clock output
TX0 ~ TX6	44,45,47,48,1,3,4	inputs	TTL TTL level input include：8 RED,8 GREEN,8 BLUE,4 control lines(HSYNC,VSYNC,DE,CNTL）
TX7 ~ TX13	6,7,9,10,12,1315	inputs	
TX14 ~ TX20	16,18,19,20,22,23, 25	inputs	
CLK IN	26	inputs	TTL level clock input.
/PDN	27	inputs	TTL level input.high：normal low：Low power
R_FB	14	inputs	Programmable strobe select high：Rising edge strobe low：Falling edge strobe
RS	2	inputs	LVDS swing control(normal RS=VCC,low swing RS=GND）
VCC	8	Power supply	Power supply pins for TTL inputs.
I/O VCC	21	I/O power supply	Power supply pins for I/O. Compatible with 1.8V, 3.3V
GND	5,11,17,24,46	Ground	Ground pins for TTL inputs
LVDS VCC	37	Power supply	Power supply pin for LVDS outputs.
LVDS GND	31,36,42	Ground	Ground pins for LVDS outputs.
PLL VCC	29	Power supply	Power supply pin for PLL.
PLL GND	28,30	Ground	Ground pins for PLL.

Block Diagram



Recommended Operating Conditions

Supply Voltage（V_{CC}）	-0.3V - 4.0V
CMOS/TTL Input Voltage	-0.3V - (VCC+0.3V)
CMOS/TTL output Voltage	-0.3V - (VCC+0.3V)
LVDS Driver Output Voltage	-0.3V - (VCC+0.3V)
Junction Temperature	+150°C
Storage Temperature	-65°C - +150°C
Power（25°C）	
MS90C365	1.9W

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	$0 \le V_{IN} \le V_{CC}$			±10	uA
I_{PD}	Low-power state current	$R\_FB=V_{CC}, V_{IH}=V_{CC}$			10	uA

Switching Characteristics

Symbol	Parameter		Min	Typ	Max	Units
T_{TCIT}	TxCLK IN Transition Time				5.0	ns
T_{TCP}	period		11.76	T	50	ns
T_{TCH}	TxCLK IN High Time		0.35T	0.5T	0.65T	ns
T_{TCL}	TxCLK IN Low Time		0.35T	0.5T	0.65T	ns
T_{TS}	TxIN Setup to TxCLK IN		2.5			ns
T_{TH}	TxIN Hold to TxCLK IN		0			ns
T_{LVT}	LVDSSignal conversion time			0.6		ns
T_{TCD}	TxCLK IN to TxCLK OUT Delay			2T/7+2.3		ns
T_{TDP1}	Output Data Bit 0	150MHz	-0.2	0	+0.2	ns
T_{TDP0}	Output Data Bit 1			0.95		ns
T_{TDP6}	Output Data Bit 2			1.90		ns
T_{TDP5}	Output Data Bit 3			2.86		ns
T_{TDP4}	Output Data Bit 4			3.81		ns
T_{TDP3}	Output Data Bit 5			4.76		ns
T_{TDP2}	Output Data Bit 6			5.71		ns
T_{TDP1}	Output Data Bit 0	100MHz	-0.2	0	+0.2	ns
T_{TDP0}	Output Data Bit 1			1.42		ns
T_{TDP6}	Output Data Bit 2			2.85		ns
T_{TDP5}	Output Data Bit 3			4.28		ns
T_{TDP4}	Output Data Bit 4			5.70		ns
T_{TDP3}	Output Data Bit 5			7.14		ns
T_{TDP2}	Output Data Bit 6			8.57		ns
T_{TDP1}	Output Data Bit 0	85MHz	-0.2	0	+0.2	ns
T_{TDP0}	Output Data Bit 1			1.68		ns
T_{TDP6}	Output Data Bit 2			3.36		ns
T_{TDP5}	Output Data Bit 3			5.04		ns
T_{TDP4}	Output Data Bit 4			6.72		ns
T_{TDP3}	Output Data Bit 5			8.40		ns
T_{TDP2}	Output Data Bit 6			10.08		ns
T_{TDP1}	Output Data Bit 0	50MHz	-0.2	0	+0.2	ns
T_{TDP0}	Output Data Bit 1			2.86		ns
T_{TDP6}	Output Data Bit 2			5.71		ns
T_{TDP5}	Output Data Bit 3			8.57		ns
T_{TDP4}	Output Data Bit 4			11.42		ns
T_{TDP3}	Output Data Bit 5			14.28		ns
T_{TDP2}	Output Data Bit 6			17.14		ns
T_{TDP1}	Output Data Bit 0	35MHz	-0.2	0	+0.2	ns

T_{TDP0}	Output Data Bit 1			4.08		ns
T_{TDP6}	Output Data Bit 2			8.16		ns
T_{TDP5}	Output Data Bit 3			12.24		ns
T_{TDP4}	Output Data Bit 4			16.33		ns
T_{TDP3}	Output Data Bit 5			20.41		ns
T_{TDP2}	Output Data Bit 6			24.49		ns
T_{TDP1}	Output Data Bit 0	20MHz	-0.2	0	+0.2	ns
T_{TDP0}	Output Data Bit 1			7.14		ns
T_{TDP6}	Output Data Bit 2			14.28		ns
T_{TDP5}	Output Data Bit 3			21.42		ns
T_{TDP4}	Output Data Bit 4			28.57		ns
T_{TDP3}	Output Data Bit 5			35.71		ns
T_{TDP2}	Output Data Bit 6			42.86		ns
T_{TPLLS}	Transmitter Phase Lock Loop Set		-	-	10	ms

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage（RS=VCC）	RL=100Ω	250	345	450	mV
	Differential Output Voltage（RS=GND）		100	200	300	
$\triangle V_{OD}$					35	mV
V_{OC}	Common mode voltage（RS=VCC）		1.125	1.25	1.375	V
	Common mode voltage（RS=GND）			1.20		
$\triangle V_{OC}$					35	mV
I_{OZ}		/PDN=0V			±10	uA

SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
I_{CCTG}	Supply Current 16 Grayscale	f=20MHz	18		mA
		f=35MHz	25		mA
		f=50MHz	28		mA

		f=85MHz	30		mA
		f=100MHz	33		mA
		f=150MHz	36		mA
I_{CCTP}	Supply Current Power Down	/PDN=0V	21		uA

AC Timing Diagrams

Figure 1. Test template "Worst Case Pattern"

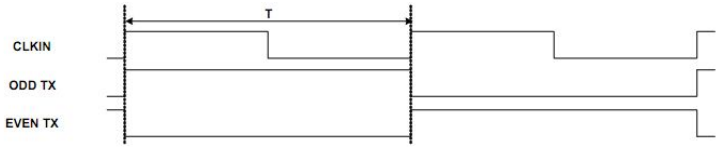


Figure 2. Test template "16 Grayscale Test Pattern"

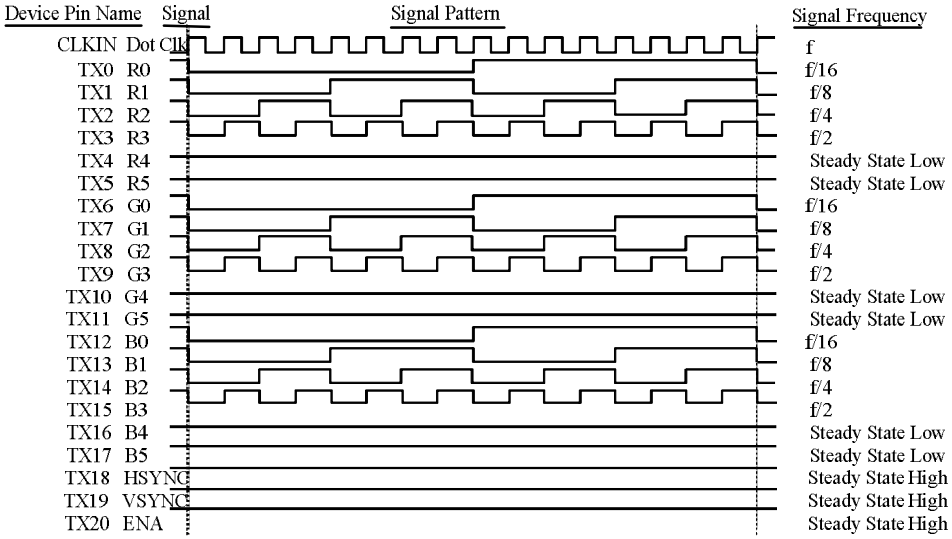


Figure 3.TTL input

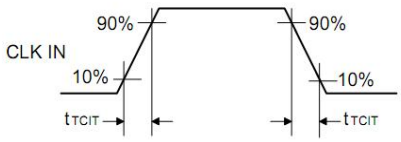


Figure 4.LVDS output

V_{diff}=（TXOUT+）-（TXOUT-）

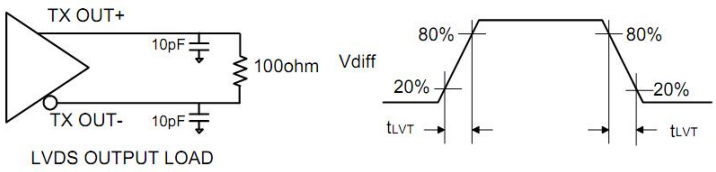


Figure 5. Phase Lock Loop Set Time

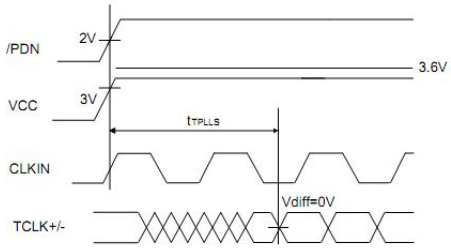
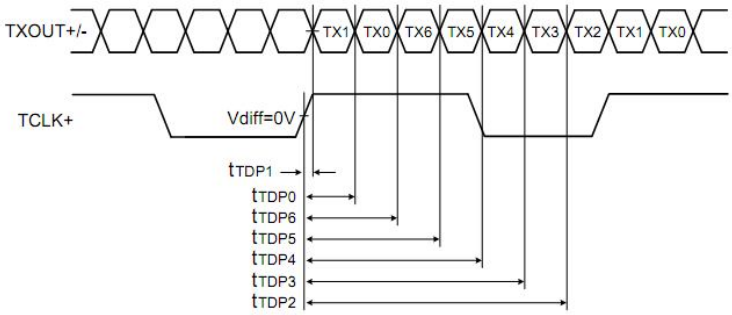


Figure 6. Transmitter state



Vdiff=（TXOUT+）-（TXOUT-），……（TCLK+）-（TCLK-）

Figure 7. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs

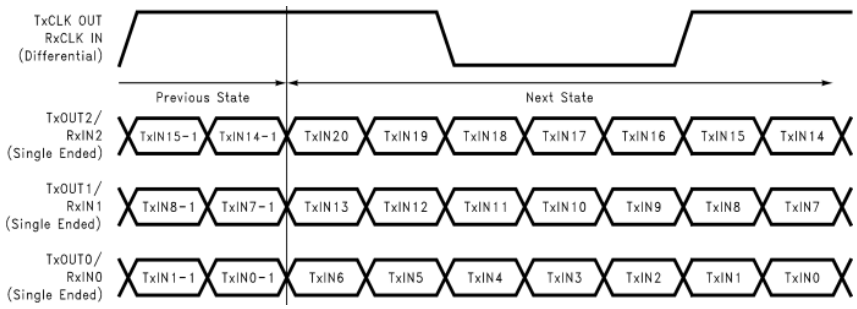


Figure 8. Setup/Hold and High/Low Times

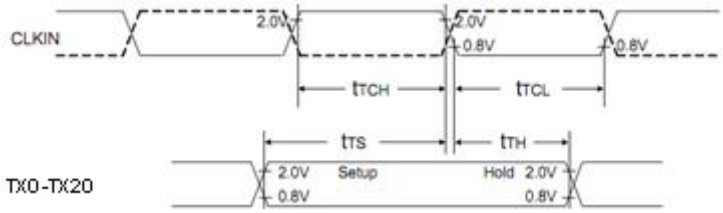
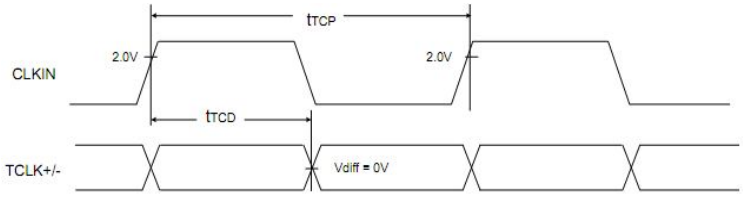
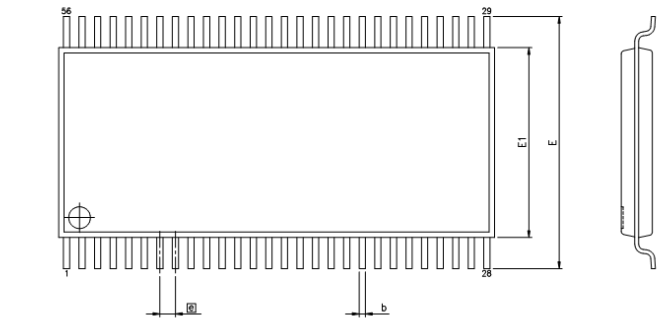
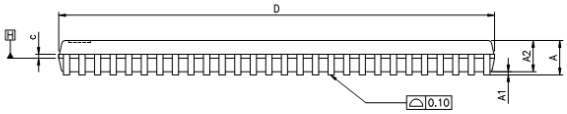


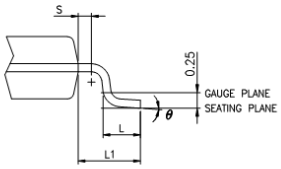
Figure 9. Clock In to Clock Out Delay



package outline drawing







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.17	–	0.27
c	0.09	–	0.20
D	13.90	14.00	14.10
E1	6.00	6.10	6.20
E	8.10 BSC		
e	0.50 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1.JEDEC OUTLINE : MO-153 EE REV.F
2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H .