MOSEL

MS621002

PRELIMINARY

256K x 4 CMOS Static RAM

MOSEL-VITELIC

T-46-23-10

FEATURES

- Fast Access Times: *20/25/35 ns
- Space Saving 400-Mil DIP
- High Density 400-Mil SOJ
- Low Standby Power
- TTL Compatible I/O
- 5V ± 10% Supply
- Fully Static Operation
- Three State Output
- JEDEC Standard Pinout

*20 nanoseconds is advanced information only.

DESCRIPTION

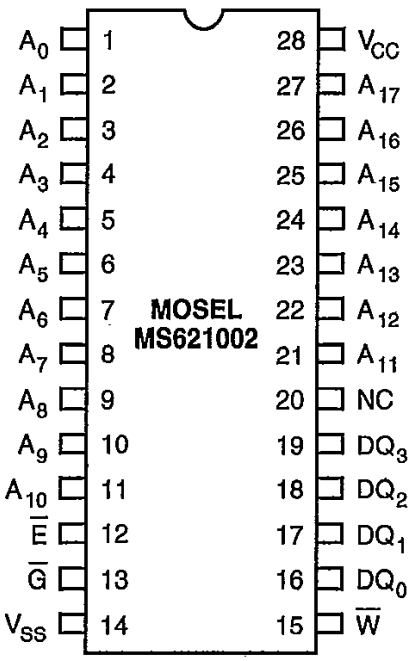
The MS621002 is a high speed 1M-bit static RAM organized as 256K x 4. Fully static in operation, the Chip Enable ($\overline{E}$) reduces power to the chip when HIGH. Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the address lines.

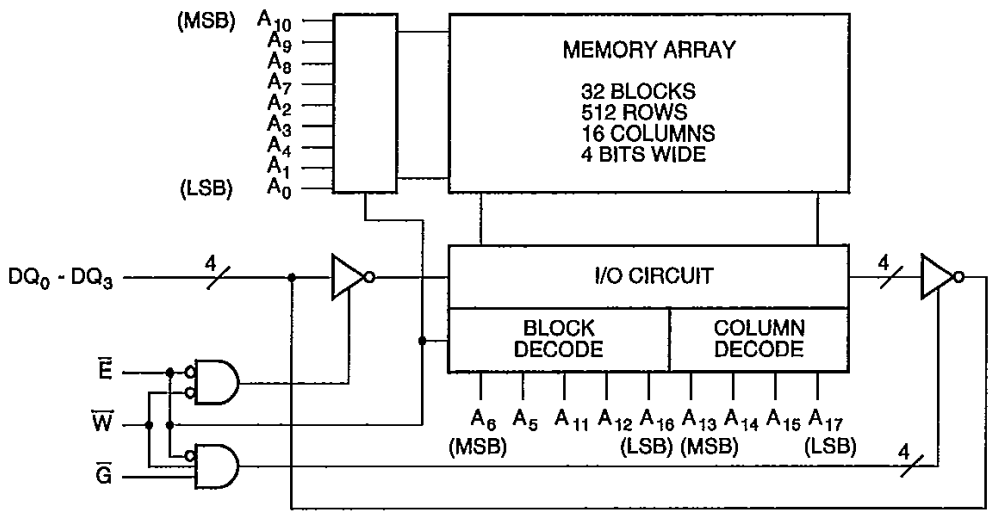
Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH.

High frequency design techniques should be employed to obtain optimum performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A_0 - A_{17} Address Inputs

These 18 address inputs select one of the 256K x 4 bit segments in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory locations.

DQ_0 - DQ_3 Data Input and Data Output Ports

These 4 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

V_{SS} Ground

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

ABSOLUTE MAXIMUM RATINGS (1)

PARAMETER NAME	PARAMETER		RATING	UNITS
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-65 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	D C Output Current		±40(2)	mA

See Notes following "SWITCHING CHARACTERISTICS".

DC ELECTRICAL CHARACTERISTICS (0°C to +70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage		4.5		5.5	V
V_{SS}	Supply Voltage		0		0	V
V_{IL}	Guaranteed Input LOW Voltage (3)		-0.5		0.8	V
V_{IH}	Guaranteed Input HIGH Voltage		2.2		V_{CC} + 0.5	V
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 20ns			130	mA
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 25ns			120	mA
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 35ns			100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$-0.2V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			5	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5V, V_{in} = 0V to V_{CC}	-2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5V, V_{in} = 0V to V_{CC}	-10		10	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA			0.4	V

See Notes following "SWITCHING CHARACTERISTICS".

CAPACITANCE(1) (T_A = 25°C, f = 1.0MHz)

PARAMETER NAME	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	I/O Capacitance	V_{DQ} = 0V	8	pF

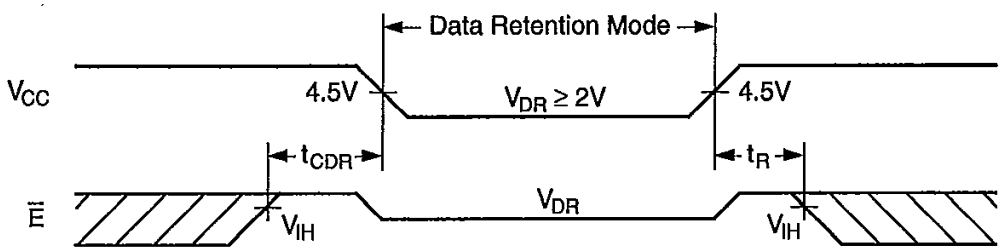
1. This parameter is guaranteed and not tested.

DATA RETENTION CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	$\overline{E} \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$-0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq$0.2V	2.0	-	5.5	V
I_{CCDR}	Data Retention Current	$\overline{E} \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$-0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq$0.2V	-	-	500(2)	µA
I_{CDR}	Chip Deselected to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(3)	-	-	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

TIMING WAVEFORM LOW V_{CC} DATA RETENTION WAVEFORM



AC ELECTRICAL CHARACTERISTICS (over the commercial operating range) [6]

PARAMETER NAME	PARAMETER	-20 MIN.	-20 MAX.	-25 MIN.	-25 MAX.	-35 MIN.	-35 MAX.	UNITS
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [7], [8]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [7], [8]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [7], [8]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [7], [8]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [8]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [8]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Timing	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [7], [8]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [7], [8]	3		3		3		ns

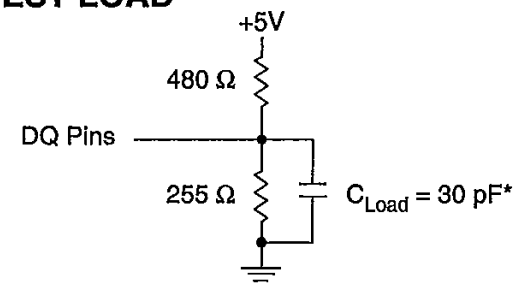
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.
2. Output should not be shorted for more than 30 seconds.
3. Negative undershoot of up to 3.0V is permitted once per cycle.
4. I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times.
5. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias}=0V and V_{CC}=5.0V.
6. Switching Characteristics measurements specified at "AC Test Conditions" levels.
7. Active output to High-Z and High-Z to active output tests specified for a ±200mV transition from steady levels into the test load.
8. Sample tested only.

AC TEST CONDITIONS

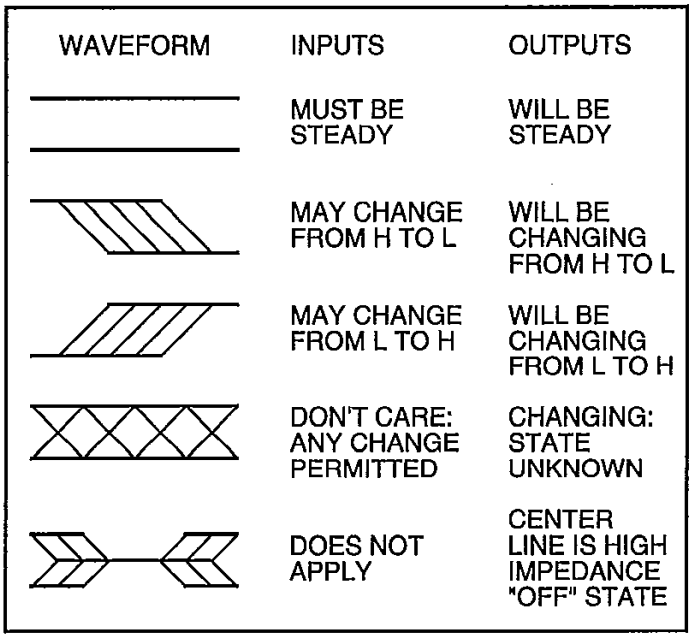
Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load, Timing Tests	See Figure Below

AC TEST LOAD



* Includes scope and jig capacitance

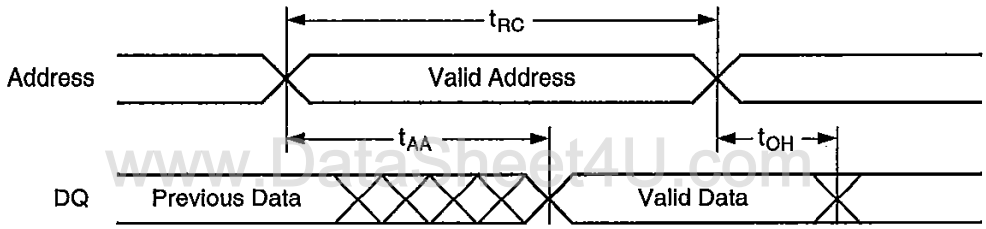
KEY TO SWITCHING WAVEFORMS



SWITCHING WAVEFORMS - READ CYCLE

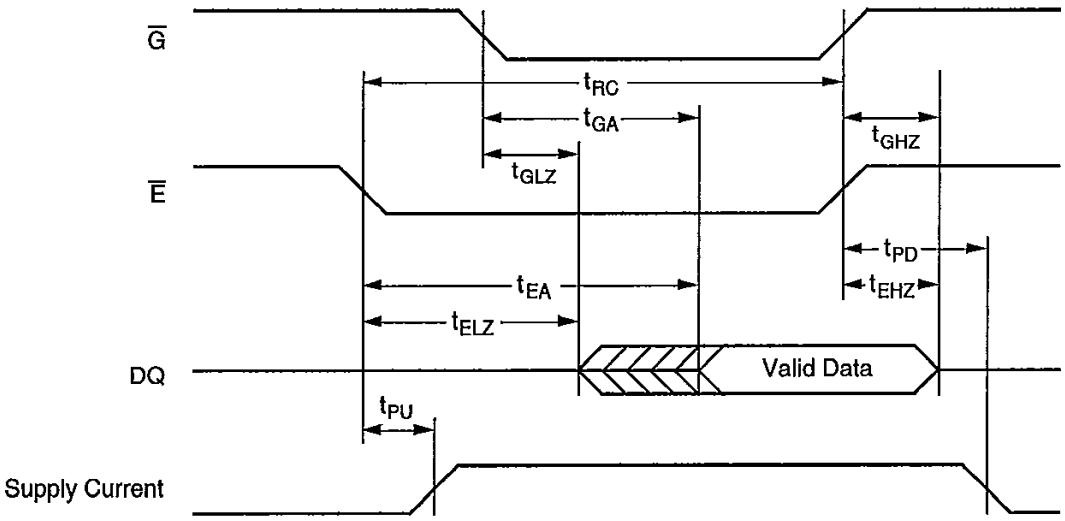
Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in Low-Z state and the data may not be valid.



Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data-out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data-out. Data-out is valid after both t_{EA} and t_{GA} are met.

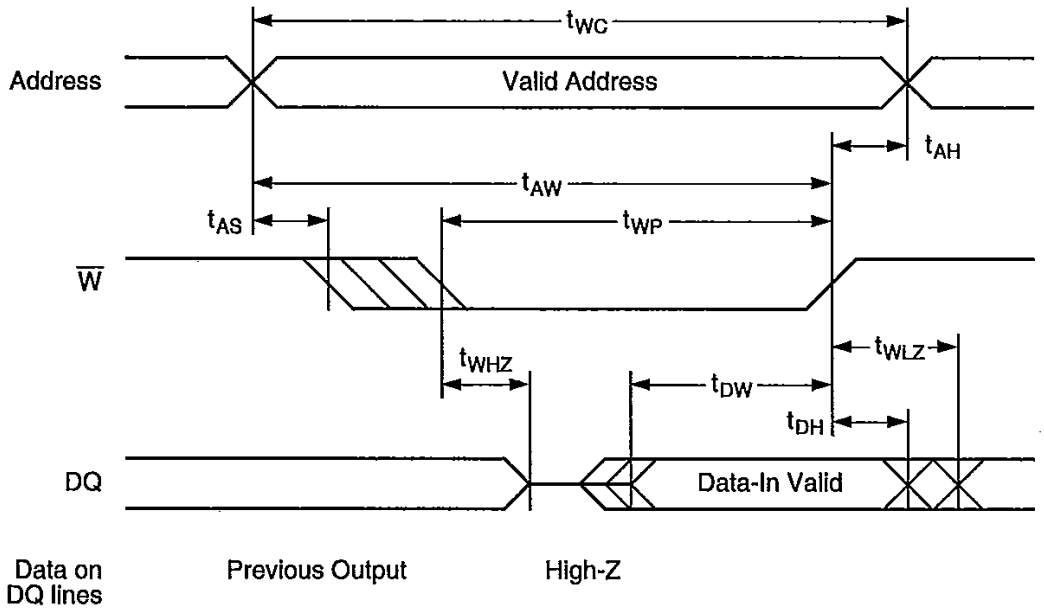


SWITCHING WAVEFORM - WRITE CYCLE

Addresses must be stable during Write Cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

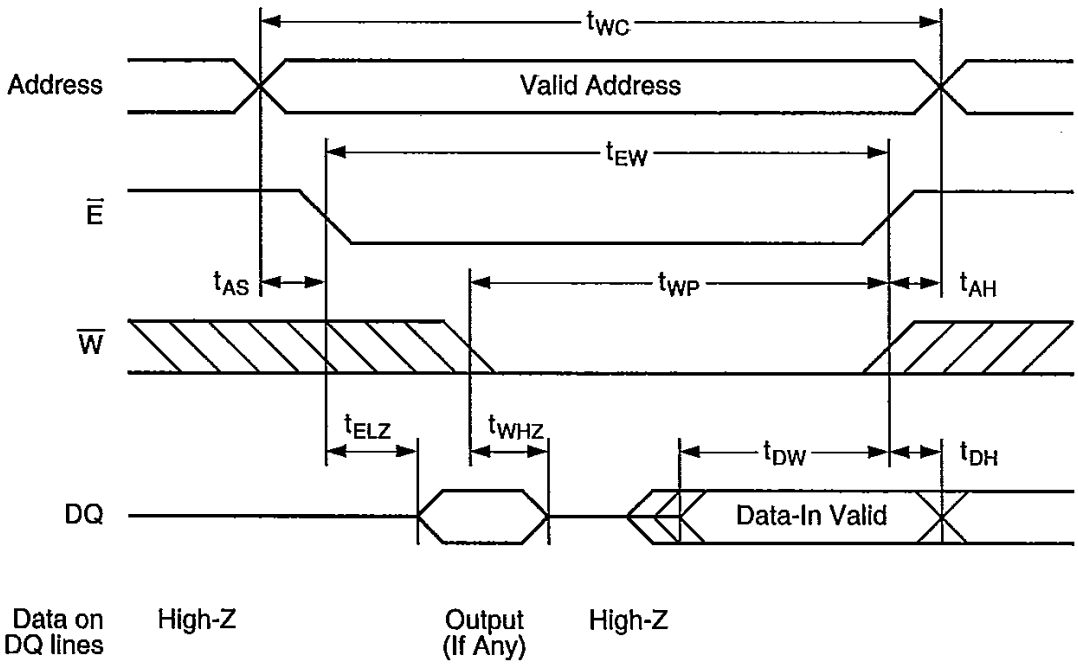
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.



Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.



ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
20	MS621002-20EC	E28-1*	0°C to +70°C
20	MS621002-20KC	K28-1	0°C to +70°C
25	MS621002-25EC	E28-1*	0°C to +70°C
25	MS621002-25KC	K28-1	0°C to +70°C
35	MS621002-35EC	E28-1*	0°C to +70°C
35	MS621002-35KC	K28-1	0°C to +70°C

* Contact Factory for Package Drawing