Quadruple 8Bit DAC

PRODUCT DESCRIPTION

The MS5620 is a quadruple, serial 8-bit voltage output digital-to-analog converter (DAC) featured by buffered reference inputs (high impedance). The output voltage range is from one or two times the reference voltage to GND and DAC is monotonic. The MS5620 is simple to use, because it operates in a single power supply, 3V to 5V. The power-up reset function can ensure repeatable start-up condition.

Digital control is achieved by three-wire serial bus which is compatible with CMOS and easily interfaced to microprocessor or microcontroller with industry standard. 11-bit command word is consist of 8-bit data, 2-bit DAC channel select and 1-bit range control. The range control bit allows the output voltage between one or two times the reference voltage. The DAC has two-stage latches, allowing a complete set of data to be written to the device. Then LDAC controls all DAC outputs to update simultaneously . The digital input has Schmitt trigger with anti-noise ability.

The small-outline package of the MS5620 enables the digital control of analog function to use in some applications which have strict demands for space. The MS5620 can operates from -40°C to 85°C and doesn't need external trimming.

FEATURES

- Four Channels, Eight Bits Output Voltage
- 3V~5V Sinle Power Supply
- Serial Interface
- Reference Input with High Impedance
- Programmable One or Two Times the Output Range
- Simultaneous Update Facility
- Internal Power-up Reset
- Low Power Dissipation
- Half-Buffered Output

SOP14

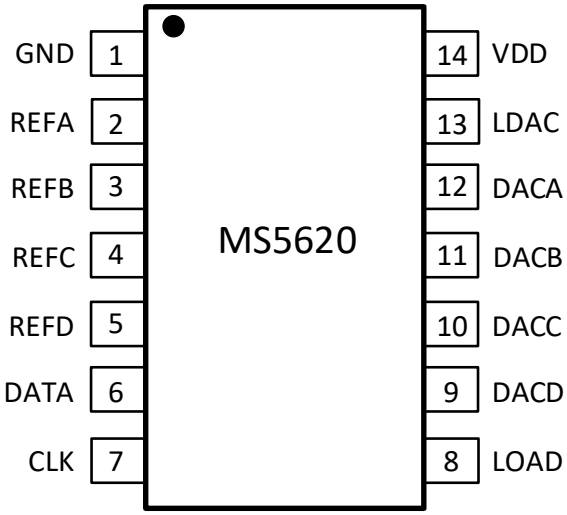
APPLICATIONS

- Programmable Voltage Source
- Digital Control Amplifier/Attenuator
- Mobile Communication
- Automatic Test Device
- Process Monitor
- Signal Synthesis

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5620	SOP14	MS5620

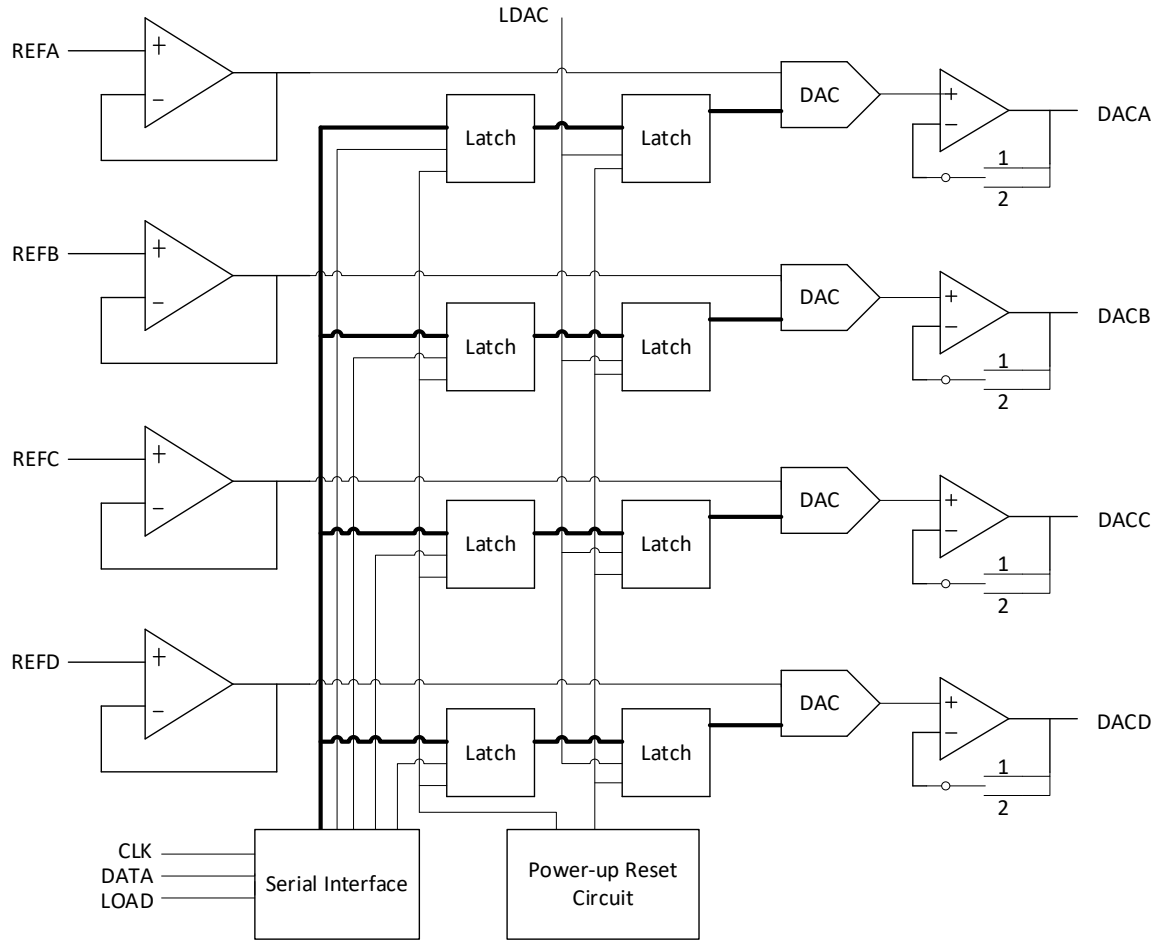
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	GND	-	Reference Ground
2	REFA	I	Reference Voltage for Channel A
3	REFB	I	Reference Voltage for Channel B
4	REFC	I	Reference Voltage for Channel C
5	REFD	I	Reference Voltage for Channel D
6	DATA	I	Serial Interface Digital Data Input. Each bit of data is written to the register of serial interface on the falling edge of clock signal.
7	CLK	I	Serial Interface Clock. Input serial data is written to the register of serial interface on the falling edge of input clock.
8	LOAD	I	Serial Interface Data Load. When LDAC is low, data is latched to the output latch on the falling edge of the LOAD and immediately analog signal is generated on the selected channel of DAC.
9	DACD	O	Analog Signal Output for Channel D
10	DACC	O	Analog Signal Output for Channel C
11	DACB	O	Analog Signal Output for Channel B
12	DACA	O	Analog Signal Output for Channel A
13	LDAC	I	DAC Data Load. When LDAC is high, DAC output doesn't update when input data is read into the serial interface. Only when LDAC become from high to low, DAC output would update.
14	VDD	--	Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	VDD	7	V
Digital Input Voltage		-0.3 ~ VDD+0.3	V
Reference Input Voltage	V_{ID}	-0.3 ~ VDD+0.3	V
Operating Temperature	TA	-40 ~ 85	°C
Storage Temperature	Tstg	-50 ~ 150	°C
Lead Temperature (Soldering 10s)		260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	VDD	2.7		5.25	V
Maximum Input Voltage	V_{IH}	0.8VDD			V
Minimum Input Voltage	V_{IL}			0.8	V
Reference Voltage	V_{REF}[A|B|C|D]			VDD-1.5	V
Load Resistor	R_L	10			kΩ
Operating Temperature	TA	-40		85	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD=3.3V±5%, VREF=2V, Gain=1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Current	IIH	V_I=VDD			±10	μA
Low-level Input Current	IIL	V_I=0			±10	μA
Current Sink Output	$I_{O(sink)}$	Each DAC Output	20			μA
Current Source Output	$I_{O(source)}$	Each DAC Output	1			mA
Input Capacitance	C_i			15		pF
Input Reference Capacitance				15		pF
Power Supply Current	I_{DD}	VDD=3.3V			2	mA
Input Reference Current	I_{ref}	VDD=3.3V, V_{REF}=1.5V			±10	μA
End Point Linearity Error [1]	E_L	V_{REF}=1.25V, Gain=2			±1	LSB
Differential Linearity Error [2]	E_D	V_{REF}=1.25V, Gain=2			±0.9	LSB
Zero-scale Error [3]	E_{ZS}	V_{REF}=1.25V, Gain=2	0		30	mV
Zero-scale Error Temperature Coefficient [4]		V_{REF}=1.25V, Gain=2		10		μV/°C
Full-scale Error [5]	E_{FS}	V_{REF}=1.25V, Gain=2			±60	mV
Full-scale Error Temperature Coefficient [6]		V_{REF}=1.25V, Gain=2		±25		μV/°C
Power Supply Rejection Ratio [7, 8]	PSRR			0.5		mV/V

Unless otherwise noted, VDD=5V±5%, VREF=2V, Gain=1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Current	IIH	V_I=VDD			±10	μA
Low-level Input Current	IIL	V_I=0			±10	μA
Current Sink Output	$I_{O(sink)}$	Each DAC Output	20			μA
Current Source Output	$I_{O(source)}$	Each DAC Output	2			mA
Input Capacitance	C_i			15		pF
Input Reference Capacitance				15		pF
Power Supply Current	I_{DD}	VDD=5V			2	mA
Input Reference Current	I_{ref}	VDD=5V, V_{REF}=2V			±10	μA
End Point Linearity Error [1]	E_L	V_{REF}=2V, Gain=2			±1	LSB
Differential Linearity Error [2]	E_D	V_{REF}=2V, Gain=2			±0.9	LSB

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Zero-scale Error [3]	E_{ZS}	V_{REF}=2V, Gain=2	0		30	mV
Zero-scale Error Temperature Coefficient [4]		V_{REF}=2V, Gain=2		10		μV/°C
Full-scale Error [5]	E_{FS}	V_{REF}=2V, Gain=2			±60	mV
Full-scale Error Temperature Coefficient [6]		V_{REF}=2V, Gain=2		±25		μV/°C
Power Supply Rejection Ratio [7, 8]	PSRR			0.5		mV/V

Note:

1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full-scale (excluding zero-scale and full-scale errors).

2. Differential nonlinearity (DNL) is the difference between the 1LSB and the change value of output voltage generated by any two adjacent codes in 8-bit digital codes. Monotonic means the change direction of output voltage is same as digital input code.

3. Zero-scale error is the difference between the output voltage and GND when input is all zero.

4. Zero-scale error temperature coefficient is determined by :

$$ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{REF} \times 10^6/(T_{max} - T_{min})$$

5. Full-scale error is the difference between the actual output voltage and ideal output when input is all one in 10kΩ load resistor condition.

6. Full-scale error temperature coefficient is determined by :

$$FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{REF} \times 10^6/(T_{max} - T_{min})$$

7. Zero-scale error rejection ratio is measured : measure the effect on output voltage when 8bit digital input is all zero and VDD changes from 4.75V to 5.25V.

8. Full-scale-error rejection ratio (FSE RR) is measured by varying the VDD from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

Full-scale error rejection ratio is measured : measure the effect on output voltage when 8bit digital input is all one and VDD changes from 3V to 3.6V.

OPERATING CHARACTERISTICS

1. Operating Characteristics in Recommended Operating Conditions

Unless otherwise noted, VDD=5V±5%, or VDD=3.3V±5%, V_{REF}=2V, Gain=1.

Parameter	Condition	Min	Typ	Max	Unit
Output Slew Rate	C_L = 100 pF, R_L = 10 kΩ		1		V/μs
Output Settling Time	to ±0.5LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		μs
Large-signal Bandwidth	Test at -3dB point		100		kHz
Digital Crosstalk	CLK=1MHz square wave is measured at DACA-DACD		-50		dB
Reference Voltage Feedthrough	See Note 10		-60		dB
Channel Isolation	See Note 11		-60		dB
Reference Voltage Input Bandwidth	See Note 12		100		kHz

Note:

9. Settling time is the time between the falling edge of LOAD and the DAC output reaching full-scale voltage within ±0.5LSB.

10. Reference feedthrough is given by measuring the output voltage of any DAC when digital input is all zero, V_{REF}=1V DC + 1V_{pp} and frequency is 10kHz.

11. Channel isolation is measured when input frequency is 10kHz, V_{REF}=1V DC + 1V_{pp}, the digital input of one channel is all one, and other three channels are all zero.

12. Reference bandwidth is the -3dB bandwidth with an input at V_{REF}=1.25V DC + 2V_{pp} and with all one of digital input.

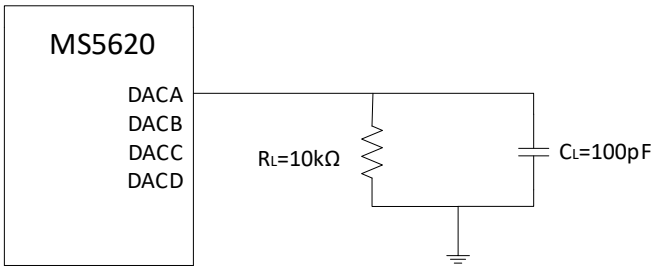
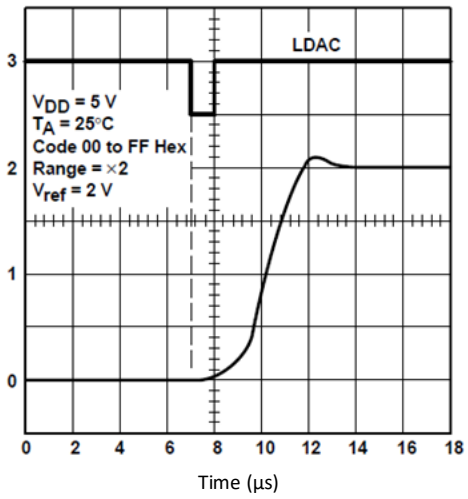
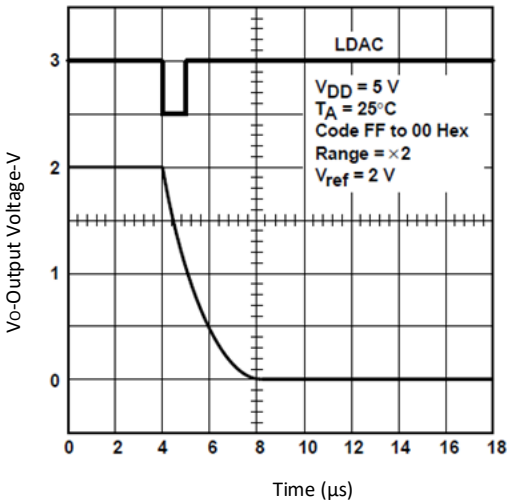
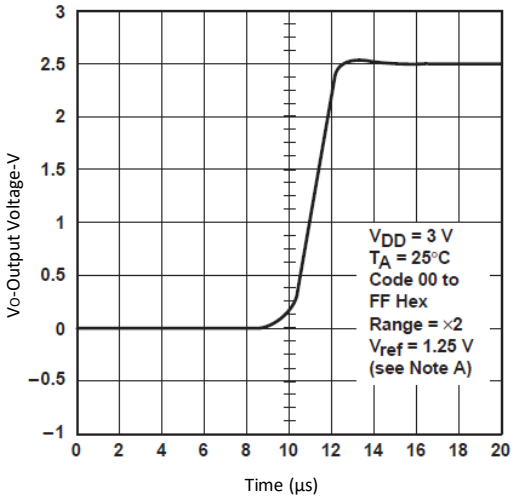


Figure 1. Measurements for Slew Rate, Settling Tim and Linearity

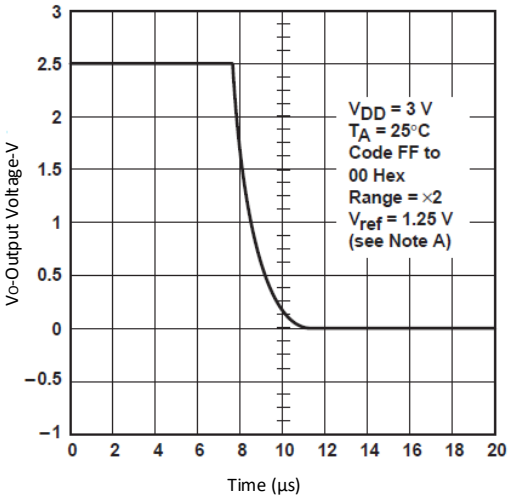
2. Typical Characteristics



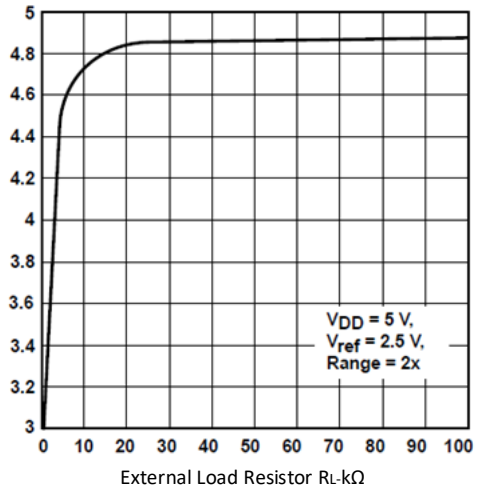


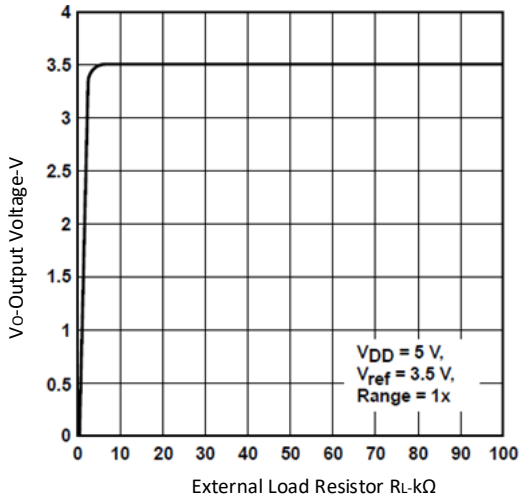


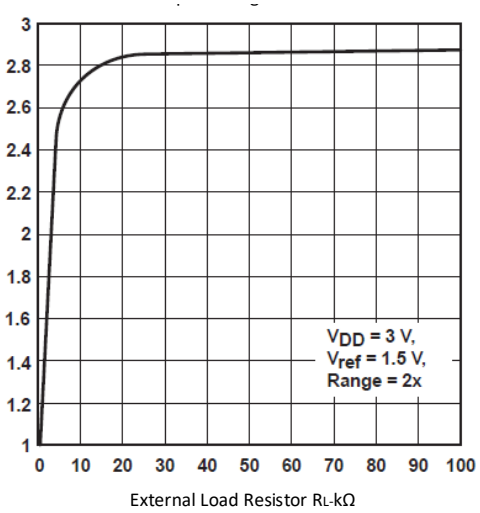
Note: Rise Time 2.05µs, Positive Slew Rate 0.96V/µs, Settling Time 4.5µs

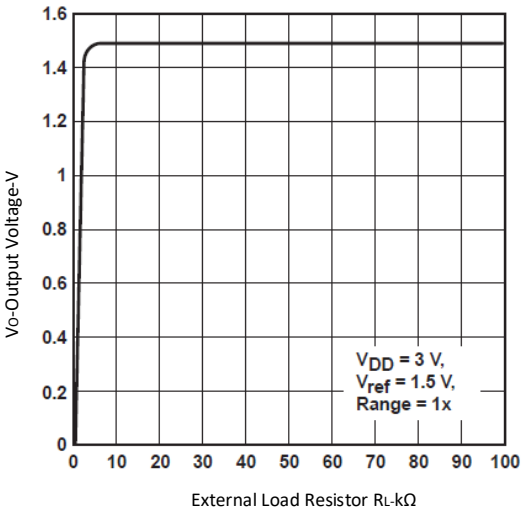


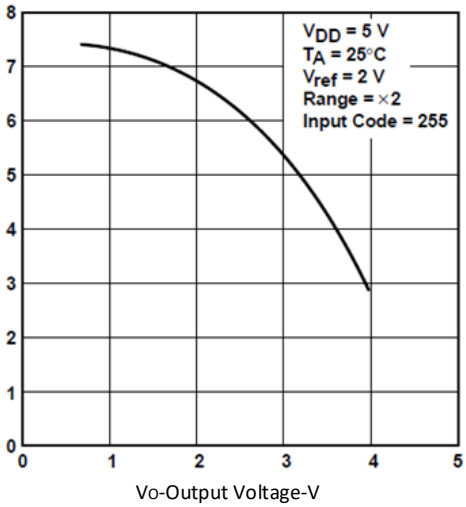
Note: Fall Time 4.25µs, Negative Slew Rate 0.46V/µs, Settling Time 8.5µs

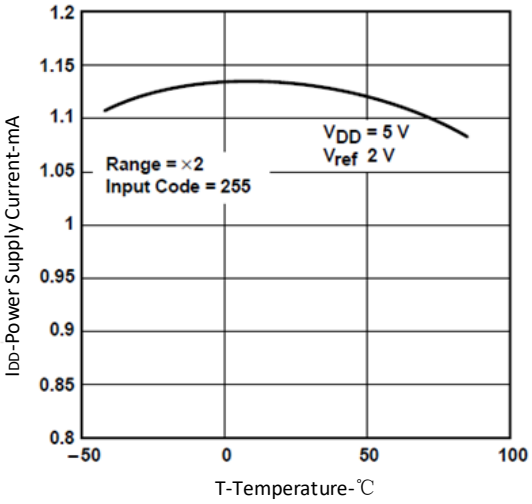

5
4.8
4.6
4.4
4.2
4
3.8
3.6
3.4
3.2
3
0 10 20 30 40 50 60 70 80 90 100
VDD = 5 V,
Vref = 2.5 V,
Range = 2x
External Load Resistor RL-kΩ


4
3.5
3
2.5
2
1.5
1
0.5
0
VO-Output Voltage-V
0 10 20 30 40 50 60 70 80 90 100
VDD = 5 V,
Vref = 3.5 V,
Range = 1x
External Load Resistor RL-kΩ

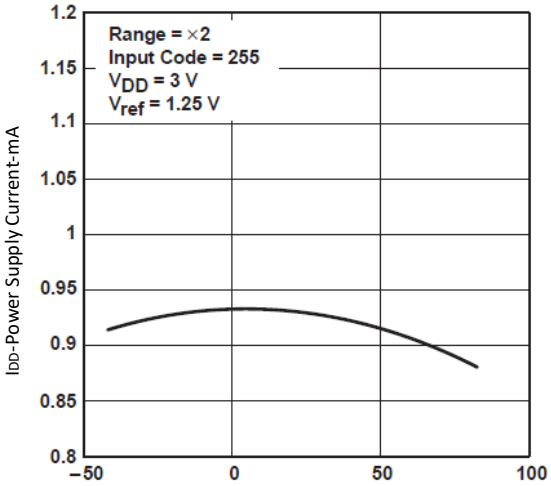

3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
0 10 20 30 40 50 60 70 80 90 100
VDD = 3 V,
Vref = 1.5 V,
Range = 2x
External Load Resistor RL-kΩ


1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
VO-Output Voltage-V
0 10 20 30 40 50 60 70 80 90 100
VDD = 3 V,
Vref = 1.5 V,
Range = 1x
External Load Resistor RL-kΩ

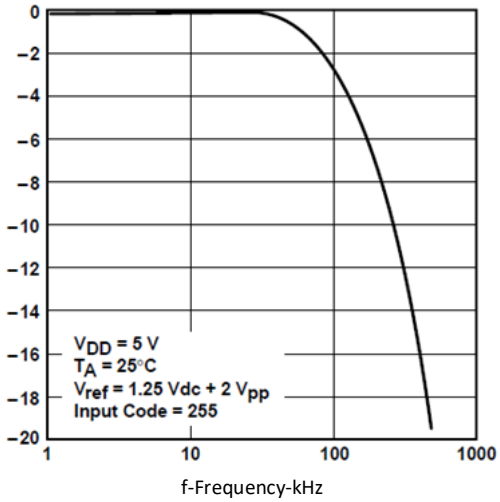


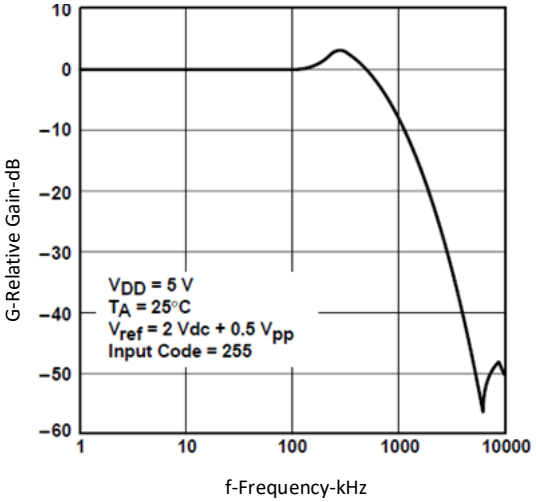


Power Supply Current VS. Temperature



Relative Gain VS. Frequency





FUNCTION DESCRIPTION

1. Resistor String DAC

The MS5620 is realized by four resistor-string DACs. The core of each DAC is a resistor with 256 taps. Table 1 shows the corresponding relationship between the level at each tape and 256 digital codes. One end of each resistor string is connected to GND and the other end is connected to output terminal of input buffer. Resistor string ensures the monotonicity. Linearity is determined by the match precision and the performance of output buffer. When reference voltage is buffered, the DAC can be regarded as a high-impedance load for reference source. Each DAC output is buffered by configurable-gain operational amplifier selecting one or two times gain. The digital input is set all zero at power-up. Each DAC output can be expressed as follows:

$$V_O(\text{DACA}\,|\,\text{B}\,|\,\text{C}\,|\,\text{D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG})$$

CODE ranges from 0 to 255. Rang control bit, RNG is 0 or 1 and in serial command word.

Table 1. Ideal Transmission Characteristics

D7	D6	D5	D4	D3	D2	D1	D0	Output Level
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256)×REF(1+RNG)
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	(127/256)×REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256)×REF(1+RNG)
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	(255/256)×REF(1+RNG)

2. Operating Timing

The MS5620 has four optional control ways shown in figure 2 to figure 5.

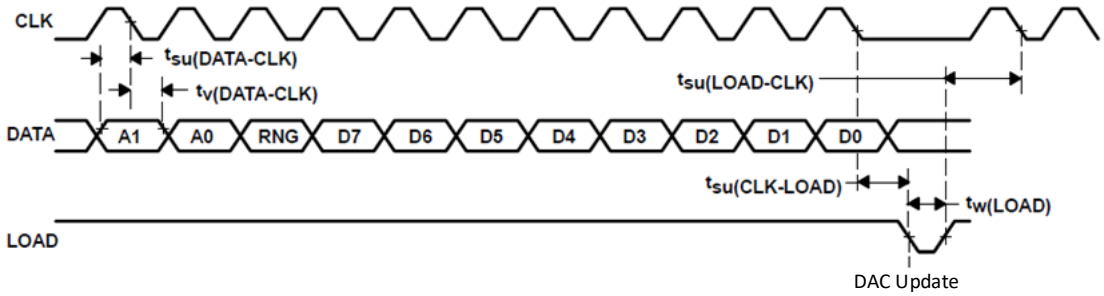


Figure 2. LOAD Controlling Output Update (LDAC=Low)

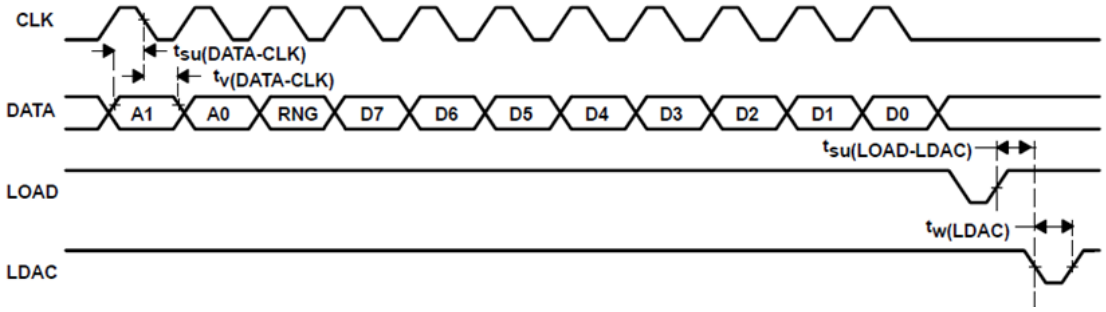


Figure 3. LDAC Controlling Output Update

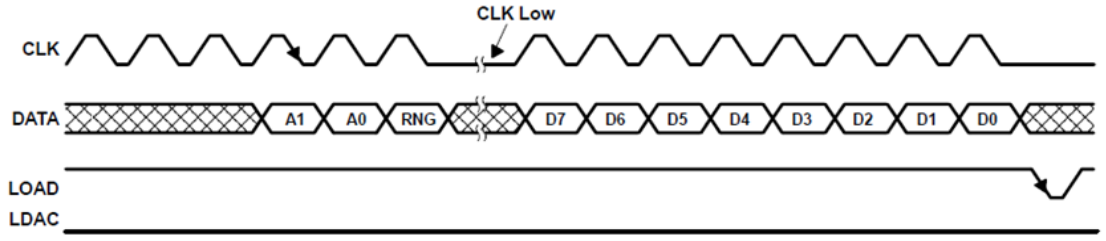


Figure 4. LOAD Controlling Output Update, Use 8bit Serial Command Word (LDAC=Low)

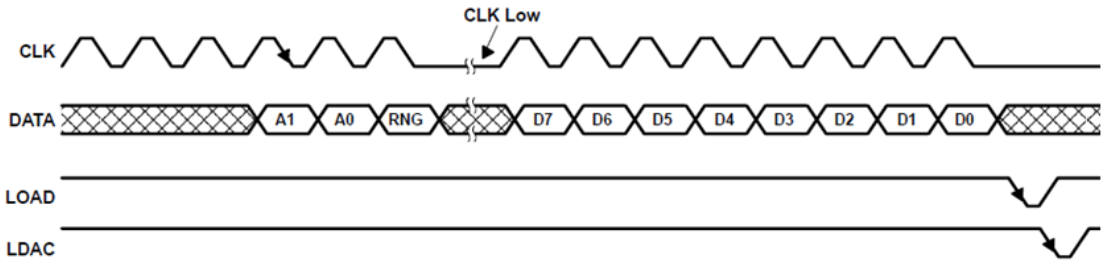


Figure 5. LDAC Controlling Output Update, Use 8bit Serial Command Word

When LOAD is high, data on DATA pin is written to latch on the falling edge of CLK. Once all data is latched, LOAD is pulled low, and data is transmitted from serial input register to the selected DAC as shown in Figure 2. When LDAC is low, DAC output voltage is immediately updated when LOAD becomes low. When LDAC is high during writing serial data, the new data is latched and digital-to-analog conversion is only performed only when LDAC is pulled low as shown in Figure 3. Most significant bit (MSB) is first written. Data conversion needs 8-clock cycle periods are shown in Figures 4 and 5. Table 2 lists the timing relationship.

Table 2. MS5620 Timing

Description	Min	Typ	Max	Unit
CLK Frequency			1	MHz
Settling Time, Data Input, $t_{su(DATA-CLK)}$ (See Figure 2 and Figure 3)	50			ns
Valid Time, Data Input Valid after CLK ↓, $t_{v(CLK\_LOAD)}$ (See Figure 2 and Figure 3)	50			ns
Settling Time, CLK↓ to LOAD, $t_{su(CLK-LOAD)}$ (See Figure 2)	50			ns
Settling Time, LOAD↑T to CLK↓, $t_{su(LOAD-CLK)}$ (See Figure 2)	50			ns

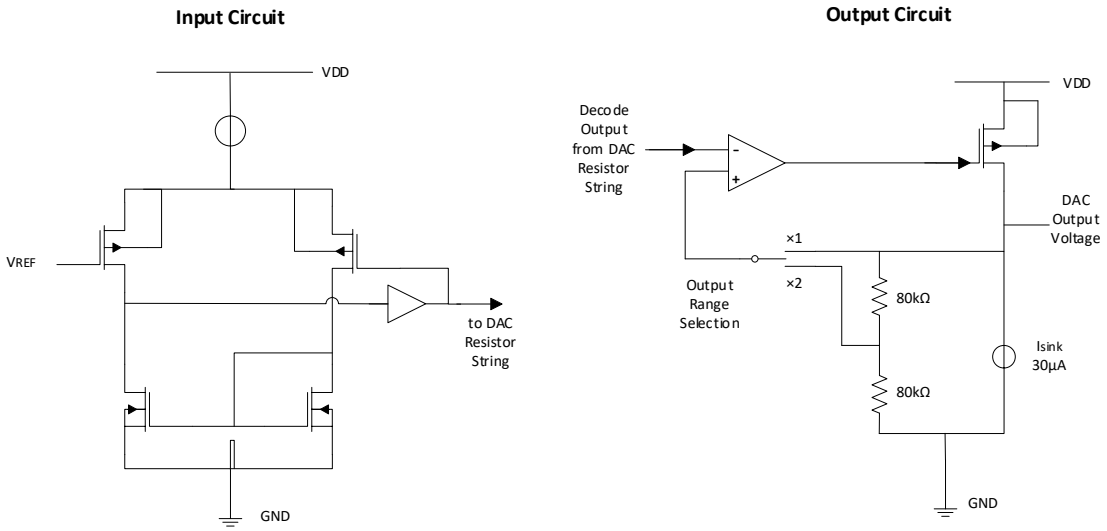
Description	Min	Typ	Max	Unit
Pulse Width, Pulse Width, LOAD, $t_{w(LOAD)}$ (See Figure 2)	250			ns
Pulse Width, DAC, $t_{w(LDAC)}$ (See Figure 3)	250			ns
Settling Time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$(See Figure 3)	0			ns

Table 3 lists the corresponding DAC channel for A1 and A0 bits. The RNG bit controls the output range. When RNG is low, output range is between the reference voltage and GND. When RNG is high, the output range is between twice the reference voltage and GND.

Table 3. Serial Input Decode

A1	A0	Select DAC Channel
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

3. Equivalent Input and Output Circuit



4. Offset Voltage

When amplifier operates from a single supply, the offset voltage can be positive or negative. When offset voltage is positive, output voltage would change on the first code change. When offset voltage is negative, output voltage may not change on the first code change, which depends on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the minimum negative supply is ground, output voltage cannot be less than ground and clamps to 0V.

The output voltage remains zero until the input code can generate enough positive output voltage to be more than the negative offset voltage. The conversion relationship is shown in Figure 6.

Offset error, not the linearity error, produces the breakpoint. If the buffer output can be less than 0, the conversion relationship is shown as dotted line .

For DAC, linearity is usually measured after offset and full-scale calibrations, and input increases from all 0 to all 1 gradually. However, due to the breakpoint, negative offset voltage cannot be calibrated in single supply. So the linearity is measured between full-scale code and the lowest code that generates positive output voltage. This code is calculated from the maximum value for the negative offset voltage.

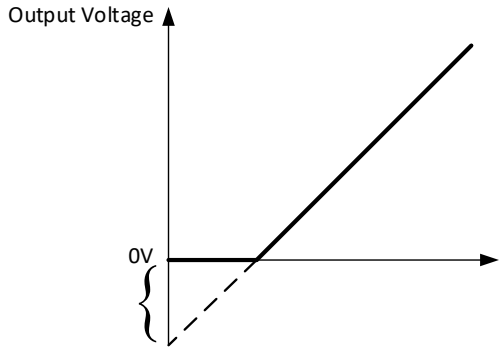


Figure 6. Negative Offset Voltage Effect (Single Supply)

TYPICAL APPLICATION DIAGRAM

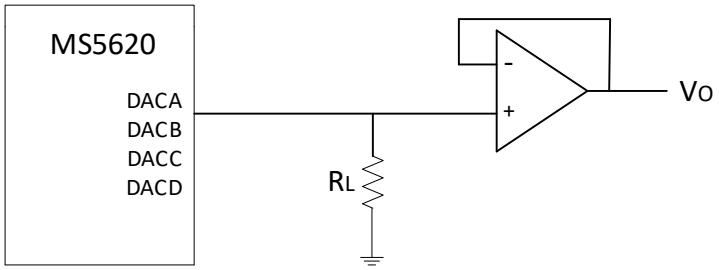
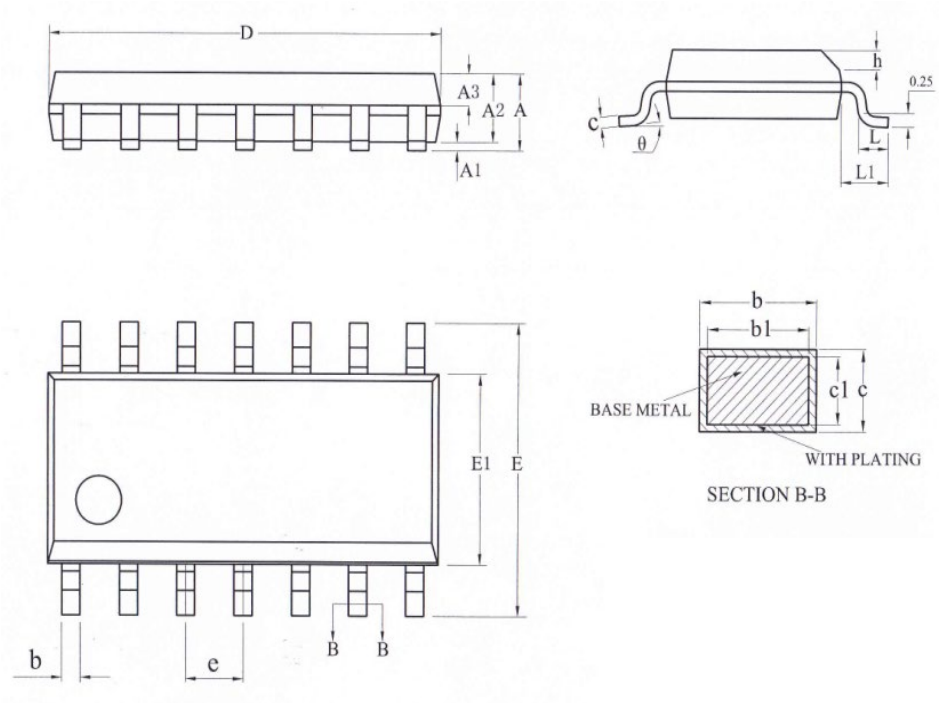


Figure7. Output Buffer Circuit, R_L≥10kΩ

PACKAGE OUTLINE DIMENSIONS

SOP14



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	--	--	1.75
A1	0.10	--	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	--	0.47
b1	0.38	0.41	0.44
c	0.20	--	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25	--	0.50
L	0.50	--	0.80
L1	1.05 REF		
θ	0 º	--	8 º

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS5620

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS5620	SOP14	2500	1	2500	8	20000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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