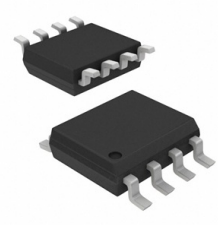
2.7V to 5.5V, Serial Input, Voltage Output, 16-Bit DAC

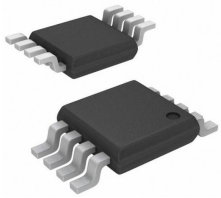
PRODUCT DESCRIPTION

The MS5541/MS5542 is a single-channel, 16-bit, serial input and voltage output digital-to-analog converter (DAC). It operates from single power supply with 2.7V to 5.5V, and the output range is from 0V to $V_{REF.}$ Within the output range, the monotonicity is ensured. And it could provide 1LSB INL accuracy at 14-bit in the temperature range of -40°C to +85°C. The MS5541/MS5542 provides unbuffered output and has many features, including short setup time, low power dissipation and low offset error. In addition, due to the low noise and low glitch characteristics, the MS5541/MS5542 is suitable for several terminal systems.

The MS5542 could operate in bipolar mode and generate $\pm V_{REF}$ output amplitude. It has Kelvin sense connection used for reference voltage and analog ground pin to reduce layout sensitivity.

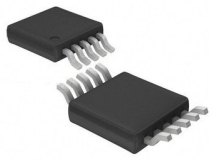


SOP8



MSOP8

SOP14



MSOP10

FEATURES

- 14-bit Valid Resolution
- 3V and 5V Single Power Supply
- Low Power Dissipation : 0.825mW
- Setup Time : 1.2us
- Unbuffered Voltage Output, Directly Drive 60kΩ Load
- Low Glitch : 1.1nV-s
- Compatible with SPI/QSPI/MICROWIRE and DSP Interface Standards

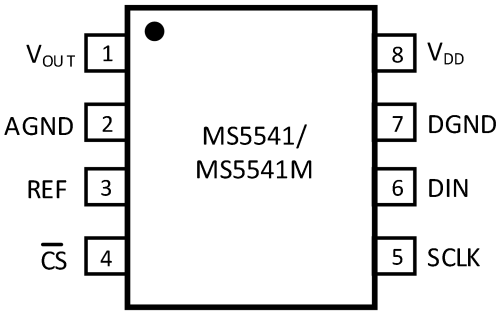
APPLICATIONS

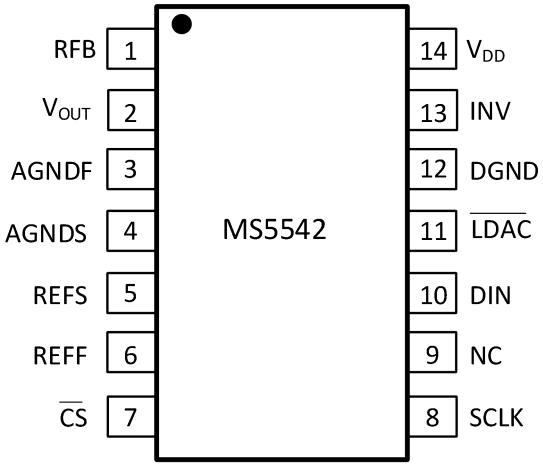
- Precision Measurement Device
- Automatic Test Device
- Data Acquisition System
- Industrial Process Control

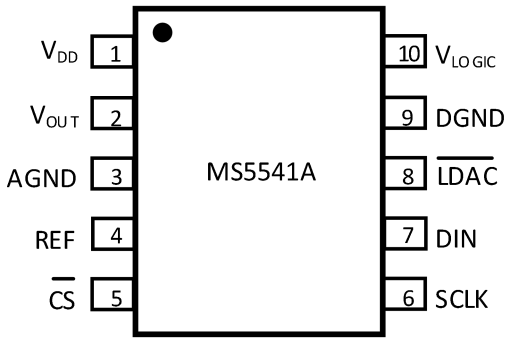
PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5541	SOP8	MS5541
MS5541M	MSOP8	MS5541M
MS5542	SOP14	MS5542
MS5541A	MSOP10	MS5541A

PIN CONFIGURATION







PIN DESCRIPTION

Pin	Name	Type	Description
MS5541/MS5541M			
1	V_{OUT}	O	DAC Analog Output Voltage
2	AGND	-	Analog Reference Ground
3	REF	I	DAC Reference Input Voltage. Connect with external 2.5V and the voltage range is from 2V to V_{DD}
4	$\overline{CS}$	I	Logic Input Signal. Chip select is used for input control of serial data
5	SCLK	I	Clock Input. Data enters into register at the rising edge
6	DIN	I	Serial Data Input. Support 16-bit data and data enters into register at the SCLK rising edge
7	DGND	-	Digital Reference Ground
8	V_{DD}	-	Power Supply
MS5542			
1	RFB	O	Resistor Feedback Pin. In bipolar mode, connect with external amplifier output
2	V_{OUT}	O	DAC Analog Output Voltage
3	AGNDF	-	Analog Reference Ground
4	AGNDS	-	Analog Reference Ground
5	REFS	I	DAC Reference Input Voltage (Sense). Connect with external 2.5V and the voltage range is form 2V to V_{DD}
6	REFF	I	DAC Reference Input Voltage (Force). Connect with external 2.5V and the voltage range is form 2V to V_{DD}
7	$\overline{CS}$	I	Logic Input Signal. Chip select is used for input control of serial data
8	SCLK	I	Clock Input. Data enters into register at the rising edge
9	NC	-	Not Connection
10	DIN	I	Serial Data Input. Support 16-bit data and data enters into register at the SCLK rising edge
11	$\overline{LDAC}$	I	When input is low level, DAC register is simultaneously updated with the content of serial register data
12	DGND	-	Digital Reference Ground
13	INV	O	Connect to DAC Internal Scaling Resistor. In bipolar mode, connect with inverting input terminal of external amplifier
14	V_{DD}	-	Power Supply

Pin	Name	Type	Description
MS5541A			
1	V_{DD}	-	Power Supply
2	V_{OUT}	O	DAC Analog Output Voltage
3	AGND	-	Analog Reference Ground
4	REF	I	DAC Reference Input Voltage. Connect with external 2.5V and the voltage range is form 2V to V_{DD}
5	$\overline{CS}$	I	Logic Input Signal. Chip select is used for input control of serial data
6	SCLK	I	Clock Input. Data enters into register at the rising edge
7	DIN	I	Serial Data Input. Support 16-bit data and data enters into register at the SCLK rising edge
8	$\overline{LDAC}$	I	When input is low level, DAC register is simultaneously updated with the content of serial register data
9	DGND	-	Digital Reference Ground
10	V_{LOGIC}	-	Logic Power Supply

BLOCK DIAGRAM

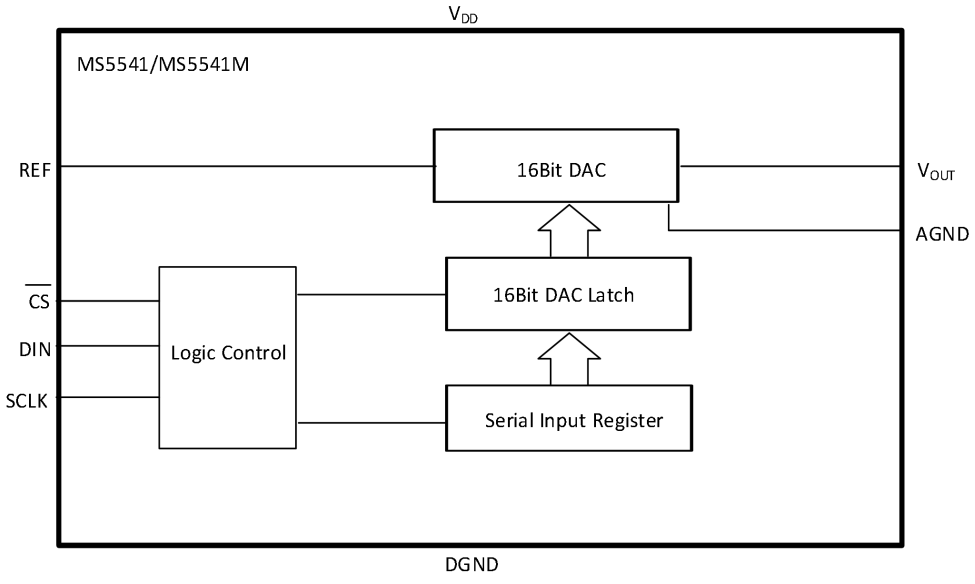


Figure 1. MS5541/MS5541M Block Diagram

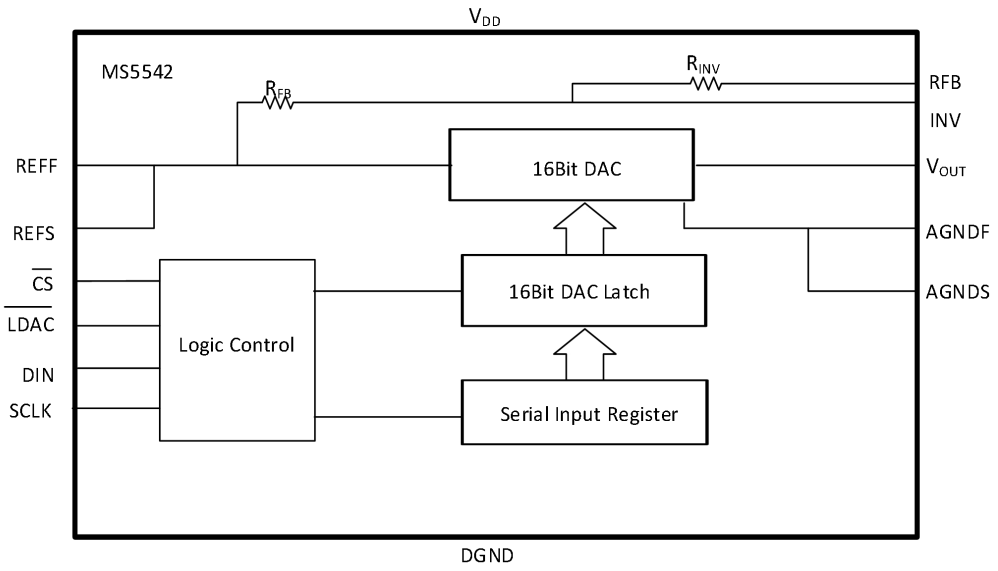


Figure 2. MS5542 Block Diagram

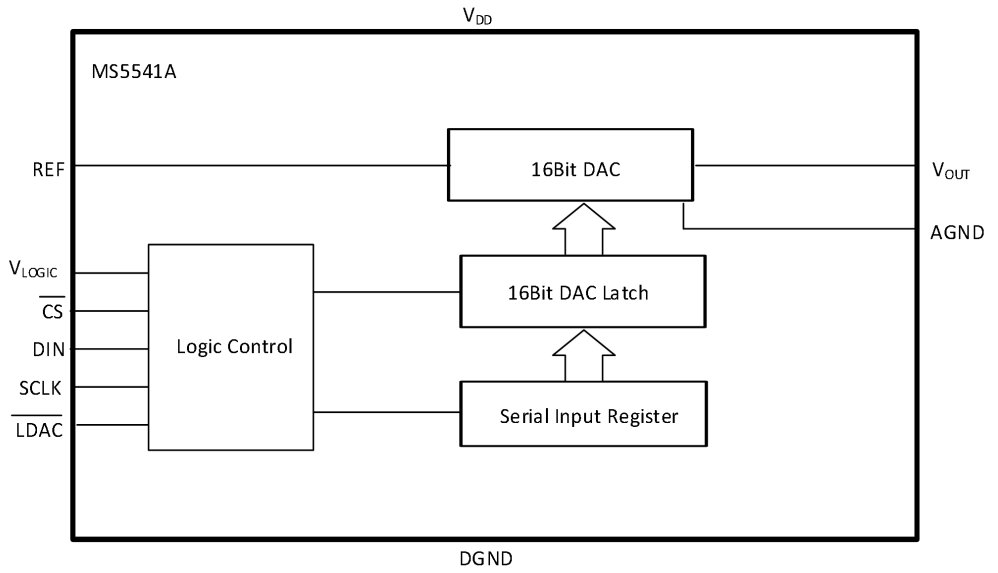


Figure 3. MS5541A Block Diagram

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

DGND=AGND=0V. All voltage values are all relative to 0V.

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	-0.3 ~ +6.0	V
Input Current	Iin	±10	mA
Operating Temperature [1]	Topr	-40 ~ +85	°C
Storage Temperature [1]	Tstg	-65 ~ +150	°C
ESD	HBM	>±3k	V

Note 1: All temperature conditions are Ta = 25°C, except operating temperature and storage temperature.

RECOMMENDED OPERATING CONDITIONS

Operating Power Supply Range

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	V_{DD}	2.7	5	5.5	V
Reference Voltage	V_{REF}	2	2.5	V_{DD}	V

ELECTRICAL CHARACTERISTICS

V_{DD}=2.7V~5.5V, V_{REF}=2V~V_{DD}, AGND=DGND=0V, TA=TMIN~TMAX

Note : Unless otherwise specified, Ta = 25°C ±2°C.

Parameter	Condition	Min	Typ	Max	Unit
Static Characteristic					
Resolution		14			bits
Integral Nonlinearity (INL)	V_{REF}=2.048V,V_{DD}=5V		±6.5	±10.5	LSB
Differential Nonlinearity (DNL)	TA=25℃		±4	±5	LSB
Gain Error	TA=25℃		±2	±5	LSB
Gain Error Temperature Coefficient			±0.1		ppm/°C
Unipolar Zero Code Error	TA=25℃		±2	±2.5	LSB
Unipolar Zero Code Error Temperature Coefficient			±0.05		ppm/°C
MS5542					
Bipolar Zero Offset Error	TA=25℃		±2	±5	LSB
Bipolar Zero Temperature Coefficient			±0.2		ppm/°C
Bipolar Zero Code Offset Error	TA=25℃		±2	±5	LSB
Bipolar Gain Error	TA=25℃		±2	±5	LSB
Bipolar Gain Temperature Coefficient			±0.1		ppm/°C
Output Characteristic					
Output Voltage	Unipolar Mode	0		V_{REF}-1LSB	V
	MS5442 Bipolar Mode	- V_{REF}		V_{REF}-1LSB	V
Setup Time, Output Voltage	C_L=10pF		1.2		us
Conversion Rate	C_L=10pF,0%-63%		17		V/us
Digital-to-Analog Glitch Impulse	1LSB		1.1		nV-sec
Digital Feedthrough	V_{REF}=2.048V		0.2		nV-sec
Output Noise Density	DAC Code=0×8400,f=1kHz		11.8		nV/√Hz
Output Noise Voltage	f=0.1Hz to 10Hz		0.134		uVp-p
Power Supply Rejection Ratio	ΔV_{DD}±10%			±1.0	LSB
DAC Reference Input					
Reference Input Range		2.0		V_{DD}	V
Reference Input Impedance	Unipolar Mode	90			kΩ
	MS5442 Bipolar Mode	72			kΩ

Parameter	Condition	Min	Typ	Max	Unit
Logic Input					
Input Current				±1	uA
Input Low Voltage				0.8	V
Input High Voltage		2.4			V
Input Capacitance				10	pF
Hysteresis Voltage			0.15		V
Power Supply					
Power Supply		2.7		5.5	V
Current	Digital Input 0		165	227	uA
Power Dissipation	Digital Input 0		0.825	1.248	mW

CLOCK CHARACTERISTICS

Unless otherwise specified : V_{DD}=2.7V~5.5V±10%, V_{REF}=2.048V, V_{INH}=90% V_{DD}, V_{INL}= 10%V_{DD}, AGND=DGND=0V, -40°C<TA<+85°C.

Parameter	Description	Value	Unit
f_{SCLK}	SCLK Cycle Frequency	20	MHz
t1	SCLK Cycle Time	50	ns min
t2	SCLK High-level Time	25	ns min
t3	SCLK Low-level Time	25	ns min
t4	Setup Time, $\overline{CS}$ Low to SCLK High	30	ns min
t5	Setup Time, $\overline{CS}$ High to SCLK High	45	ns min
t6	Hold Time, SCLK High to $\overline{CS}$ Low	45	ns min
t7	Hold Time, SCLK High to $\overline{CS}$ High	30	ns min
t8	Data Start Time	20	ns min
t9	Data Hold Time	10	ns min
t10	$\overline{LDAC}$ Pulse Width	60	ns min
t11	$\overline{CS}$ High to $\overline{LDAC}$ Low	60	ns min
t12	Valid Time, $\overline{CS}$ High	60	ns min

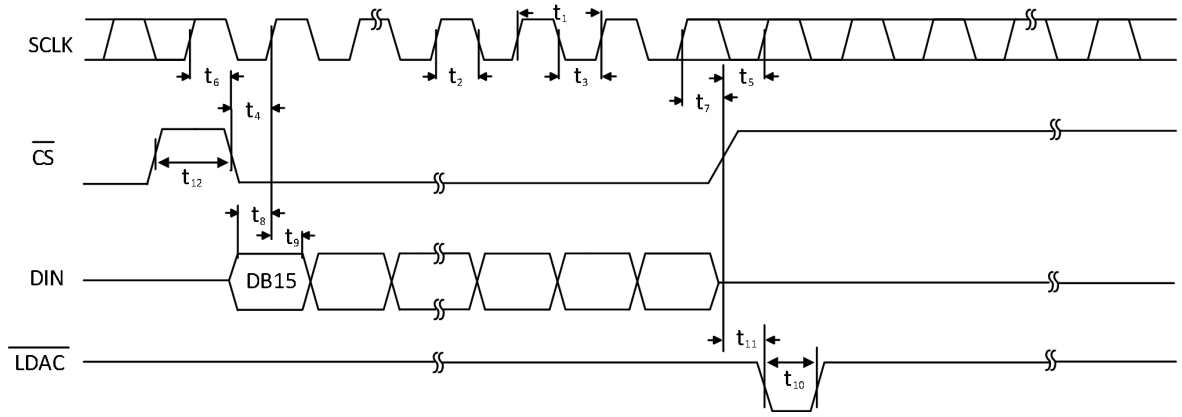


图 4. Timing Diagram

TYPICAL CHARACTERISTICS

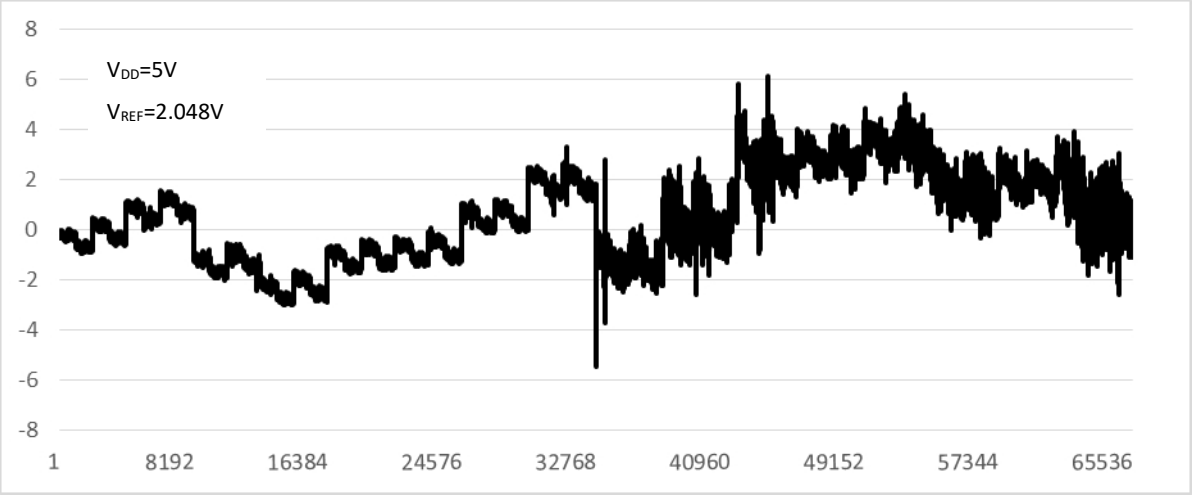


Figure 5. INL VS. Code

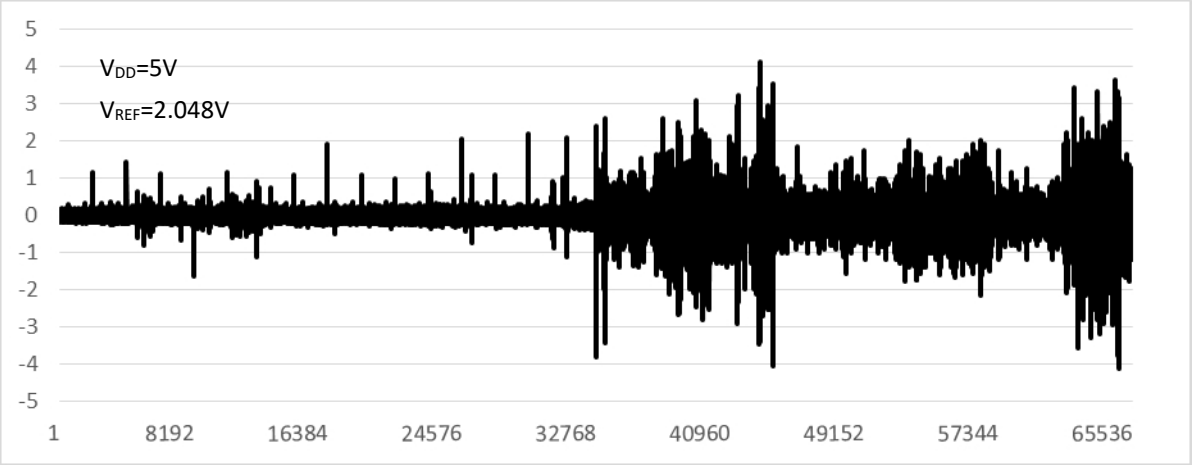


Figure 6. DNL VS. Code

OPERATING PRINCIPLE

The MS5541/MS5542 is a single-channel, 16-bit, serial input and voltage output DAC, whose operating voltage range is from 2.7V to 5.5V. The typical current consumption is 165uA at 5V power supply. Data is written to the device in 16-bit word format through 3-wire or 4-wire serial interface. In order to in known reset state, the device has power-up-reset function. In the unipolar mode, the MS5541 outputs 0. In bipolar mode, the MS55542 outputs -$V_{REF.}$ The MS5542 has Kelvin sense connection used for reference voltage and analog ground.

Digital-to-Analog Section

DAC architecture consists of two matched DAC sections. The figure 7 is simplified circuit diagram. The MS5541/MS5542 adopts segment-type architecture. The four MSBs of 16-bit data are decoded to drive 15 switches, E1 to E15. Each switch would connect one of 15 matched resistors to AGND or $V_{RE.}$ Other 12 bits of 16-bit data drive S0 to S11 switches of voltage mode R-2R ladder network.

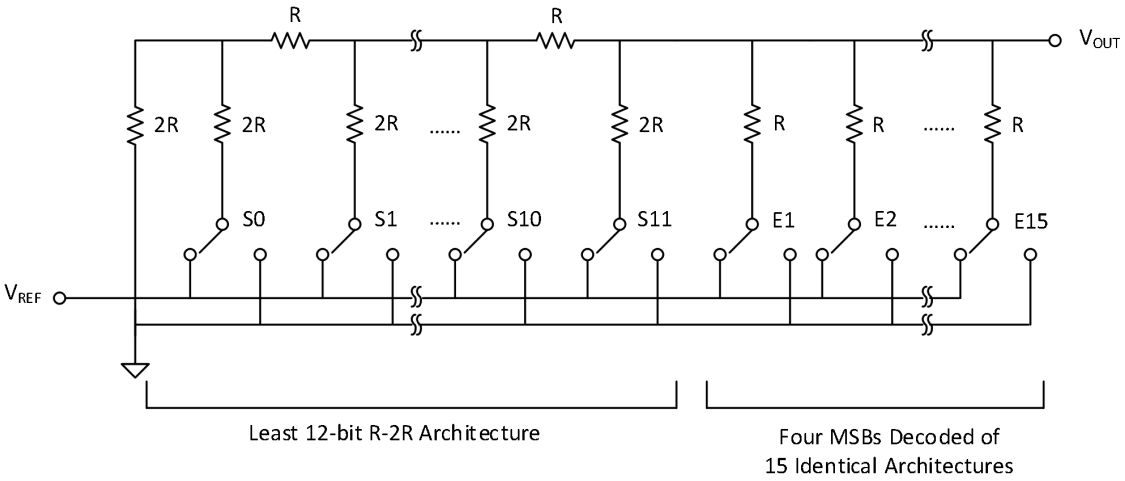


Figure 7. DAC Architecture

With this DAC configuration, output impedance is irrelevant to code. However, input impedance of reference voltage source is highly relevant to code. Output voltage is related to reference voltage shown in following formula.

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

D is decimal data word loaded to DAC register. N is DAC resolution. For 2.5V reference voltage, above formula could be simplified as follows.

$$V_{OUT} = \frac{2.5 \times D}{65536}$$

V_{OUT} is 1.25V when DAC is loaded to mid-scale; V_{OUT} is 2.5V when DAC is loaded to full-scale. LSB is V_{REF} /65536.

Serial Interface

The MS5541/MS5542 is controlled by multi-function 3-wire or 4-wire serial interface. It can operate at maximum 20MHz clock frequency and compatible with SPI, QSPI, MICROWIRE and DSP interface standards. The timing diagram is shown in figure 4. Beside 16-bit DAC register, the MS5541/MS5542 also has one independent serial input register. New data could be pre-loaded to the serial input register, and not disturb present DAC output voltage.

Input data is frame transmitted by chip select input $\overline{CS}$. When high-to-low transition occurs on $\overline{CS}$, data is shifted synchronously at the rising edge of serial clock SCLK, and latched in serial input register. After 16 data bits are all loaded to serial input register, low-to-high transition occurs on $\overline{CS}$. If $\overline{LDAC}$ is low level, the contents of shifted register would be transmitted to DAC register; If $\overline{LDAC}$ is high level, the contents only would be transmitted to serial input register. After new values are completely loaded to serial input register, transmit asynchronously to DAC register by making $\overline{LDAC}$ low . Data is loaded in 16-bit word format and MSB first. Data is loaded only when $\overline{CS}$ is low level.

Unipolar Output

DAC could drive 60kΩ unbuffered load. The unbuffer operation cause the power supply current (300uA type value) and offset error are all very low. The unipolar output range of the MS5541 is 0V to $V_{REF.}$ The figure 8 shows an typical unipolar output voltage circuit. The example diagram uses 2.5V reference and the MS8629, reference voltage buffer with low offset and zero drift.

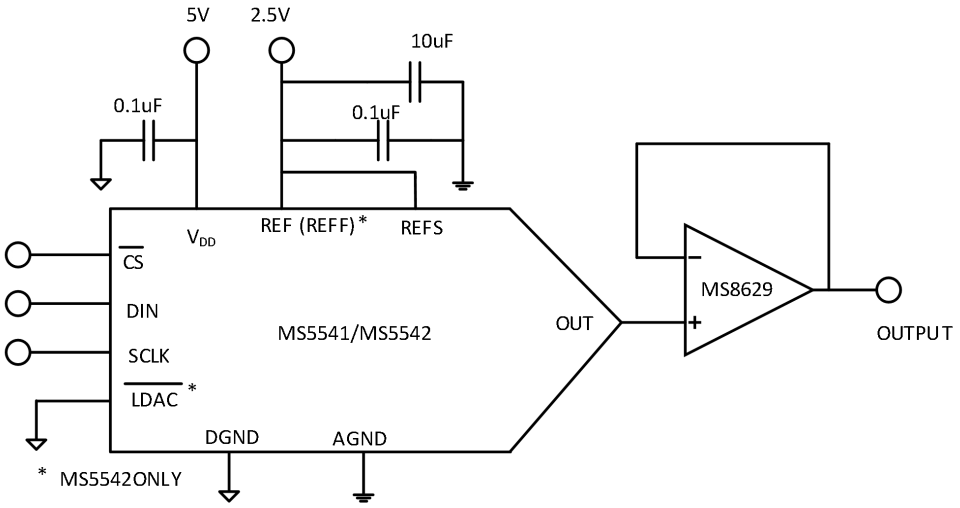


Figure 8. Unipolar Output Circuit

If ideal reference voltage source is used, the worst condition of unipolar output could be calculated as follows:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times \left(V_{REF} + V_{GE}\right) + V_{ZSE} + INL$$

$V_{OUT-UNI}$ is the worst condition of unipolar mode. D is the code loaded to DAC. V_{REF} is the reference voltage applied to device. V_{GE} is gain error with unit(V). V_{ZSE} is zero scale error with unit(V). INL is integral nonlinearity with unit(V).

Bipolar Output

For external operation amplifier, the MS5542 could provide bipolar output. The typical circuit is shown in figure 9. The feedback resistors, R_{INV} and R_{FB}, typical values of 28kΩ, are connected to input and output terminal of operation amplifier to achieve bipolar output.

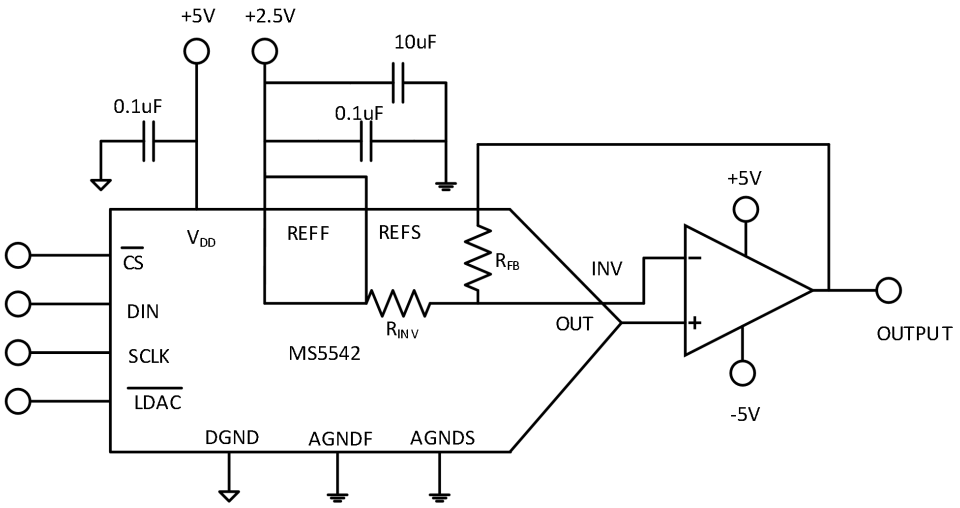


Figure 9. Bipolar Output Circuit

If ideal reference voltage source is used, the worst condition of bipolar output could be calculated as follows:

$$V_{OUT-BIP} = \frac{\left[\left(V_{OUT-UIN} + V_{OS}\right)\left(2+RD\right) - V_{REF}\left(1+RD\right)\right]}{1+\left(2+RD\right)/A}$$

V_{OUT-BI} is the worst condition of bipolar mode. $V_{OUT-UIN}$ is the worst condition of unipolar mode. V_{OS} is input offset voltage of external op. RD is the matched error of R_{FB} and $R_{INV.}$ A is open-loop gain.

TYPICAL APPLICATION

Layout Guide

In any circuit focusing on accuracy, it contributes to ensure specified performance that consider power and ground loop layout carefully. The PCB used by the MS5541/MS5542 should adopt the design where analog and digital parts are separated and limited to certain field. If several devices demand connection for analog and digital ground in the MS5541/MS5542 system, only one star point is made as close to the device as possible. The MS5541/MS5542 should have large enough 10μF power bypassing capacitance, which is paralleled with 0.1μF capacitance of each power. The 10μF capacitor is tantalum capacitor. And the 0.1μF capacitor should have low ESR and ESI, such as the ceramic capacitor, which provides low impedance ground path at high-frequency to process transient current caused by internal logic switch.

Opto-coupler Circuit

The MS5541/MS5542 is Schmitt-triggered digital input, which makes it receive slow digital transmission. Therefore, it is suitable in industrial application, which may need use opto-coupler to isolate DAC from controller. The figure 10 shows opto-coupler interface circuit.

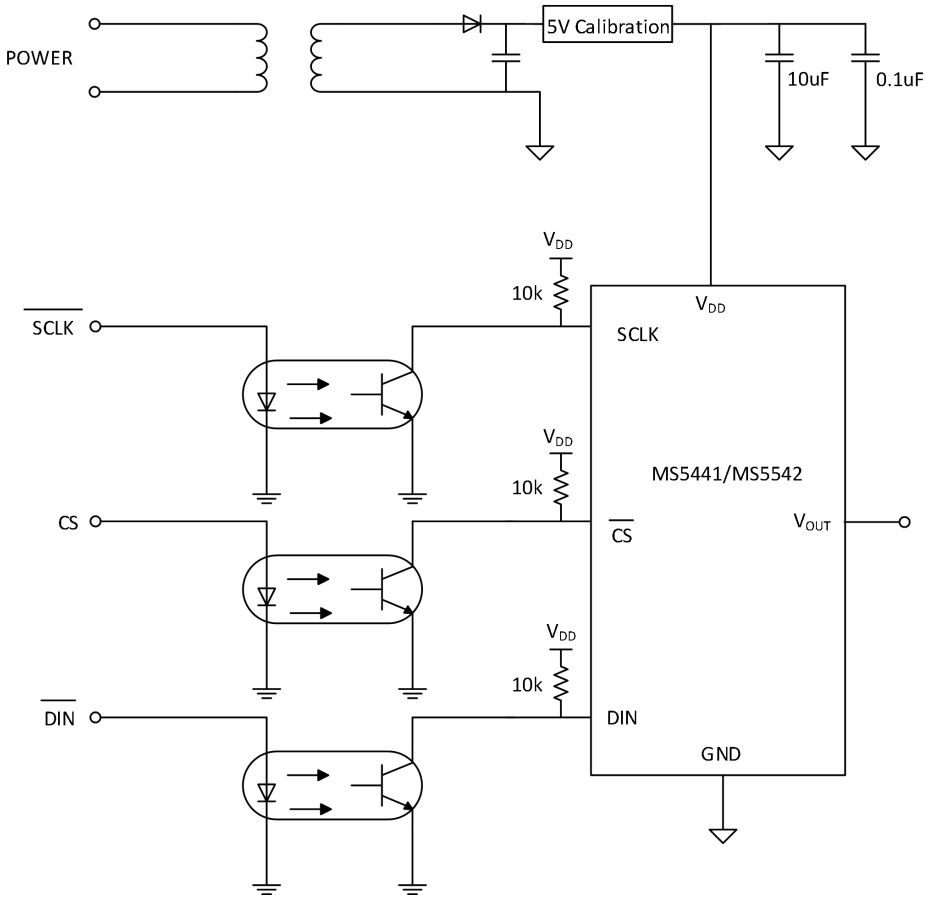


Figure 10. Opto-coupler Interface Circuit

Multi-channel Decoding Circuit

The MS5541/MS5542 has chip select pin $\overline{CS}$, which could choose one or several DACs. All devices receive the same serial clock and data, but only one device could receive $\overline{CS}$ signal at one time. The DAC address is decided by decoder. Digital feedthrough phenomenon exists in digital line. And using burst clock could reduce the effect on analog signal channel to a minimum. The typical circuit is shown in figure 11.

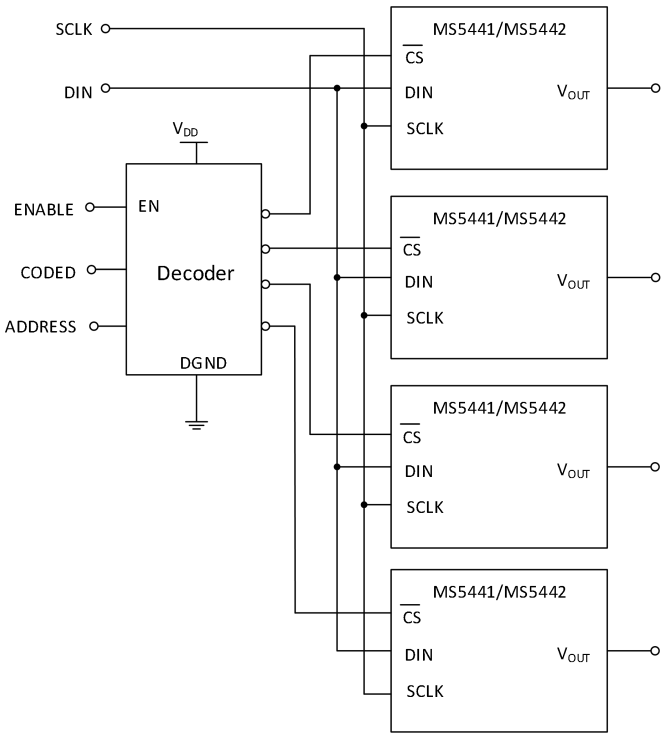
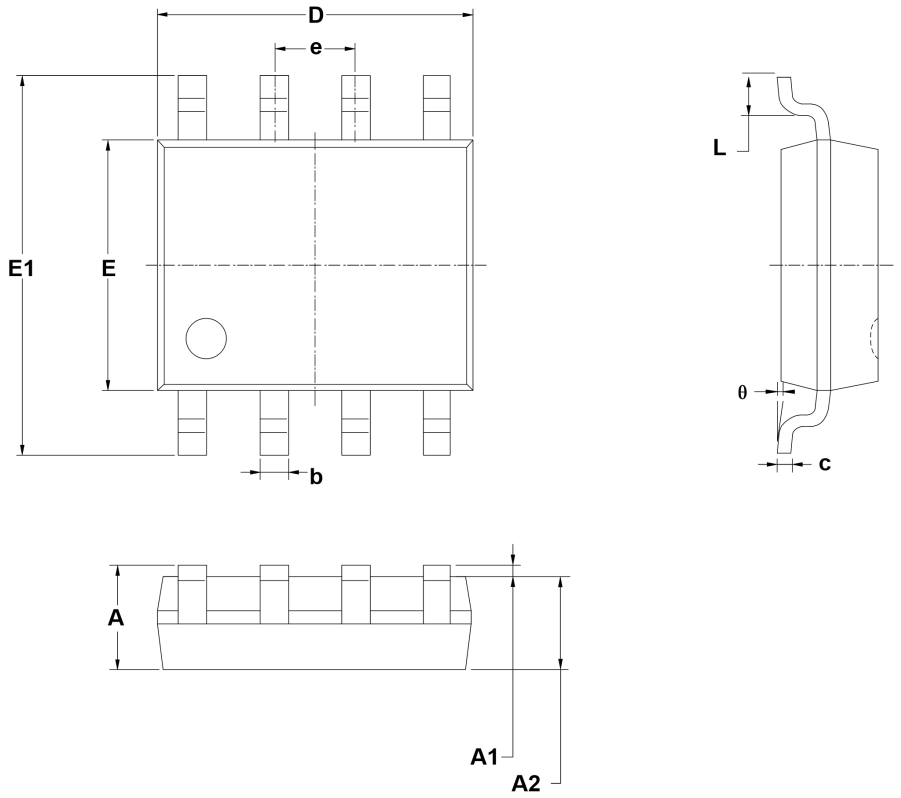


Figure 11. Multiple DACs

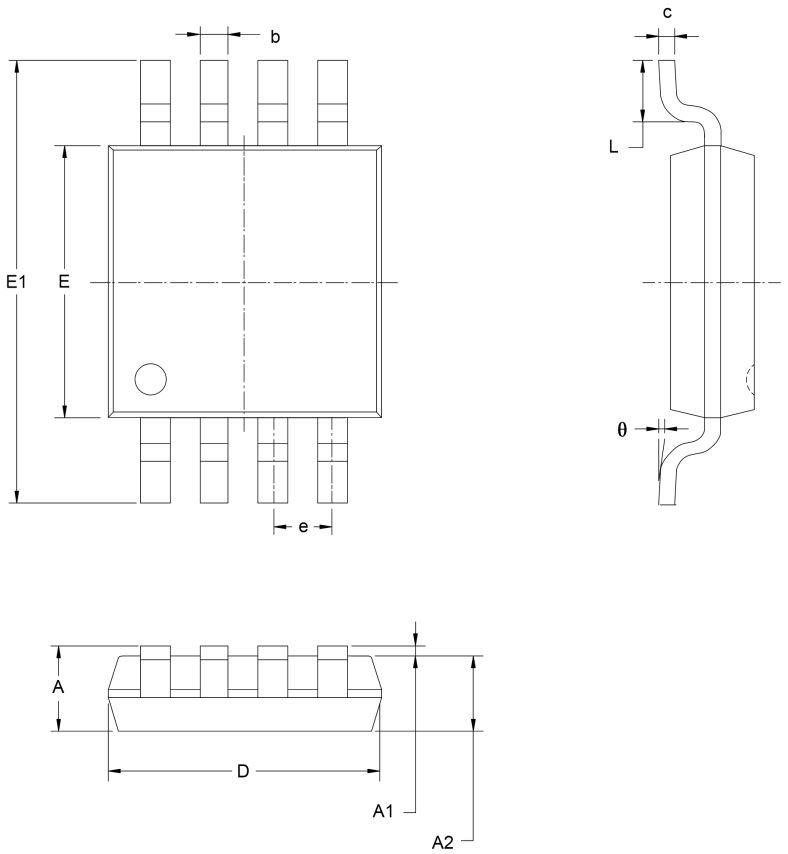
PACKAGE OUTLINE DIMENSIONS

SOP8



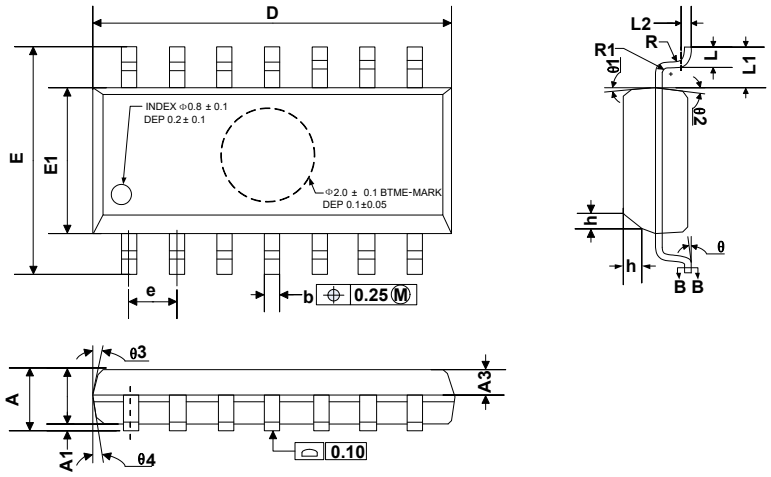
Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A			1.75
A1	0.10		0.225
A2	1.30	1.40	1.50
b	0.39		0.47
c	0.20		0.24
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27BSC		
L	0.50		0.80
θ	0		8°

MSOP8



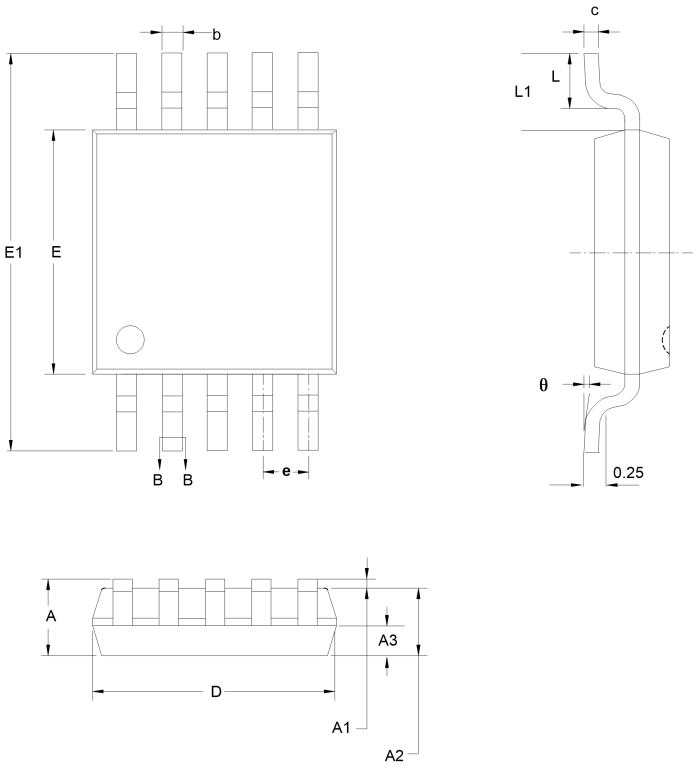
Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A			1.10
A1	0.05		0.15
A2	0.75	0.85	0.95
b	0.28		0.36
c	0.15		0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.65BSC		
L	0.40		0.70
θ	0		8°

SOP14



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	1.35		1.75
A1	0.10		0.25
A2	1.25		1.65
A3	0.55		0.75
D	8.53		8.73
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
L	0.45		0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07		
R1	0.07		
h	0.30		0.50
θ	0 °		8 °
θ1	6 °	8°	10 °
θ2	6 °	8°	10 °
θ3	5 °	7°	9 °
θ4	5 °	7°	9 °

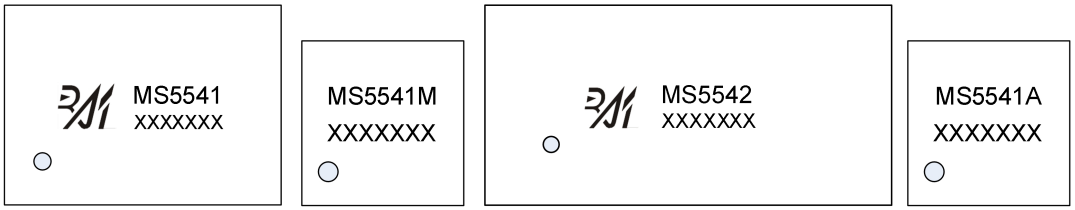
MSOP10



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A			1.10
A1	0.05		0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18		0.26
c	0.15		0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.50BSC		
L	0.40		0.70
L1	0.95REF		
θ	0		8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : MS5541, MS5541M, MS5542, MS5541A

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5541	SOP8	2500	1	2500	8	20000
MS5541M	MSOP8	3000	1	3000	8	24000
MS5542	SOP14	2500	1	2500	8	20000
MS5541A	MSOP10	2500	1	2500	8	20000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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