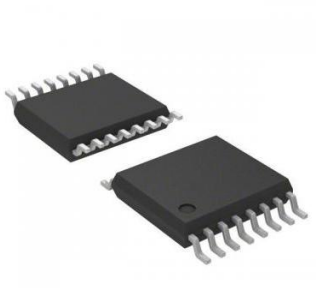
Single-Ended, 24-Bit, 96-kHz Stereo ADC

PRODUCT DESCRIPTION

The MS5358 is a high-performance,stereo A/D converter for audio applications. Its sample rate ranges from 8kHz to 96kHz. The MS5358 has high-accuracy feature achieved by using a delta-sigma modulator and a digital decimation filter. The audio interface has two modes (MSB Justified, I^2S) and is suitable for wide variety of cost-sensitive consumer applications requiring good performance.

The device is available in TSSOP16 package.



TSSOP16

FEATURES

- 24bit ADC
- Single-ended Input
- High Performance:
  THD+N: -92.5dB
  DR: 102dB
  S/N: 102dB
- Sampling Rate: 8kHz ~ 96kHz
- Master Clock:
  256fs/384fs/512fs/768fs (8kHz~48kHz)
  256fs/384fs (48kHz~96kHz)
- Digital Input Level: CMOS
- Master or Slave Mode
- Audio Interface: 24bit MSB Justified or I^2S
- Analog Power Supply：4.5V~5.5V
- Digital Power Supply：2.7V~3.6V
- Ambient Temperature: -40°C~105°C
- TSSOP16 Package

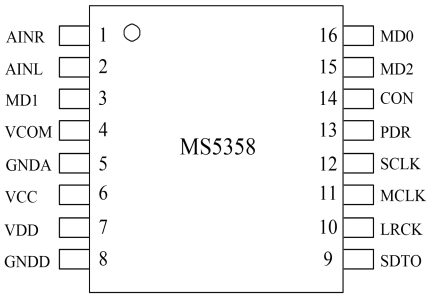
APPLICATIONS

- Audio Interface
- DTV, DVR and AV Receiver

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5358	TSSOP16	MS5358

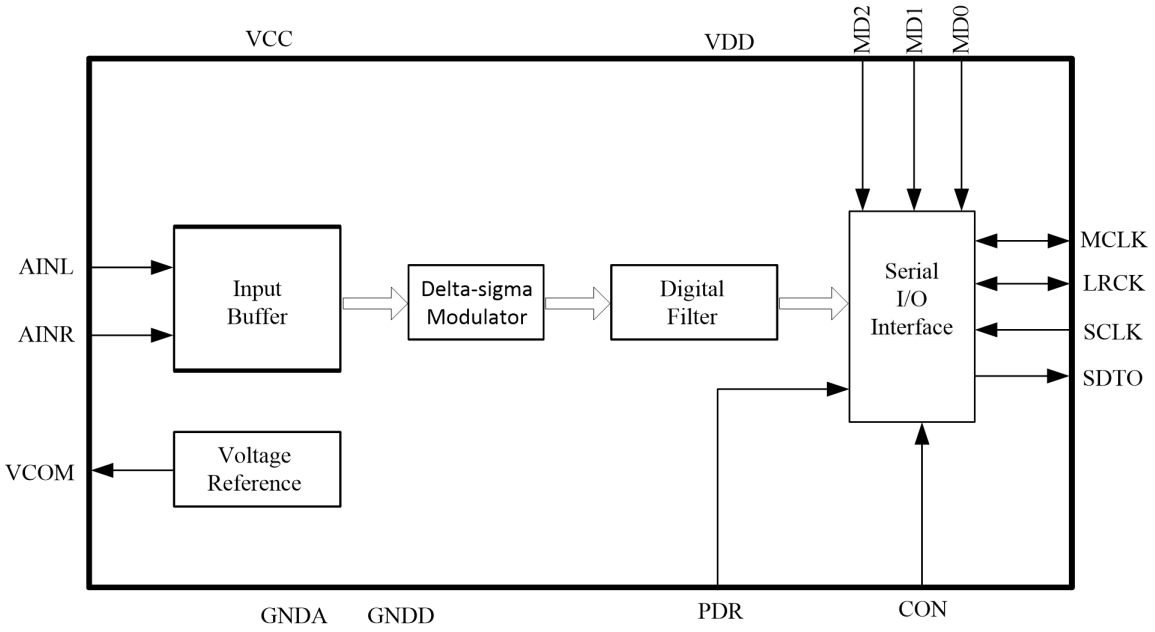
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	AINR	I	Rch Analog Input Pin
2	AINL	I	Lch Analog Input Pin
3	MD1	I	Mode Select 1 Pin
4	VCOM	O	Common Voltage Output Pin, VCC/2 Bias Voltage of ADC Input.
5	GNDA	-	Analog Ground Pin
6	VCC	-	Analog Power Supply Pin, 4.5 ~ 5.5V
7	VDD	-	Digital Power Supply Pin, 2.7 ~ 3.6V
8	GNDD	-	Digital Ground Pin
9	SDTO	O	Audio Serial Data Output Pin Low Output at Power Down Mode
10	LRCK	I/O	Output Channel Clock Pin Low Output at Power Down Mode in Master Mode
11	MCLK	I	Master Clock Input Pin
12	SCLK	I/O	Audio Serial Data Clock Pin Low Output at Power Down Mode in Master Mode
13	PDR	I	Power Down Mode & Reset Mode “H”: Power Up, ”L”: Power Down & Reset The MS5358 must be reset once after power-up.
14	CON	I	Audio Interface Type Select Pin “H”: 24bit IIS Compatible, ”L”: 24bit MSB Justified
15	MD2	I	Mode Select 2 Pin
16	MD0	I	Mode Select 0 Pin

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

GNDA, GNDD = 0V (1)

Parameter	Symbol	Range	Unit
Analog Power Supply	VCC	-0.3 ~ 6.0	V
Digital Power Suppl	VDD	-0.3 ~ 4.6	V
|GNDA – GNDD| (2)	ΔGND	0.3	V
Analog and Digital Input Current	IIN	±10	mA
Analog Input Voltage (AINL, AINR, MD1 pin)	AIN	-0.3 ~ VCC+0.3	V
Digital Input Voltage (3)	VIND	-0.3 ~ VDD+0.3	V
Ambient Temperature	Ta	-40 ~ 105	°C
Storage Temperature	Tstg	-65 ~ 150	°C

Note: (1) All voltages are relative to ground.

(2) GNDA and GNDD must be connected to the same analog ground plane.

(3) PDR, CON, MCLK, SCLK, LRCK, MD0, MD2 pin

ELECTRICAL CHARACTERISTICS

Recommended Operation Voltage

GNDA, GNDD = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Analog Power Supply	VCC	4.5		5.5	V
Digital Power Supply	VDD	2.7		3.6	V

Analog Characteristics

Ta=25°C; VCC=5.0V, VDD=3.3V; GNDA=GNDD=0V; fs=48kHz, 96kHz; SCLK = 64fs; Signal Frequency = 1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 40Hz~40kHz at fs=96kHz. Unless otherwise specified.

Parameter			Min	Typ	Max	Unit
ADC Analog Input Characteristics						
Resolution					24	Bits
Input Voltage (1)			2.7	3.0	3.3	Vpp
S/(N+D)	fs = 48kHz	-1dBFS	82	92.5		dB
	BW = 20kHz	-60dBFS		39		dB
	fs = 96kHz	-1dBFS		90		dB
	BW = 40kHz	-60dBFS		38		dB
DR (-60dBFS, A-weighted)			90	102		dB
S/N (A-weighted)			94	102		dB
Input Resistance	fs = 48kHz		13	20		kΩ
	fs = 96kHz		9	14		kΩ
Interchannel Isolation			89	95		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				100	-	ppm/°C
Power Supply Rejection (2)			-	50		dB
Power Supply						
Power Supply Current						
Normal Operation (PDR = "H")						
VCC				10	16	mA
VDD (fs = 48kHz)				2	5	mA
VDD (fs = 96kHz)				4	9	mA
Power Down Mode (PDR = "L") (3)						
VCC+VDD				10	100	uA

Note: (1) The value is full scale (0dB) of input voltage. Input voltage is in proportional to VCC,Vin=0.6*VCC (Vpp).

(2) PSR is applied to VCC and VDD with 1kHz, 50mVpp.

(3) All digital input pins and MD1 pin are held VDD or GNDD.

Filter Characteristics (fs=48kHz)

Ta = -40°C~100°C; VCC = 4.5V~5.5V; VDD = 2.7V~3.6V.

Parameter		Symbol	Min	Typ	Max	Unit
ADC Digital Filter (Decimation LPF)						
Passband (1)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband		SB	28			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay Distortion		ΔGD		0		us
Group Delay		GD		16		1/fs
ADC Digital Filter (HPF)						
Frequency Response (2)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz

Filter Characteristics (fs=96kHz)

Ta = -40°C~100°C; VCC = 4.5V~5.5V; VDD = 2.7V~3.6V

Parameter		Symbol	Min	Typ	Max	Unit
ADC Digital Filter (Decimation LPF)						
Passband (1)	±0.1dB	PB	0			kHz
	-0.2dB		-	40.0	37.8	kHz
	-3.0dB		-	46.0	-	kHz
Stopband		SB	56			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay Distortion		ΔGD		0		us
Group Delay		GD		16		1/fs
ADC Digital Filter (HPF)						
Frequency Response (2)	-3dB	FR		2.0		Hz
	-0.1dB			13.0		Hz

Note: (1) The passband and stopband frequencies change with fs.

For example, PB=18.9kHz@±0.1dB is 0.39375*fs

(2) The calculated delay time induced by digital filtering.

DC Characteristics (CMOS Level Mode)

Ta = -40°C~100°C; VCC = 4.5V~5.5V; VDD = 2.7V~3.6V

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	VIH	70%VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VDD	V
High-Level Output Voltage (Iout=-1mA)	VOH	VDD - 0.5	-	-	V
Low-Level Output Voltage (Iout=1mA)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	uA

Switching Characteristics

Ta = -40°C~100 °C; VCC = 4.5V~5.5V; VDD = 2.7V~3.6V; CL=20pF

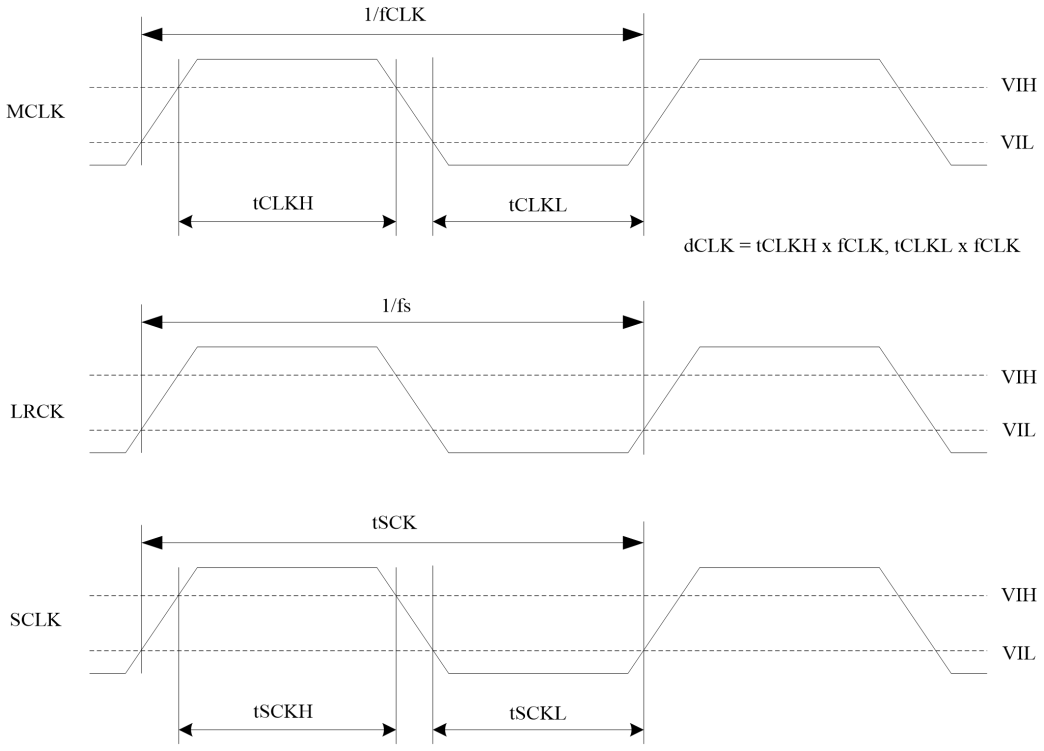
Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Timing					
512fs,256fs Frequency	fCLK	2.048		24.576	MHz
Duty	dCLK	40		60	%
768fs,384fs Frequency	fCLK	3.072		36.864	MHz
Duty	dCLK	40		60	%
LRCK Frequency	fs	8		96	kHz
Duty Slave Mode		45		55	%
Master Mode			50		%
Audio Interface Timing					
Slave Mode					
SCLK Period	tSCK	160			ns
SCLK Pulse Width Low	tSCKL	65			ns
Pulse Width High	tSCKH	65			ns
LRCK Edge to SCLK"↑" (1)	tLRSH	30			ns
SCLK"↑" to LRCK Edge (1)	tSHLR	30			ns
LRCK to SDTO(MSB) (Except I²S Mode)	tLRS			35	ns
SCLK"↓" to SDTO	tSSD			35	ns
Master Mode					
SCLK Frequency	fsCK		64fs		Hz
SCLK Duty	dSCK		50		%
SCLK"↓" to LRCK	tMSLR	-40		20	ns
SCLK"↓" to SDTO	tSSD	-40		35	ns
Reset Timing					
PDR Pulse Width (2)	tPD	150			ns
PDR"↑" to SDTO Valid at Slave Mode (3)	tPDV		4132		1/fs
PDR"↑" to SDTO Valid at Master Mode (3)	tPDV		4129		1/fs

Note: (1) SCLK rising edge must not occur at the same time as LRCK rising and falling edges.

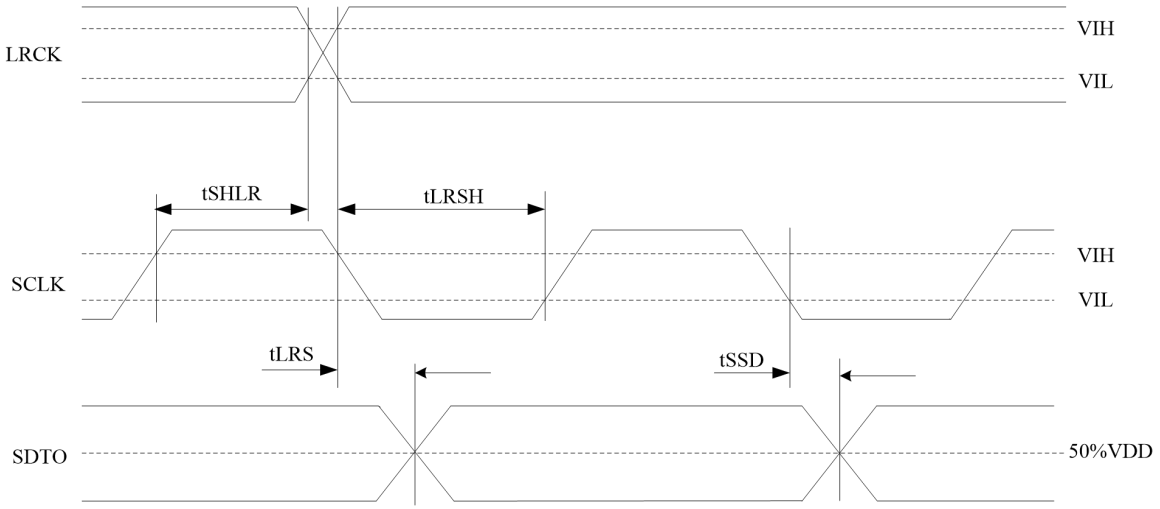
(2) The MS5358 can be reset with PDR="L"

(3) The period is the number of LRCK rising edges from the PDR = "H".

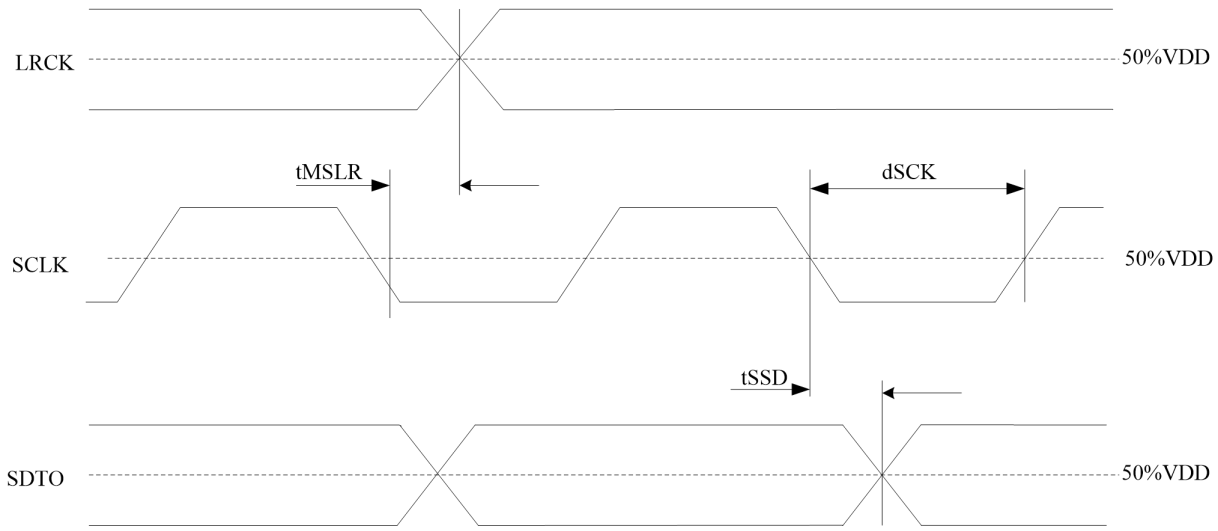
TIMING DIAGRAMS



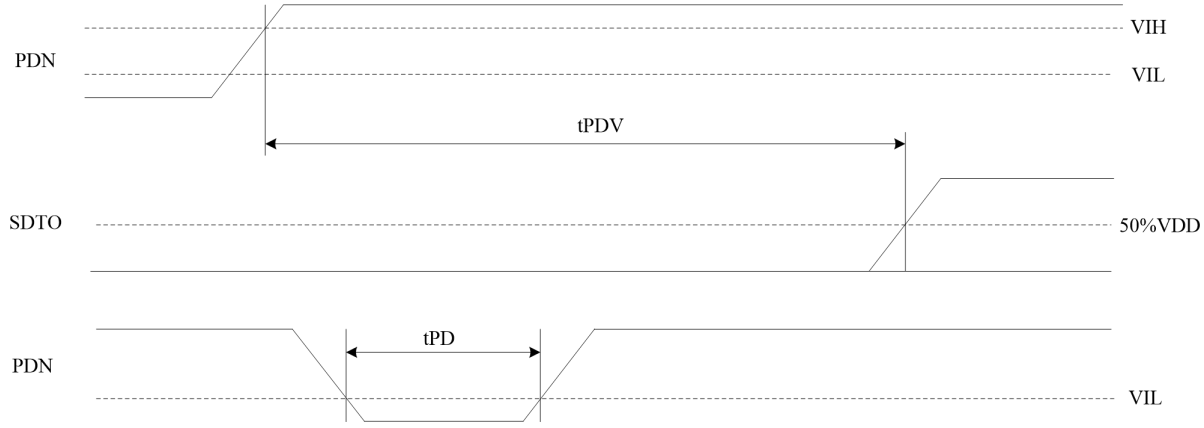
Clock Timing



Audio Interface Timing (Slave Mode)



Audio Interface Timing (Master Mode)



Power Down & Reset Timing

FUNCTIONAL DESCRIPTION

System Clock

In Slave mode, MCLK, SCLK and LRCK(fs) are required. LRCK must synchronize with MCLK. Table 1 shows typical relationship between sampling rate and MCLK. Table 2 shows MCLK, SCLK and master/slave controlled by MD2-0 pin. MCLK, SCLK and LRCK must exist unless PDR="L". If without these clocks, the MS5358 would absorb excess current due to using internal dynamically refreshed logic. If external clocks aren't present, the MS5358 needs to be set as power-down mode (PDR="L"). In master mode, MCLK must be provided unless PDR="L".

Table 1. System Clock Example

fs	MCLK			
	256fs	384fs	512fs	768fs
32kHz	8.192MHz	12.288 MHz	16.384 MHz	24.576 MHz
44.1kHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	33.8688 MHz
48 kHz	12.288 MHz	18.432 MHz	24.576 MHz	36.864 MHz
96 kHz	24.576 MHz	36.864 MHz	N/A	N/A

Table 2. Operation Mode Select

Mode	MD2	MD1	MD0	Input Level	Master/Slave	MCLK	SCLK
0	L	L	L	CMOS	Slave	256/384fs(8k≤fs≤96k) 512/768fs(8k≤fs≤48k)	≥48fs or 32fs (1)
1	L	L	H			Reserved	
2	L	H	L	CMOS	Master	256fs(8k≤fs≤96k)	64fs
3	L	H	H	CMOS	Master	512fs(8k≤fs≤48k)	64fs
4	H	L	L			Reserved	
5	H	L	H			Reserved	
6	H	H	L	CMOS	Master	384fs(8k≤fs≤96k)	64fs
7	H	H	H	CMOS	Master	768fs(8k≤fs≤48k)	64fs

Note: (1) SDTO outputs 16bit data at SCLK=32fs

Audio Interface Format

The two different data formats are selected by CON pins (Table 3). In both modes, the serial data format is MSB first and two's complement. SDTO clock outputs when the falling edge of the SCLK clock occurs. The audio interface supports two modes (master and slave mode). In master mode, SCLK and LRCK are output.The SCLK frequency is 64*fs , the LRCK frequency is 1*fs.

Table 3. Audio Interface Format

Mode	CON	SDTO	LRCK	SCLK	Figure
0	L	24bit, MSB Justified	H/L	≥48fs or 32fs	Figure 1
1	H	24bit, I²S Compatible	L/H	≥48fs or 32fs	Figure 2

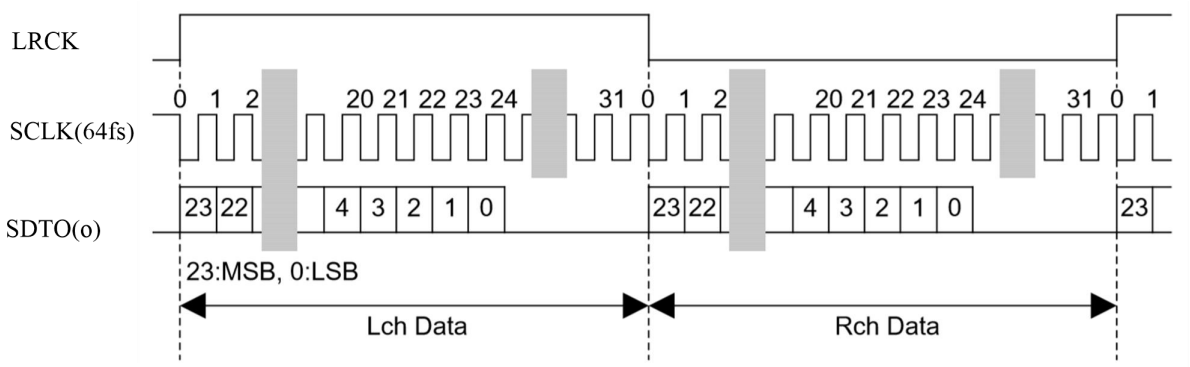


Figure 1. Mode 0 Timing

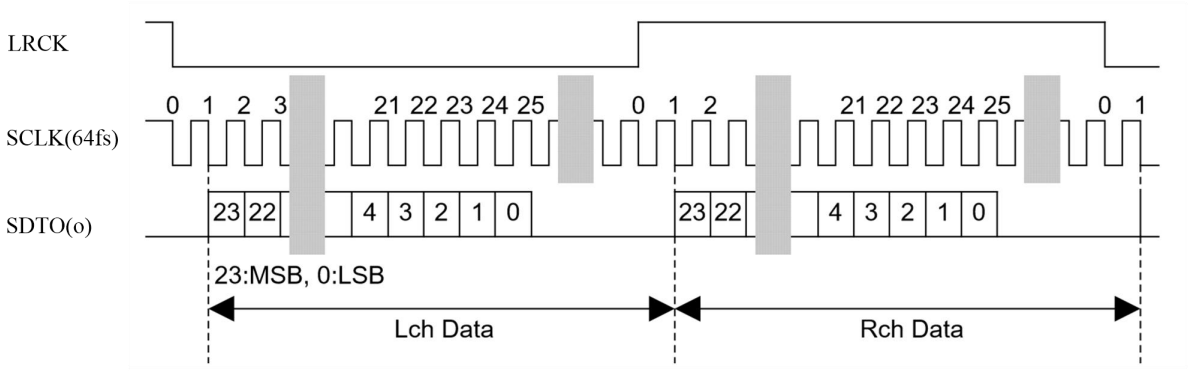
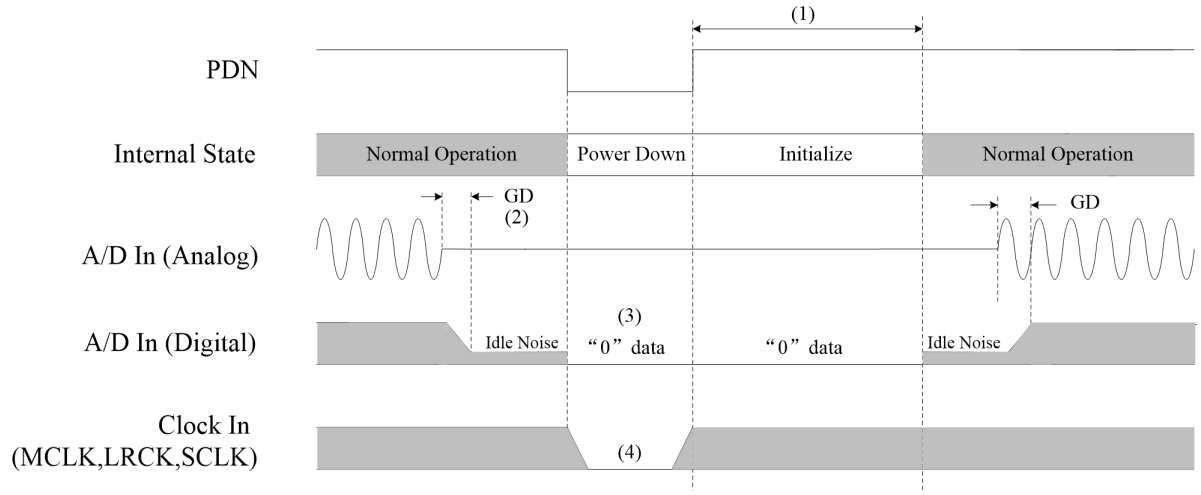


Figure 2. Mode 1 Timing

Power Down

When PDR="L", the MS5358 is set as power down mode, VCOM is set to GNDA level， and the digital filter is reset at the same time. Reset should be done after power up. Once the MS5358 exiting power down mode, An analog initialization period starts. During initialization, the ADC outputs are set as two's complement "0". After the end of start time, the ADC output gradually accord with corresponding input signals.



Note: (1) The time is 4132/fs in slave mode, 4129/fs in master mode.

(2) Digital output corresponding to analog input has the group delay (GD).

(3) A/D outputs "0" in power down state.

(4) When external clocks (MCLK, SCLK, LRCK) stop, the MS5358 should be in power down state.

System Reset

After power on, when PDN= "L", MS5358 will be reset immediately. In slave mode, the internal timing starts to work through the rising edge (falling edge in Mode 1) of LRCK after exiting reset and power down states. The MS5358 would stay in power down state unless LRCK is input. In master mode, the internal timing starts when MCLK is input.

System Design

Figure 3 shows the system typical connection diagram.

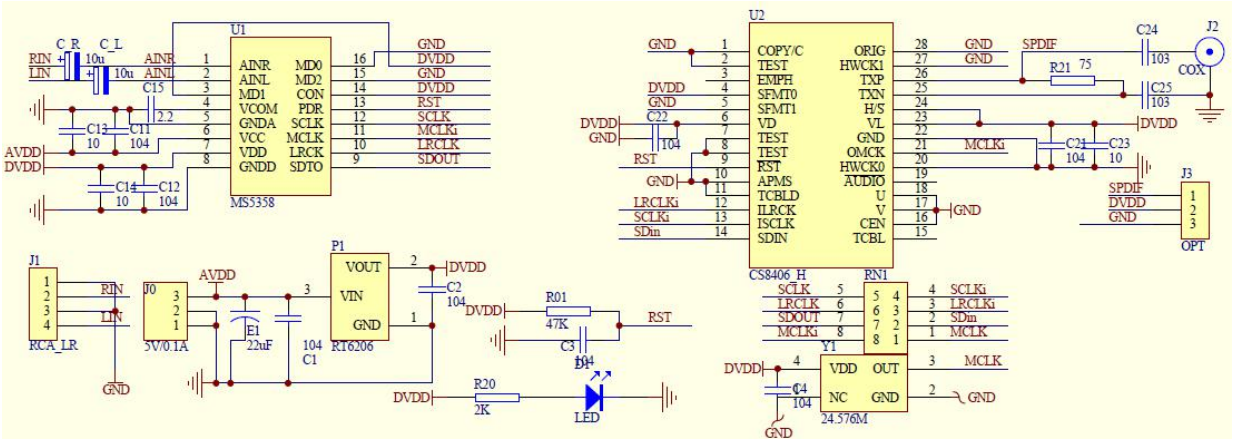


Figure 3. Typical Connection Diagram

Ground and Power Supply Decouple

MS5358 requires special careful power and ground arrangement. And if VCC and VDD are separated, the power up sequence is not the key. GNDA and GNDD must be connected on the same ground plane. The system analog ground and digital ground should be connected close to the power supply of the PCB ground. De-coupling capacitance should be placed as close to MS5358 as possible , and the small ceramic capacitor should be nearest.

Voltage Reference

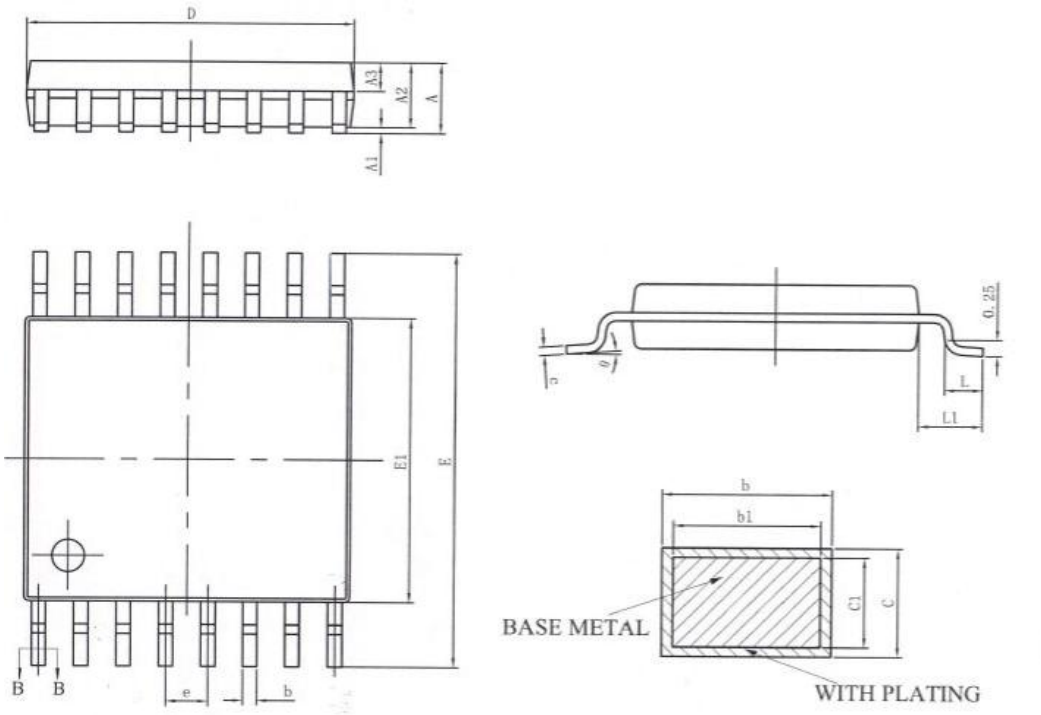
The analog voltage input range is set by VCC and VCOM is 50% VCC. A 2.2uF capacitor is attached to VCOM pin. In order to avoid needless coupling into the MS5358, all signals especially clock signals should be separate from VCOM pin.

Analog Input

The ADC inputs are single-ended and biased to VCOM with 20kΩ (typ@fs=48kHz).The input signal range changes with VCC, normally 0.6*VCC Vpp (typ). The ADC output data format is two's complement. The internal high pass filter eliminates DC offset.

PACKAGE OUTLINE DIMENSIONS

TSSOP16



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	-	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

MS5358： Product Name
XXXXXX： Product Code

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5358	TSSOP16	3000	1	3000	8	24000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

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