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MS2002EXP

DIGITAL SWITCH MODULE (DSM)

The Plessey MS2002 is an n-channel MOS LSI integrated circuit providing digital switching for 256 channels in PCM systems. The device is unidirectional in operation and is capable of switching data from any incoming channel to any outgoing channel. Input data can be either serial or parallel. The DSM is designed to be easily expandable to provide a greater switching capacity.

FEATURES

- Single 5V Supply
- TTL Compatible
- Interfaces Directly with European Standard CCITT 32 Channel 2.048Mb/s Format
- 256 Input/256 Output Channels
- Inputs and Outputs can be either Serial or Parallel
- Open Drain Outputs Allow Easy Expansion
- Only One System Clock Required with One Frame Synchronisation Pulse

APPLICATION

- Circuit Switched PCM or Data Systems

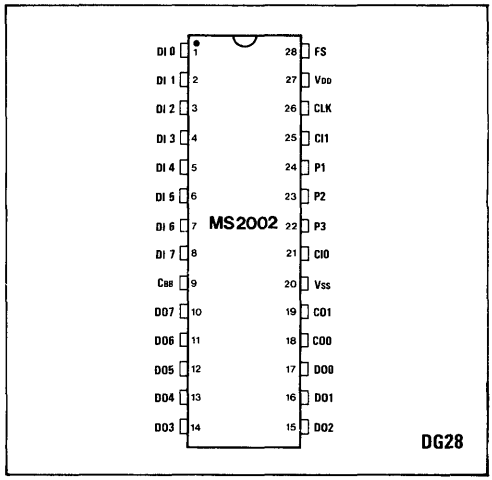


Fig.1 Pin connections - top view

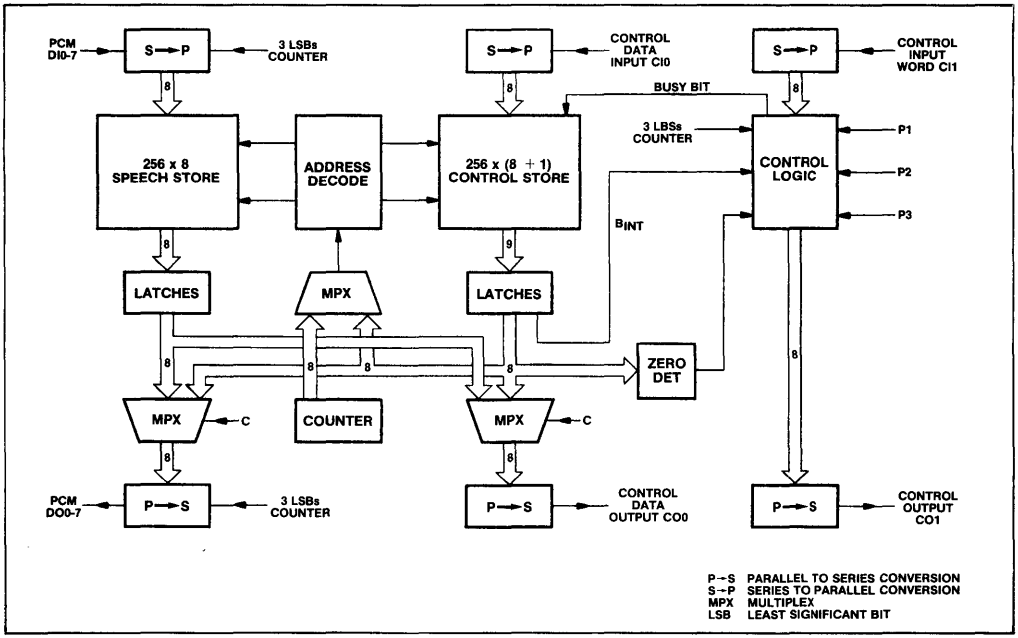


Fig.2 Block diagram of DSM

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	4.75	5	5.25	V	
High input voltage	V_{IH}	2.4		V_{DD}	V	
Low input voltage	V_{IL}	-0.5		0.8	V	
O/P pull up resistor	R_{PU}	950			Ω	+1 Schottky load
C_{BB} capacitor			1		nF	

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, T_{amb} = 25° C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		40		mA	
Input current	I_{IH}			50	μA	V_{IH} = 2.7V Logic
	I_{IL}			50	μA	V_{IL} = 0.4V inputs
Output voltage	V_{OH}	2.7			V	R_{PU} = 1kΩ Logic
	V_{OL}			0.5	V	R_{PU} = 1kΩ outputs
Input capacitance	C_i			5	pF	Logic inputs
Output capacitance	C_o			5	pF	Logic outputs

AC CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0° C to +70° C, V_{DD} = 5V ± 5%)

Characteristic	Symbol	Value		Units
		Min.	Max.	
System clock period	t_c	243	245	ns
System clock low period	t_{cl}	82		ns
System clock high period	t_{ch}	82		ns
Frame sync period	t_f	512	512	Clock periods
Frame sync set up time	t_{fss}	60		ns
Frame sync hold time	t_{fsh}	90		ns
Input data set up time	t_{ds}	60		ns
Input data hold time	t_{dh}	90		ns
Clock to output delay *	t_{cd}	5	150	ns

* Loaded with 7 similar outputs + 1 Schottky TTL input + 1kΩ pull up resistor to V_{DD} + 16pF.

PIN NAMES

DI0-7	Speech data input channels
DO0-7	Speech data output channels
CO0	Control data out
CO1	Control word out
CI0	Control data in
CI1	Control word in
P1-3	Programming pins
CLK	Clock
FS	Frame sync. pulse
V_{SS}	Negative supply (0V)
V_{DD}	Positive supply (5V)
C_{BB}	Substrate bias decoupling

ABSOLUTE MAXIMUM RATINGS

Supply voltage range (V_{DD})	-0.5V to +7V
Input voltage	-0.5V to +7V
Output voltage	-0.5V to +7V
Temperature: Storage	-65° C to +150° C
Operating	0° C to +70° C

NOTE
All voltages with respect to V_{SS}

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
DI0-DI7	1-8	**Speech Data Inputs** accept the 256 incoming speech channels at a 2.048Mb/s data rate and are latched on every alternate negative edge of the 4.096MHz system clock. The eight data bits of each channel may be arranged in serial format with each input line carrying 32 time multiplexed channels in standard CCITT PCM format. Frame and bit synchronisation is provided by the negative edge of FS as shown in Fig.4. The eight lines must be time slot synchronous with each other. Alternatively the speech data may be arranged in 8 bit parallel format, the eight input lines now operating as an eight bit wide bus carrying 256 consecutive channels. Channel 0 appears on the first negative edge of the clock after the FS negative transition as shown in Fig.4. The width of the frame sync. pulse FS is used to select the required format as shown in Table 2.
C_{BB}	9	**Substrate Bias Decoupling** for the -2.7V on-chip substrate bias generator is provided by a single capacitor between this pin and V_{SS}.
DO0-DO7	17-10	**Speech Data Outputs** carry the 256 switched outgoing speech channels at a 2.048Mb/s rate. As with the speech data inputs the data may be arranged in either serial or parallel format, the frame sync. pulse FS width designating the selected mode. The outgoing channels are delayed by 21 bit periods with respect to the incoming lines and are timed by the negative clock edges alternate to those used for input data. The timing relationships are shown in Fig.4. The speech data outputs use open drain drivers allowing wire OR-ing of up to 8 DSMs. The correspondence of the Speech and Control store data as seen at the Speech data outputs is shown in Fig.5(a).
CI0	21	**Control Data Input** allows updating of control memory contents (excluding B_{int}). Data format is 8 bit serial at a 2.048Mb/s rate. Thirty two words are received per frame, the frame sync. pulse designating the first bit (MSB) of the first word, as shown in Fig.4. Each Control Data word corresponds to a specific output channel and carries the number (in bit inverted format) of the input channel which is to be switched to that output. The format of the Control data input is shown in Fig.5(b). The numbering system for incoming channels is shown in Fig.5(a). The Control Data words are written to the appropriate locations in the control store determined by the current state of the Control Word CI1, received on pin 25, and the timeslot (0-31) in which the Control Data is received. The address construction is shown below (Outgoing Channel Address Construction). Table 1 shows those conditions under which a control store modification occurs.
CI1	25	**Control Word Input** accepts 8 bit serial data, word synchronised with the Control Data input CI0, thirty two Control Words being received per frame. Each Control Word corresponds to and controls the processing of the 8 bits of Control Data (CI0) received in the same timeslot on pin 21. The Control Word format is shown below. **CONTROL WORD FORMAT** (MSB) S3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$ W BEXT S2 S1 (LSB) (T = Φ) The outgoing speech channel address to which the present Control Data relates is determined by the combination of the present timeslot number (0-31 represented as a 5 bit number TS0-TS4) and the bits A0-A2 of the present Control Word as shown below. **OUTGOING CHANNEL ADDRESS CONSTRUCTION** (MSB) TS4 TS3 TS2 TS1 TS0 A2 A1 A0 (LSB) The remaining bits of the Control Word have the following functions: S1-S3 allows the message to be addressed to a specific DSM. These bits are compared with the status of the 3 Programming Pins P1-P3. W indicates whether the present operation is a control store write (W = 0) or a speech/control store read (W = 1) operation. B_{ext} is the external busy bit. If the operation is a control store write to this DSM then B_{ext} replaces the control store busy bit (B_{int}) for this channel, setting the channel to busy (B_{ext} = 0), or free (B_{ext} = 1) status. If the operation is a read then(B_{ext} = 1) data is to be read. The flow diagram of Fig.3 gives the precise interpretation of the control word.
CO0	18	**Control Data Output** allows interrogation of control or speech store contents. Data output is 8 bit serial with 32 words per frame. Each outgoing word corresponds to an incoming Control Data word but is delayed from it by 21 bit periods. The precise contents of each outgoing word are determined by the state of the related incoming Control Word CI1 as shown in the flow diagram of Fig.3. The Control Data Output uses an open drain driver allowing wire OR-ing of up to 8 DSMs.
CO1	19	**Control Word Out** is a reflection of the input Control Word delayed by 21 bit periods. The S1-S3 and B_{ext} bits may be modified depending on the internal state of the DSM, details are shown in Fig.3. The CO1 uses an open drain driver allowing wire OR-ing of up to 8 DSMs.

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
P1-P3	22-24	**Programming Pins** allow up to 8 DSMs to share a common control highway (CI0,CI1) and simplify the control structure when arrays of DSMs are used to construct larger switches. The Programming Pins should be hardwired to V_{SS} or V_{DD} to give each DSM a unique address. The state of the P1-P3 pins in combination with the S1-S3 and W bits (Control Word Format) of the control word determine how the control store is modified and also influence the contents of the outgoing CO0 and CO1 words. The complete control flow is shown in Fig.3. Table 1 summarises the effects on the control memory.
CLK	26	**Clock** input requires a 4.096MHz TTL level signal. All input signals are strobed in on alternate negative clock edges, the active edge being denoted by the position of the frame sync. signal FS, as shown in Fig.4.
FS	28	**Frame Sync.** provides a frame datum for the incoming data (both speech and control), marks the active edge of the system clock, and controls the speech input and output formats (serial or parallel) Fig.4 shows the timing relationship of the frame sync. signal to clock and data. The duration of the frame sync. low period determines the I/O format as shown in Table 2. Following a change in I/O mode the operation of the DSM is undefined for the remainder of that frame and the whole of the following frame.

W	S3 = P3	S2 = P2	S1 = P1	Action on Control Store
0	1	1	1	CI0→Control Store, BEXT→BINT
0	1	0	1	*FF→Control Store, 1→BINT
0	1	1	0	*FF→Control Store, 1→BINT
0	1	0	0	*FF→Control Store, 1→BINT
X	0	X	X	No action on Control Store
1	X	X	X	No action on Control Store

Table 1 Control Store modification

*Denotes hexadecimal notation.

Low period *	I/O format
1	SISO
2	SIPO
3	PISO
4	PIPO

Table 2 I/O format control

*Low period is shown in multiples of 4.096MHz system clock periods.

OPERATION

The DSM (block diagram is shown in Fig.2) is a 256 channel non-blocking digital switch capable of connecting all 256 incoming channels to all 256 outgoing channels in any desired order. Alternatively, selected input channels may be broadcast to any number of output channels. Each output channel may, however, receive from only one input channel at a time, i.e. conferencing facilities are not provided. Speech input to the device is via 8 lines (DI0-DI7) that can accept 8 bit data in either serial or parallel format at a 2.048Mb/s rate. Speech output is via a further 8 lines which may be set independently of the input lines to give out serial or parallel format data.

Call routings are held in an on-chip control memory in the form of a nine bit word for each outgoing speech channel, bit nine (B_{int}) indicating the busy status of the channel (0 = busy). In the case of a busy outgoing channel the remaining eight bits denote the number of the input channel to be connected to that outgoing channel. The numbering system for incoming channels is shown in Fig.5(a). If B_{int} indicates the channel is free then the remaining eight bits of the control word are used as the contents of the outgoing channel, hence allowing free choice of idle code. The contents of the control store can be modified, and speech or control store interrogated, via control messages received over the control interface CI0, CI1. Data generated by interrogation of either the control or speech memories appears on the two control output lines CO0, CO1.

SPEECH PATH DELAY CHARACTERISTICS

The switching function of the DSM is achieved by storing the incoming speech channels sequentially in the 256 x 8 speech memory (after conversion to parallel format) and then sending them to the output channels in the order specified by the control memory. The delay encountered by each channel consists of a fixed delay, determined by the format conversion circuitry and the memory read/write cycle time, and a variable delay determined by the time spent in memory waiting for the relevant outgoing timeslot. The delay is given by the relations:

$$\left.\begin{array}{l} D = 21 + (N - M) \text{ for } N \geqslant M \\ D = 277 + (N - M) \text{ for } N < M \end{array}\right\} \text{PIPO format}$$

$$\left.\begin{array}{l} D = 21 + (\text{INT}\frac{N}{8} - \text{INT}\ ) \times 8\ N \geqslant M) \\ D = 277 + (\text{INT}\frac{N}{8} - \text{INT}\ ) \times 8\ N < M \end{array}\right\} \text{SISO format}$$

where D = delay in bit periods (488ns)
M = incoming channel No. (as shown in Fig.5)
N = outgoing channel No.

CONSTRUCTION OF 512 CHANNEL SWITCH

Fig.6 demonstrates the use of the address facilities of the DSM control structure to build larger switches (512 channels in this case). The four devices share common control and speech highways, each device being assigned a unique address designated by the programming pins P1-P3. It should be noted that devices sharing a common output highway have been allocated a common value for P3. This allocation of addresses reduces the number of control messages required to set up or clear down calls as inspection of table 1 reveals; a message sent to one DSM setting or clearing a channel will automatically clear the same channel on any DSM which outputs to the same highway (has the same P3 value).

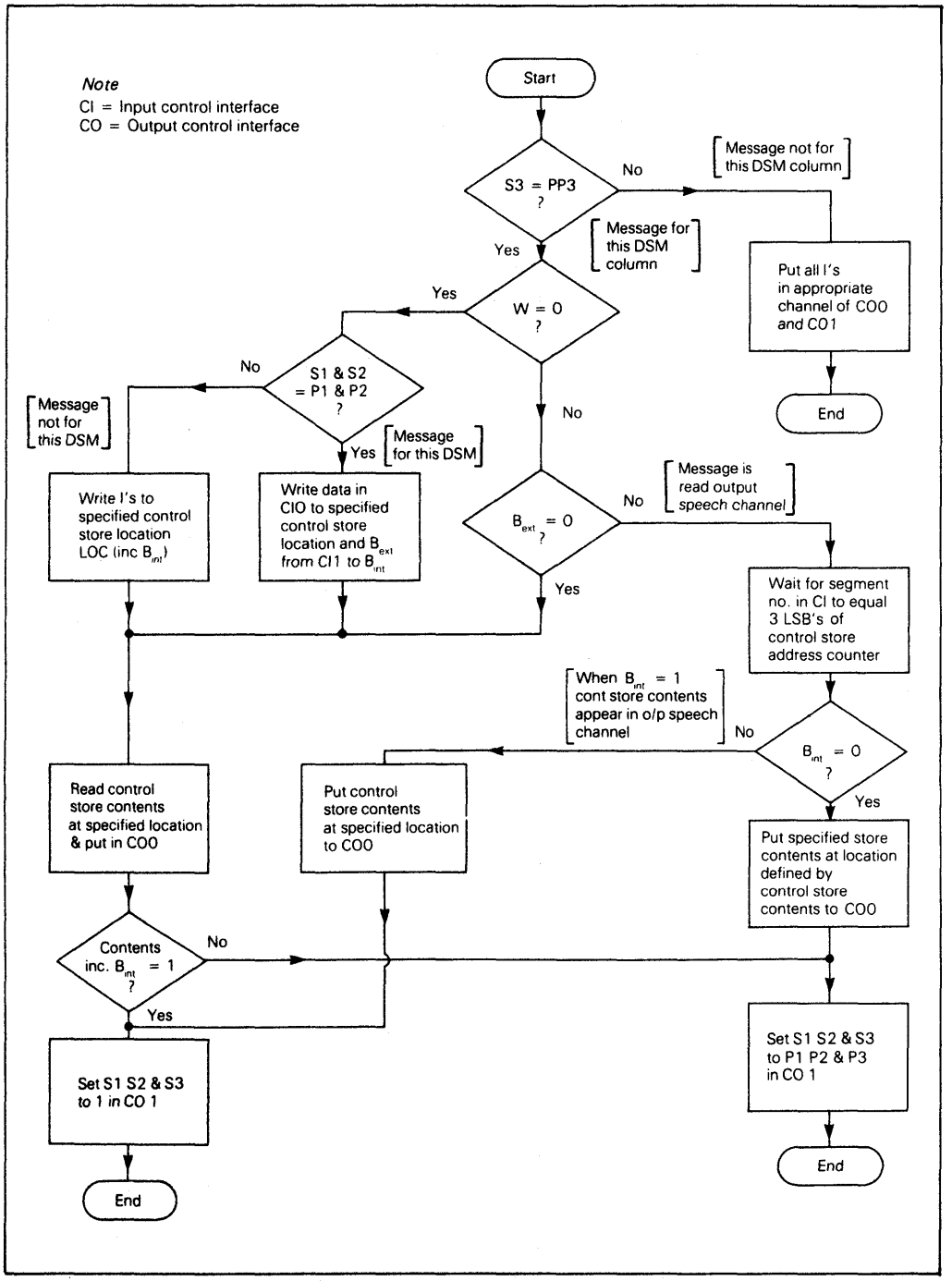
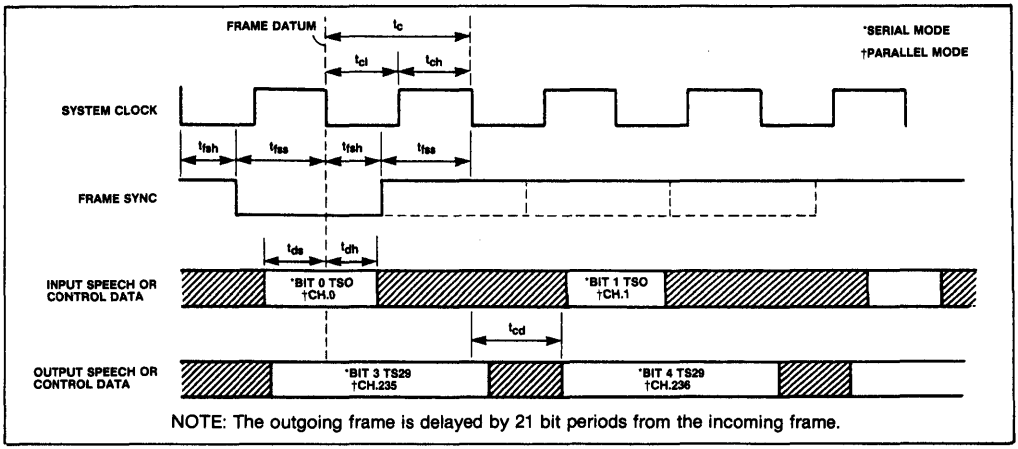


Fig.3 DSM control logic flowchart



NOTE: The outgoing frame is delayed by 21 bit periods from the incoming frame.

Fig.4 Clock, data, and frame sync timing relationships

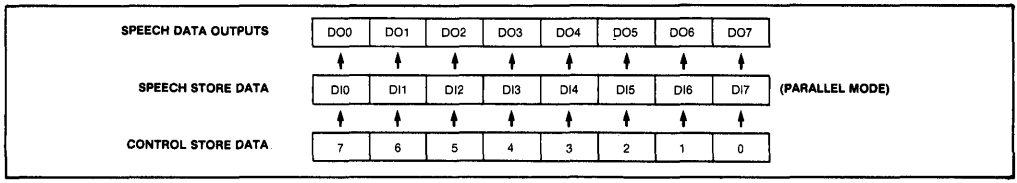


Fig.5(a) Correspondence of Speech and Control data

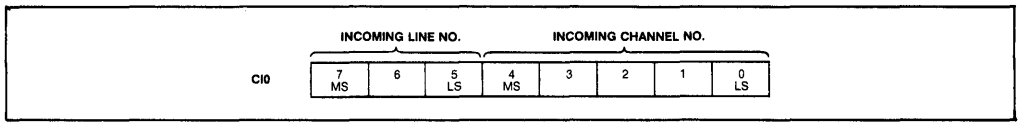


Fig.5(b) Format of Control data input

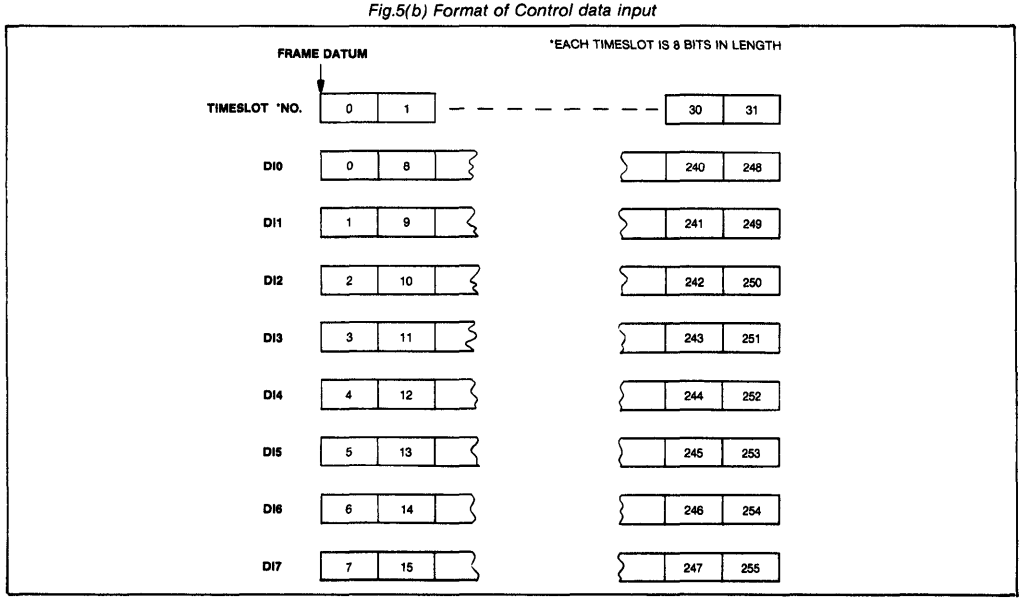


Fig.5(c) Channel numbering for incoming speech data (serial mode)

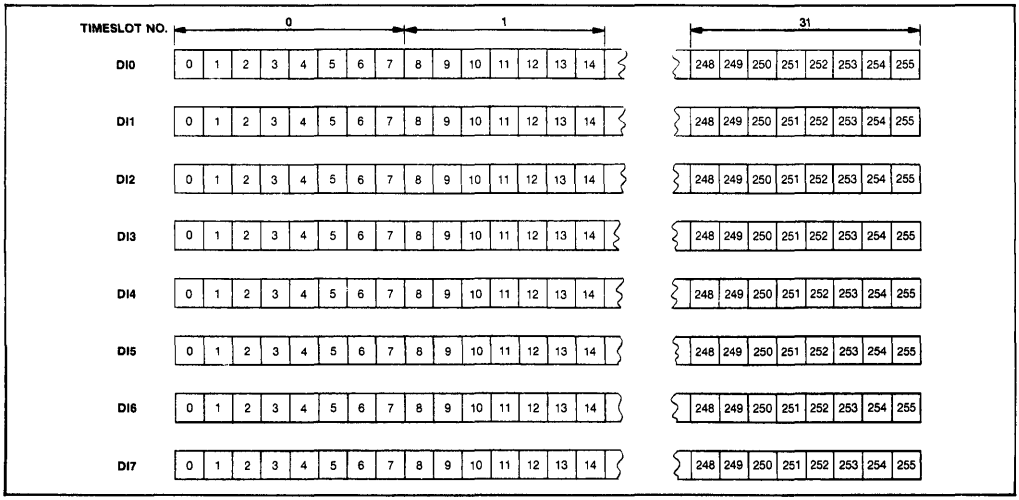


Fig.5(d) Channel numbering for incoming speech data (parallel mode).

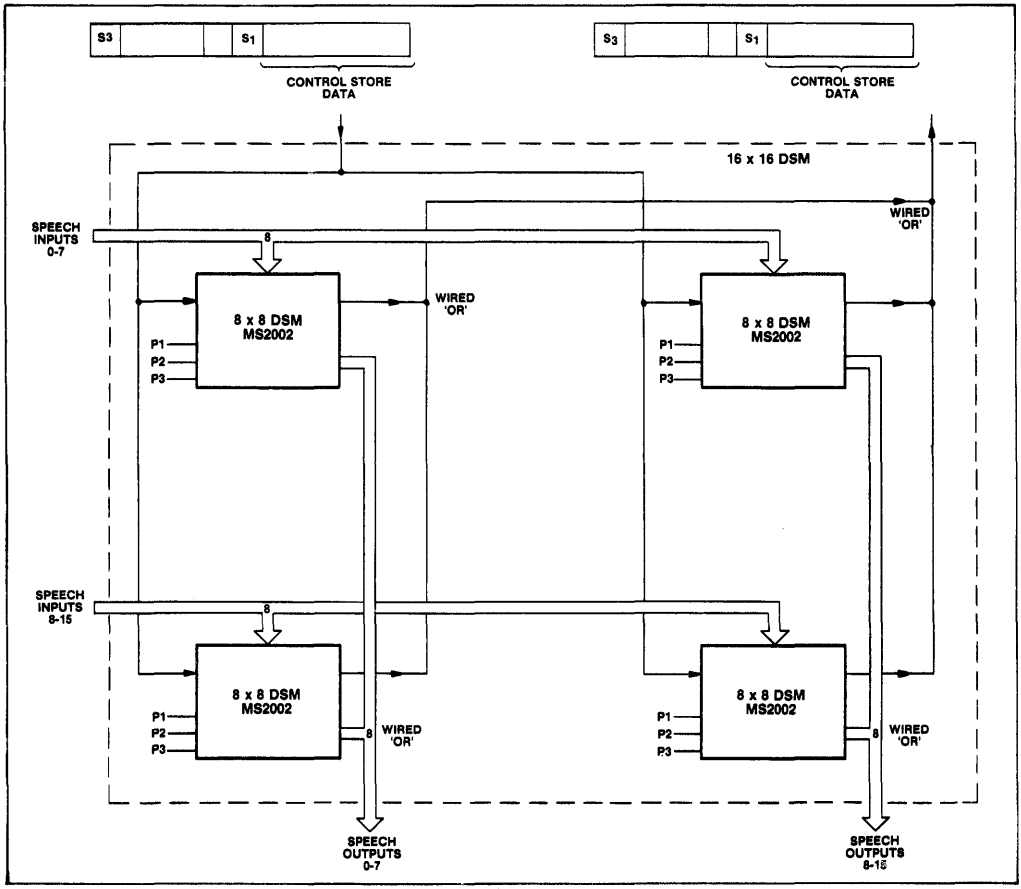


Fig.6 512 channel DSM made from four 8 x 8 DSMs