

N-Channel 30-V (D-S) MOSFET

Description

These miniature surface mount MOSFETs utilize High Cell Density process. Low rDS(on) assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are lower voltage application, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones

Features

- · Low rDS(on) trench technology
- · Fast switching speed
- · Low thermal impedance
- · RoHS compliant package

Applications:

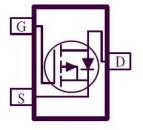
- · Power Routing
- · Li Ion Battery Packs
- · Level Shifting and Driver Circuits

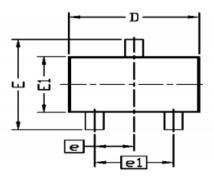
Packing & Order Information

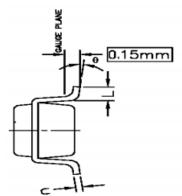
3,000/Reel

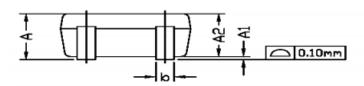


Graphic symbol









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES				
SIMBULS	MIN	NOM	MAX	MIN	NOM	MAX		
Α			1.10			0.043		
A1	0.00		0.10	0.00		0.004		
A2	0.7	0.9	1.00	0.028	0.035	0.039		
ь	0.15		0.30	0.006		0.012		
C	0.08		0.22	0.003		0.009		
D	1.85	2.10	2,15	0.073	0.083	0.085		
Е	1.80	2.30	2.40	0.071	0.091	0.094		
е		0.65 BSC		0.026 BSC				
el	1.30 BSC			0.051 BSC				
E1	1.1	1.30	1.4	0.043	0.051	0.055		
L	0.26	0.36	0.46	0.010	0.014	0.018		
θ	0°	4°	8°	0°	4°	8°		



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T _A =25°C unless otherwise specified)						
Symbol	Parameter	Value	Unit			
V_{DS}	Drain-Source Voltage	30	V			
V_{GS}	Gate-Source Voltage	±20	V			
1	Continuous Drain Current ^a (T _A =25°C)	2.0	Α			
ID	Continuous Drain Current _a (T _A =70°C)	1.6	Α			
I _{DM}	Pulsed Drain Current ^b	10	Α			
Is	Continuous Source Current (Diode Conduction) ^a	0.45	Α			
D	Power Dissipation ^a (T _A =25°C)	0.34	W			
P_{D}	Power Dissipation ^a (T _A =70°C)	0.22	W			
T _J /T _{STG}	Operating Junction and Storage Temperature	-55 to +150	°C			

Thermal Resistance Ratings						
Symbol	Parameter	Maximum	Units			
R _{THJA}	Maximum Junction-to-Ambient C/W ^a (t <= 10 sec)	375	°C/W			
	Maximum Junction-to-Ambient C/W ^a (Steady-State)	430	C/VV			

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Static						
Symbol	Parameter	Test Conditions	Min	Тур.	Max.	Units
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	1			V
I _{GSS}	Gate-Body Leakage	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			1 10	uA
I _{D(on)}	On-State Drain Current ^A	V _{DS} = 5 V, V _{GS} = 10 V	3			Α
R _{DS(on)}	Drain-Source On-Resistance ^A	$V_{GS} = 10 \text{ V}, I_D = 1.6 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 1.3 \text{ A}$			58 82	mΩ
g _{fs}	Forward Tranconductance ^A	V _{DS} = 15 V , I _D = 1.6 A		4		S
V _{SD}	Diode Forward Voltage	I _S = 0.25 V , V _{GS} = 0 V		0.74		V

Dynamic ^b							
Symbol	Parameter	Test Conditions	Min	Тур.	Max.	Units	
$t_{d(on)}$	Turn-On Delay Time			4		ns	
t _r	Rise Time	$\begin{split} V_{DS} &= 15 \text{ V }, \text{ R}_{L} = 9.4 \Omega, \\ V_{GEN} &= 10 \text{ V }, \text{ R}_{GEN} = 6 \Omega \\ I_{D} &= 1.6 \text{ A} \end{split}$		7		ns	
$t_{d(off)}$	Turn-Off Delay Time			19		ns	
tf	Fall Time			5		ns	



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Dynamic ^b							
Symbol	Parameter	Test Conditions	Min	Тур.	Max.	Units	
Q_g	Total Gate Charge	$V_{DS} = 15 \text{ V}, I_{D} = 1.6 \text{ A}$ $V_{GS} = 4.5 \text{ V}$		5.9		nC	
Q _{gs}	Gate-Source Charge			2.1		nC	
Q_{gd}	Gate-Drain Charge	V _{GS} = 4.5 V		2.1		nC	
C _{ISS}	Input Capacitance	V _{GS} = 0 V , V _{DS} = 15 V , f = 1MHz		513		pF	
Coss	Output Capacitance			69		pF	
C _{RSS}	Reverse Transfer Capacitance	VDS - 13 V , 1 - 11VII 12		54		pF	

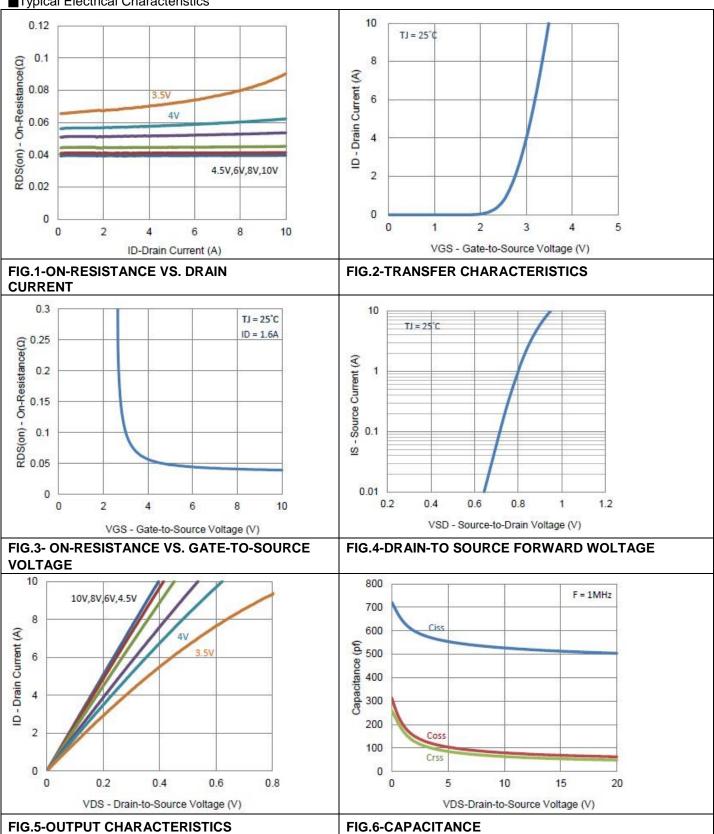
Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.



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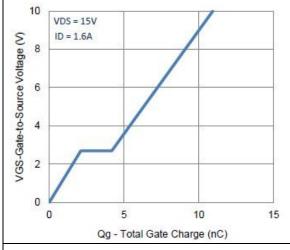






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■Typical Electrical Characteristics



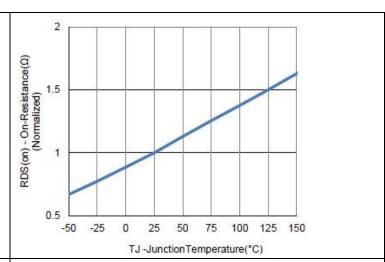


FIG.7-GATE CHARGE

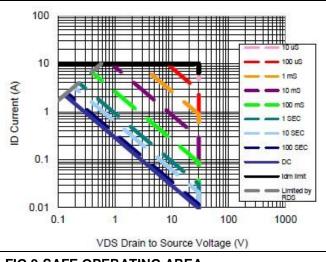


FIG.8-NORMALIZED ON-RESISTANCE VS JUNCTION TEMPERATURE

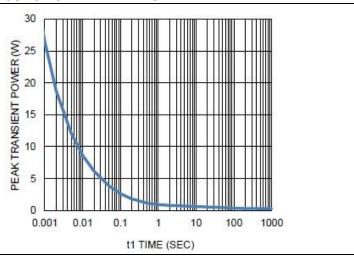


FIG.9-SAFE OPERATING AREA



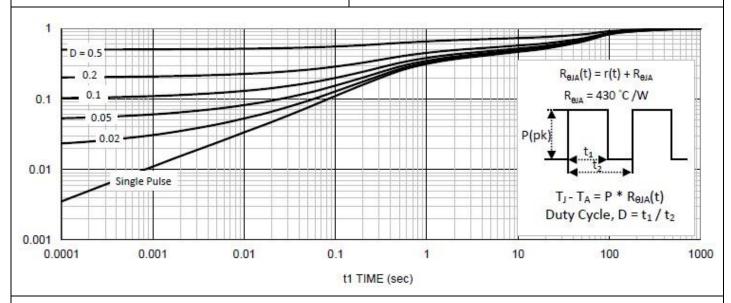


FIG.11-NORMALIZED THERMAL TRANSIENT JUNCTION TO AMBIENT



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