MRFIC1505/MRFIC1505A Integrated GPS Downconverter

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1.575 GHz GPS DOWNCONVERTER

This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Motorola's low-cost, high-performance MOSAIC 5. silicon bipolar process and is packaged in a low-cost surface mount LQFP-48 package. In addition to the mixers, a VCO, PLL, Crystal Oscillator, A/D converter and a loop filter are integrated on-chip. Output IF is nominally 4.1 MHz.

- 105 dB Typical Conversion Gain
- 2.7 V Operation
- 28 mA Typical Current Consumption
- Low–Cost, Low–Profile Plastic LQFP Package

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Ordering Information

Device	Operating Temperature Range	Package
MRFIC1505R2	$T_{A} = -40$ to $85^{\circ}C$	LQFP-48
MRFIC1505AR2	$T_{A} = -40$ to $85^{\circ}C$	LQFP-48



Plastic Package Case 932 (LQFP-48)



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Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	5.0	Vdc
DC Supply Current	I _{DD}	60	mA
Operating Ambient Temperature	T _A	-40 to 85	°C
Storage Temperature Range	T _{stg}	-65 to 150	°C
Lead Soldering Temperature Range	-	260	°C

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

Electrical Characteristics (VCC = 2.7 to 3.3 V; TA = -40 to 85°C; Enable = 2.7 V unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit	
Total Device						
Supply Voltage	V _{CC}	2.7	3.0	3.3	V	
Supply Current	1		28	36	m۵	
(TA = 25°C, VCC = 2.7 V, Enable = 2.7V)	'CC	-	20	30	IIIA	
Supply Current	lee	_	2.0	4.0	mA	
$(TA = 25^{\circ}C, VCC = 2.7 V, Enable = 2.7V)$	00		_	_		
RF Amplifier						
RF Input Frequency	f _{in}	-	1575.42	-	MHz	
Input Impedance	Z _{in}	-	50	-	Ω	
Input VSWR	VSWR _{in}	_	2.0	_	-	
Gain	G	13	15	_	dB	
Noise Figure	NF	-	2.0	-	dB	
1.0 dB Compression (Measured at Output)	P _{1dB}	_	1.0	-	dBm	
First Mixer						
Input Frequency	f _{in}	—	1575.42	-	MHz	
Gain	G	10	14		dB	
Noise Figure	NF	-	13	-	dB	
1.0 dB compression (Measured at Output)	P _{1dB}	-	-13	-	dBm	
First Local Oscillator Frequency	f _{LO1}	-	1636.8	_	MHz	
First Intermediate Frequenc	f _{IF1}	_	61.38	_	MHz	
LO Leakage at IF Port	-	_	-40	_	dBm	
LO Leakage at RF Port	-	_	-50	_	dBm	
Output Impedance	Z _{out}	-	50	-	Ω	
First IF Amplifier and Second Mixer			•		•	
Input Frequency	f _{in}	-	61.38	-	MHz	
Input Impedance	Z _{in}	_	230	-	Ω	
Output Impedance	Z _{out}	_	50	-	Ω	
Second Local Oscillator Frequency	f _{LO2}	-	65.47	-	MHz	
Second Intermediate Frequency	f _{IF2}	_	4.092	-	MHz	
LO Leakage at IF Port	-	-	-40	-	dBm	
Gain	G	40	43	-	dB	
Cascaded Noise Figure	NF	_	9.3	-	dB	
1.0 dB Compression Point (Measured at Output)	P _{1dB}	_	-13	-	dBm	
Limiting Amplifier			1			
Second Intermediate Frequency	f _{IF2}	-	4.092	-	MHz	
Input Signal Level	-	4.0	11	31	Μv	
Output Voltage Swing (into 10 pf II100 k Ω	V _{out}	800	-	_	mVpp	
DC Output Level	-	_	1.4	_	V	
Gain	G	-	50	_	dB	
Reference Oscillator	L		1			
Reference Frequency	f _r	-	16.368	-	MHz	
Reference Frequency Input Level (Crystal Output Pin)	-	-	500	-	mVpp	

Characteristic	Symbol	Min	Тур	Max	Unit
Reference Oscillator Output Voltage Level (Into 15 pf II 10 k Ω)	-	750	-	-	mVpp
Reference Clock Input Drive Level	-	400	800	1500	mVpp
PLL	•	•			
First Local Oscillator Frequency	f _{LO1}	-	1636.8	-	MHz
Second Local Oscillator Frequency	f _{LO2}	-	65.47	-	MHz
VCO C/N (at 10 kHz Offset)	-	-	-80	-	dBc/Hz
VCO Gain (TBD Varactor)	-	-	200	-	MHz/V
Enable	•	•		•	
Enable Active Level	-	0.8 x V _{CC}	V _{CC}	-	V
Disable Active Level	-	-	0	0.2 x V _{CC}	V
Voltage Regulator		•			
Regulator Output Voltage	V-	2.1	2.3	2.5	V
(V _{CC} = 2.7 to 3.3 V, I _{out} = 3.0 mA)	vo				
MRFIC505 Temperature Sense Specs					
Temperature Sensor Output Voltage @ 25°C	-	1.2	1.28	1.375	V
Temperature Sensor Slope over Temperature	-	_	5.0	-	mV/°C
MRFIC505A Temperature Sense Specs					
Temperature Sensor Output Voltage @ 25°C	-	1.270	1.395	1.463	V
Temperature Sensor Slope over Temperature	-	_	5.0	-	mV/°C

Electrical Characteristics (VCC = 2.7 to 3.3 V; TA = -40 to 85°C; Enable = 2.7 V unless otherwise noted)



NOTES: 1. R8 must be set to match your 2nd IF filter impedance.

2. Layout of capacitors C10, C11, C12 is critical for stability of Limiter.

Figure 1 Applications Schematic (1636.8 MHz LO)

Outline Dimensions

PLASTIC PACKAGE CASE 932-03 (LQFP-48) ISSUE F



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