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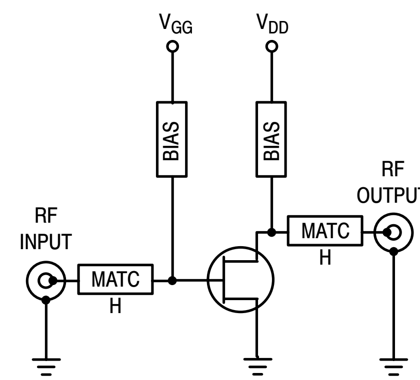
RF Reference Design Library

Gallium Arsenide PHEMT

RF Power Field Effect Transistors

MRFG35003NT1
MRFG35003MT1
BWA

BWA
2.4-2.5 GHz



Device Characteristics (From Device Data Sheet)

Designed for WLL/MMDS/BWA or UMTS driver applications with frequencies from 1.8 to 3.6 GHz. Devices are unmatched and are suitable for use in Class AB linear base station applications.

- Typical W-CDMA Performance: -42 dBc ACPR, 3.55 GHz, 12 Volts, I_{DQ} = 55 mA, 5 MHz Offset/3.84 MHz BW, 64 DPCH (8.5 dB P/A @ 0.01% Probability)
  Output Power — 300 mWatt
  Power Gain — 11.5 dB
  Efficiency — 25%
- 3 Watts P1dB @ 3.55 GHz
- Excellent Phase Linearity and Group Delay Characteristics
- High Gain, High Efficiency and High Linearity
- N Suffix Indicates Lead-Free Terminations

Reference Design Characteristics

- Typical Single-Channel W-CDMA Performance: -45 dBc ACPR, 2.45 GHz, 12 Volts, I_{DQ} = 55 mA, 5 MHz Offset/3.84 MHz BW, 64 DPCH (8.5 dB P/A @ 0.01% Probability)
  Output Power — 350 mWatt
  Power Gain — 12.5 dB
  Efficiency — 26%

MRFG35003NT1(MT1) BWA 2.4-2.5 GHz REFERENCE DESIGN

Designed by: Monte Miller and Rick Hooper

This reference design is designed to demonstrate the typical RF performance characteristics of the MRFG35003NT1(MT1) when applied for the 2.4-2.5 GHz W-CDMA frequency band. The reference design is tuned for the best tradeoff between good W-CDMA linearity and good power capability and efficiency.

REFERENCE DESIGN LIBRARY TERMS AND CONDITIONS

Freescale is pleased to make this reference design available for your use in development and testing of your own product or products, without charge. The reference design contains easy-to-copy, fully functional amplifier designs. Where possible, it consists of “no tune” distributed element matching circuits designed to be as small as possible, includes temperature compensated bias circuitry, and is designed to be used as “building blocks” for our customers.

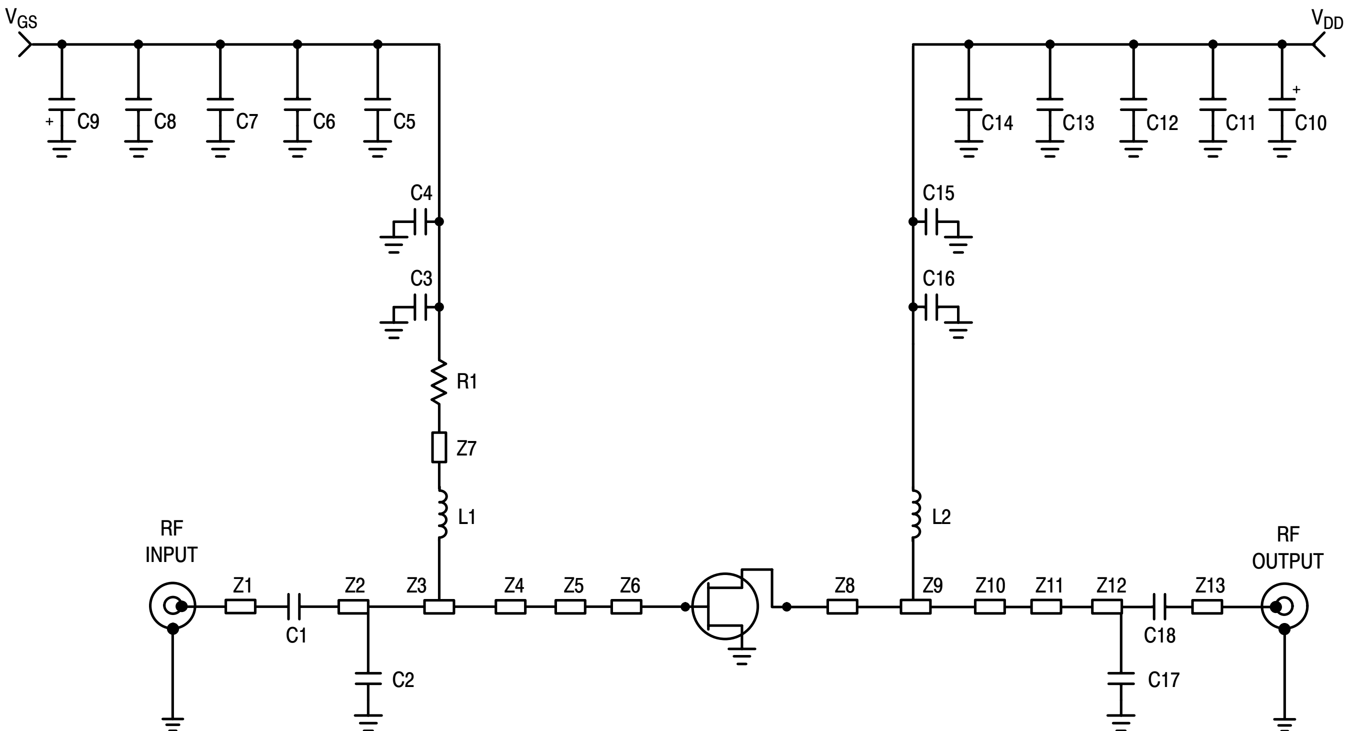
HEATSINKING

When operating this fixture please provide adequate heatsinking for the device. Excessive heating of the device will prevent repeating of the included measurements.

NONLINEAR SIMULATION

To aid the design process and help reduce time to market for our customers, Freescale provides device models for several commercially available harmonic balance simulators. Our model Library is available for all major computer platforms supported by these simulators. For details on the RF model library and supported harmonic balance simulators, go to the following url:

http://www.freescale.com/rf/models

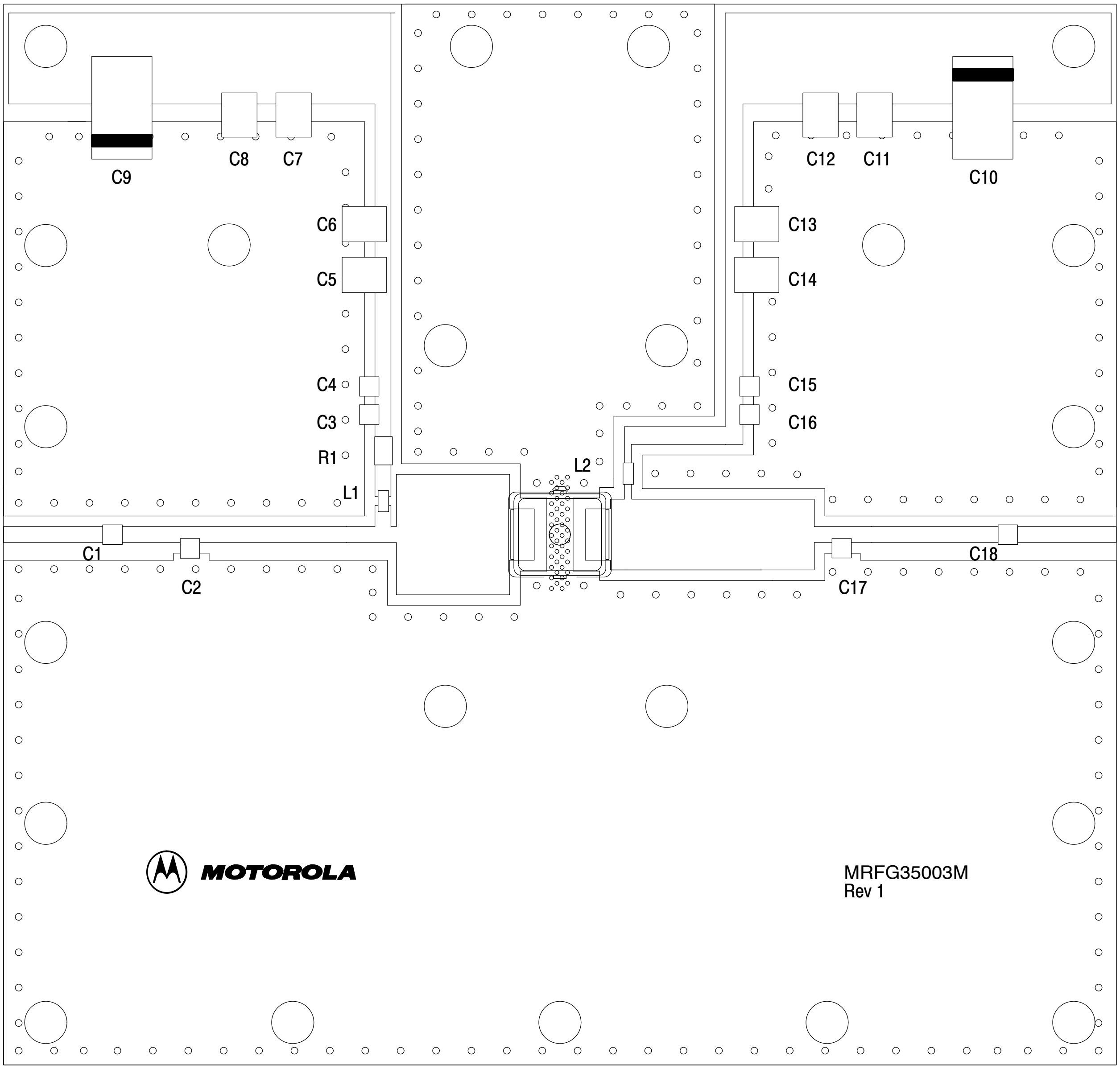


Z1, Z13	0.044″ x 0.295″ Microstrip	Z7	0.045″ x 0.100″ Microstrip
Z2	0.044″ x 0.730″ Microstrip	Z9	0.200″ x 0.040″ Microstrip
Z3	0.105″ x 0.045″ Microstrip	Z10	0.260″ x 0.020″ Microstrip
Z4	0.044″ x 0.015″ Microstrip	Z11	0.200″ x 0.516″ Microstrip
Z5	0.340″ x 0.320″ Microstrip	Z12	0.044″ x 0.534″ Microstrip
Z6, Z8	0.146″ x 0.070″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.50

Figure 1. MRFG35003NT1(MT1) BWA Reference Design Schematic

Table 1. MRFG35003NT1(MT1) BWA Reference Design Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	3.9 pF Chip Capacitor	08051J3R9BBT	AVX
C2	0.9 pF Chip Capacitor	08051J0R9BBT	AVX
C3, C16	10 pF Chip Capacitors	100A100JP150X	ATC
C4, C15	100 pF Chip Capacitors	100A101JP150X	ATC
C5, C14	100 pF Chip Capacitors	100B101JP500X	ATC
C6, C13	1000 pF Chip Capacitors	100B102JP500X	ATC
C7, C12	0.1 μF Chip Capacitors	CDR33BX104AKWS	Kemet
C8, C11	39K pF Chip Capacitors	200B393KP500X	ATC
C9, C10	22 μF Tantalum Capacitors	T491X226K035AS	Newark
C17	1.0 pF Chip Capacitor	08051J1R0BBT	AVX
C18	15.0 pF Chip Capacitor	08051J15R0GBT	AVX
L1	4.7 nH Chip Inductor	LL2102-F4N7K	TOKO
L2	8.2 nH Chip Inductor	LL1608-FHN2K	TOKO
R1	75 Ω, 1/4 W 1% Chip Resistor	D55342M07B75JOR	Newark



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRFG35003NT1(MT1) BWA Reference Design Component Layout

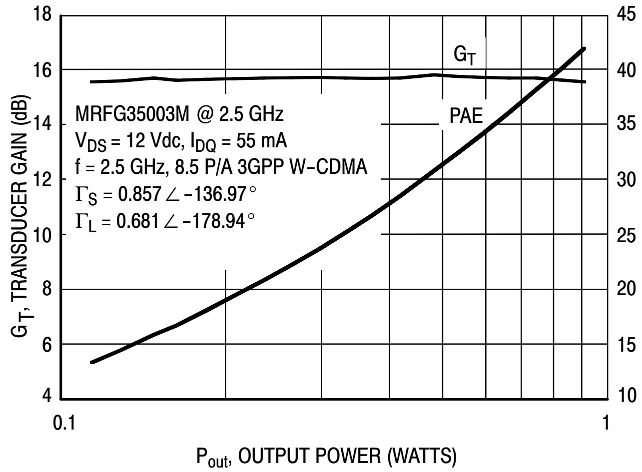


Figure 3. Transducer Gain and Power Added Efficiency versus Output Power

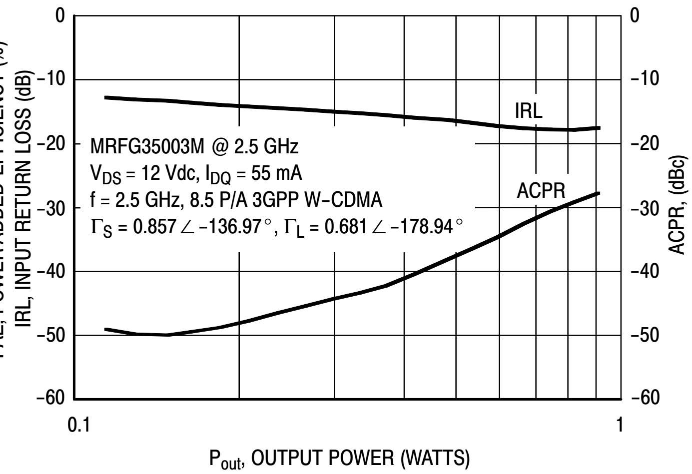


Figure 4. W-CDMA ACPR and Input Return Loss versus Output Power

NOTE: Data in Figures 3 and 4 is generated from load pull, not from the test circuit shown.

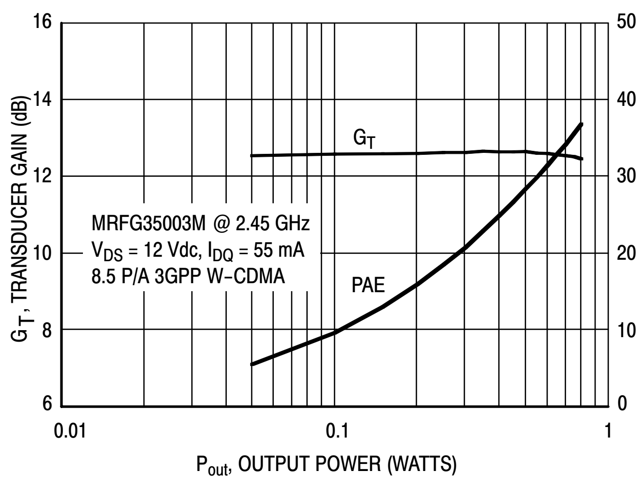


Figure 5. Transducer Gain and Power Added Efficiency versus Output Power

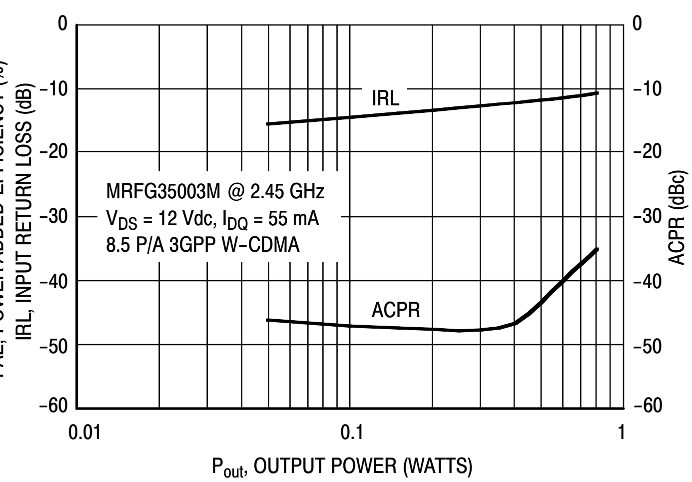


Figure 6. W-CDMA ACPR and Input Return Loss versus Output Power

NOTE: Data in Figures 5 and 6 is generated from the test circuit shown.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

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