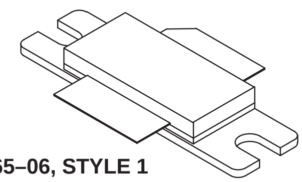
The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF9085
MRF9085R3
MRF9085S
MRF9085SR3
MRF9085LS
MRF9085LSR3

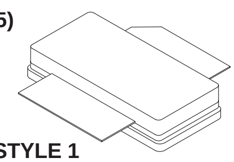
880 MHz, 90 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 26 volt base station equipment.

- Typical CDMA Performance @ 880 MHz, 26 Volts, I_{DQ} = 700 mA
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  - Output Power — 20 Watts
  - Power Gain — 17.9 dB
  - Efficiency — 28%
  - Adjacent Channel Power —
    - 750 kHz: –45.0 dBc @ 30 kHz BW
    - 1.98 MHz: –60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.



CASE 465–06, STYLE 1
(NI–780)
(MRF9085)



CASE 465A–06, STYLE 1
(NI–780S)
(MRF9085S, MRF9085LS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions		Class
Human Body Model		1 (Minimum)
Machine Model	MRF9085 MRF9085S/MRF9085LSR3	M2 (Minimum) M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

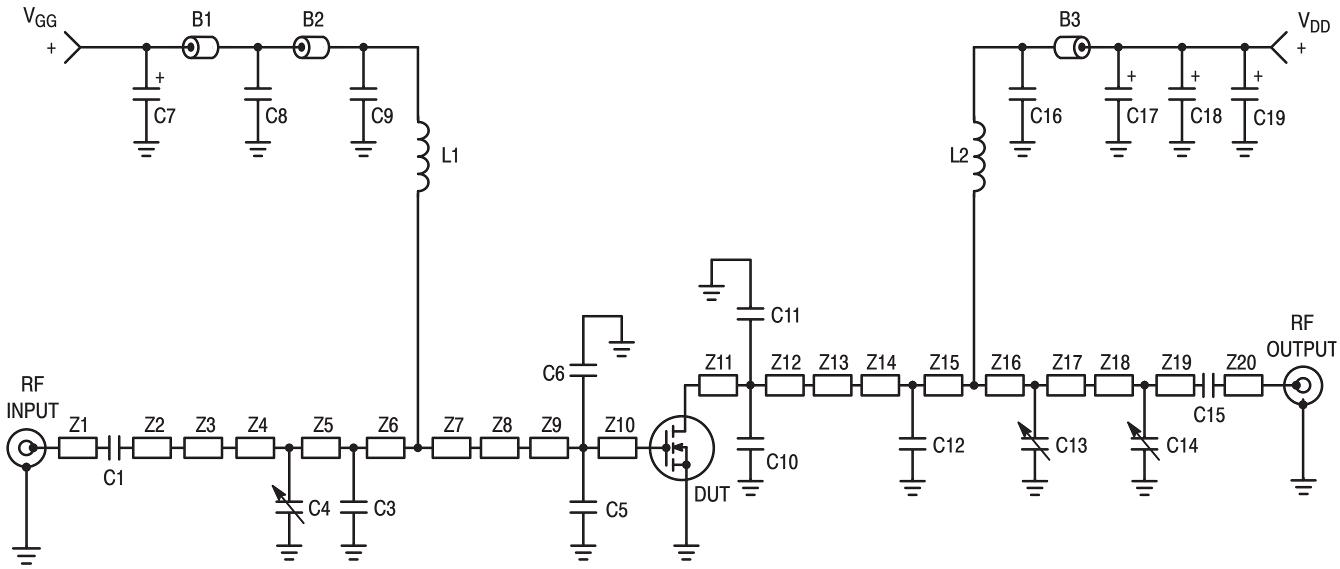
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vds, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 700 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6 Adc)	g_{fs}	—	8.0	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	73	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.9	—	pF

(1) Part is internally input matched.

(continued)

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	G_{ps}	17	17.9	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	η	36	40	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 880.0 MHz, f2 = 880.1 MHz)	IRL	—	–21	–9	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	G_{ps}	—	17.9	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	η	—	40.0	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 700 mA, f1 = 865.0 MHz, f2 = 865.1 MHz)	IRL	—	–16	—	dB
Power Output, 1 dB Compression Point (V_{DD} = 26 Vdc, CW, I_{DQ} = 700 mA, f1 = 880.0 MHz)	P_{1dB}	—	105	—	W
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 700 mA, f1 = 880.0 MHz)	G_{ps}	—	17.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 700 mA, f1 = 880.0 MHz)	η	—	51	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 700 mA, f = 880.0 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			



B1, B2, B3	Short Ferrite Beads, Surface Mount	Z6	0.076″ x 0.220″ Microstrip
C1, C9, C15, C16	47 pF Chip Capacitors, B Case , ATC	Z7	0.261″ x 0.220″ Microstrip
C3	5.6 pF Chip Capacitor, B Case, ATC	Z8	0.220″ x 0.630″ x 0.200″ Taper
C4, C13	0.8 – 8.0 Variable Capacitors, Gigatrim	Z9	0.240″ x 0.630″ Microstrip
C5, C6, C12	10 pF Chip Capacitors, B Case, ATC	Z10	0.060″ x 0.630″ Microstrip
C7, C17, C18, C19	10 μF, 35 V Tantalum Surface Mount Capacitors, Kemet	Z11	0.067″ x 0.630″ Microstrip
C8	20 K pF Chip Capacitor, B Case, ATC	Z12	0.233″ x 0.630″ Microstrip
C10, C11	16 pF Chip Capacitors, B Case, ATC	Z13	0.630″ x 0.220″ x 0.200″ Taper
C14	0.6 – 4.5 Variable Capacitor, Gigatrim	Z14	0.200″ x 0.220″ Microstrip
L1	7.15 nH Inductor, Coilcraft	Z15	0.055″ x 0.220″ Microstrip
L2	18.5 nH Inductor, Coilcraft	Z16	0.088″ x 0.220″ Microstrip
N1, N2	N–Type Panel Mount, Stripline, M/A–Com	Z17	0.226″ x 0.220″ Microstrip
WB1, WB2	5 Mil BeCu Shim (0.225 x 0.525)	Z18	0.868″ x 0.080″ Microstrip
Z1	0.219″ x 0.080″ Microstrip	Z19	0.129″ x 0.080″ Microstrip
Z2	0.150″ x 0.080″ Microstrip	Z20	0.223″ x 0.080″ Microstrip
Z3	0.851″ x 0.080″ Microstrip	PCB	Etched Circuit Board, Glass, Teflon®
Z4	0.125″ x 0.220″ Microstrip		ε_r = 2.55, 30 Mils
Z5	0.123″ x 0.220″ Microstrip		

Figure 1. 865–895 MHz Broadband Test Circuit Schematic

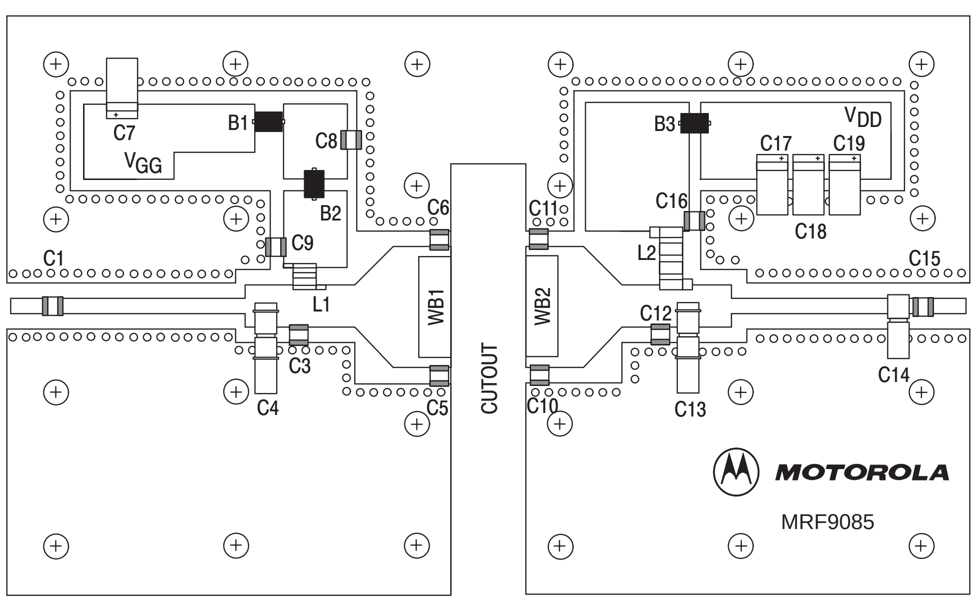


Figure 2. 865–895 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

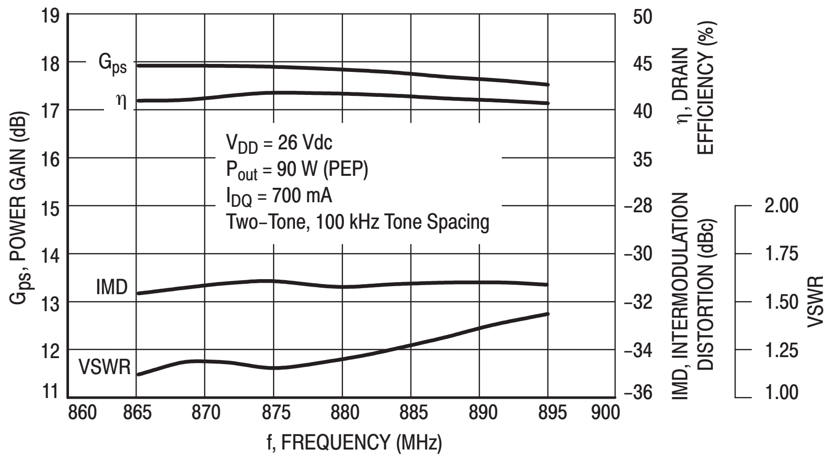


Figure 3. Class AB Broadband Circuit Performance

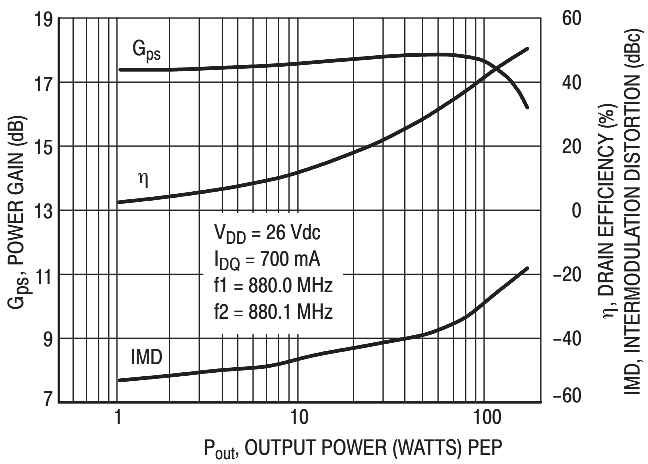


Figure 4. Power Gain, Efficiency, IMD versus Output Power

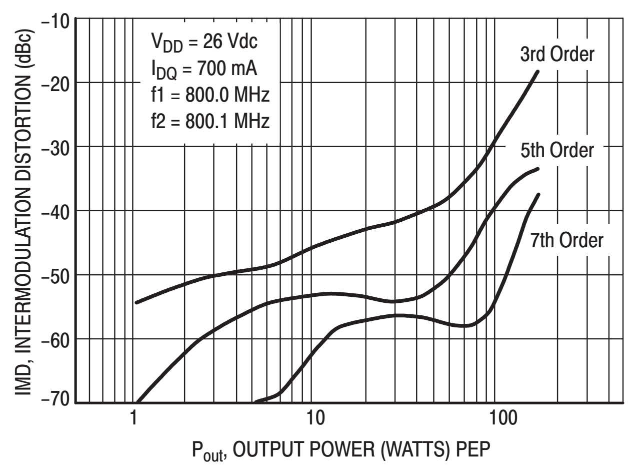


Figure 5. Intermodulation Distortion Products versus Output Power

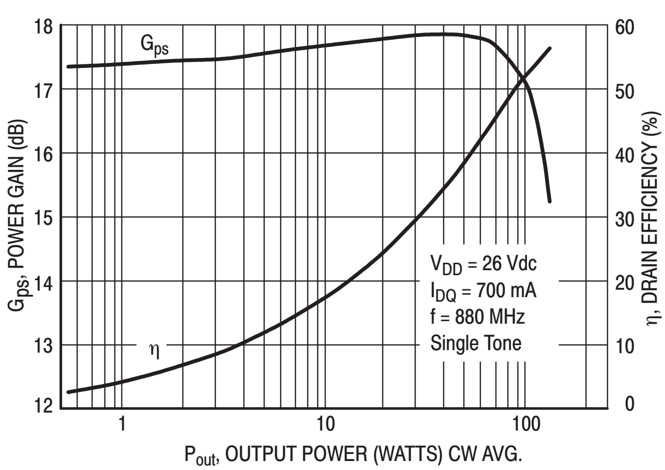


Figure 6. Power Gain, Efficiency versus Output Power

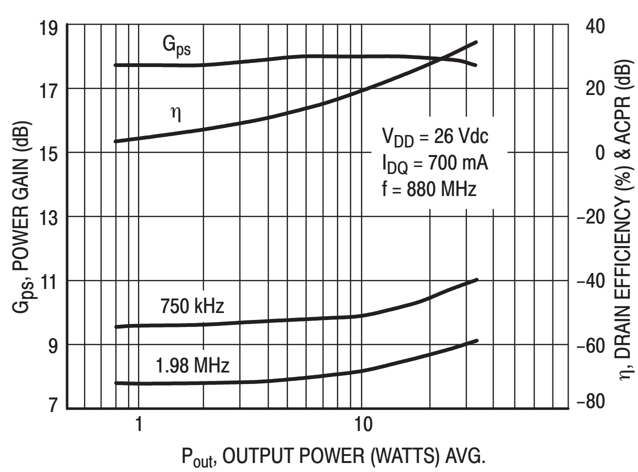
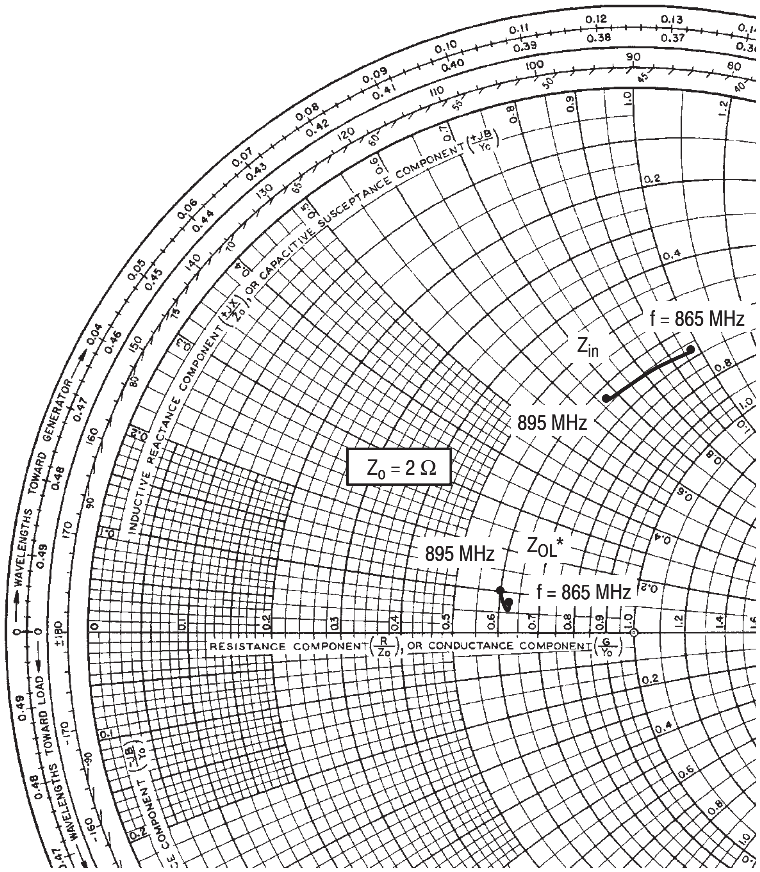


Figure 7. Power Gain, Efficiency, ACPR versus Output Power



V_{DD} = 26 V, I_{DQ} = 700 mA, P_{out} = 90 W PEP

f MHz	Z_{in} Ω	Z_{OL}* Ω
865	1.35 + j1.92	1.26 + j0.15
880	1.33 + j1.66	1.26 + j0.10
895	1.28 + j1.30	1.21 + j0.20

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

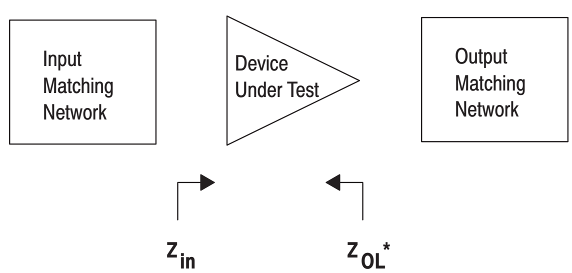


Figure 8. Series Equivalent Input and Output Impedance