

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for base station applications with frequencies from 728 to 768 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 1200$ mA, $P_{out} = 50$ Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
728 MHz	19.7	37.1	6.2	-38.7
748 MHz	19.5	37.0	6.1	-37.5
768 MHz	19.4	37.9	6.1	-37.8

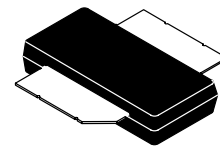
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 748 MHz, 170 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Typical P_{out} @ 1 dB Compression Point $\approx$ 182 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

MRF8S7170NR3

**728-768 MHz, 50 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFET**



**CASE 2021-03, STYLE 1
OM-780-2
PLASTIC**

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 170 W CW, 28 Vdc, $I_{DQ} = 1200$ mA Case Temperature 81°C, 50 W CW, 28 Vdc, $I_{DQ} = 1200$ mA	$R_{\theta JC}$	0.30 0.37	°C/W

- Continuous use at maximum temperature will affect MTTF.
- MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
- Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 70\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 355\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1.5	2.3	3	Vdc
Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 1200\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	2.3	3.1	3.8	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.9\text{ Adc}$)	$V_{DS(on)}$	0.1	0.22	0.3	Vdc

Functional Tests ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1200\text{ mA}$, $P_{out} = 50\text{ W Avg.}$, $f = 748\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

Power Gain	G_{ps}	18.0	19.5	21.0	dB
Drain Efficiency	η_D	34.0	37.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.5	-35.0	dBc
Input Return Loss	IRL	—	-24	-9	dB

Typical Broadband Performance (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1200\text{ mA}$, $P_{out} = 50\text{ W Avg.}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
728 MHz	19.7	37.1	6.2	-38.7	-13
748 MHz	19.5	37.0	6.1	-37.5	-24
768 MHz	19.4	37.9	6.1	-37.8	-16

1. Part internally matched both on input and output.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1200\text{ mA}$, 728-768 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	182	—	W
IMD Symmetry @ 160 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands $> 2\text{ dB}$)	IMD _{sym}	—	16	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	65	—	MHz
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 50\text{ W Avg.}$	G _F	—	0.5	—	dB
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.017	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	$\Delta P1\text{dB}$	—	0.0048	—	dBm/ $^\circ\text{C}$

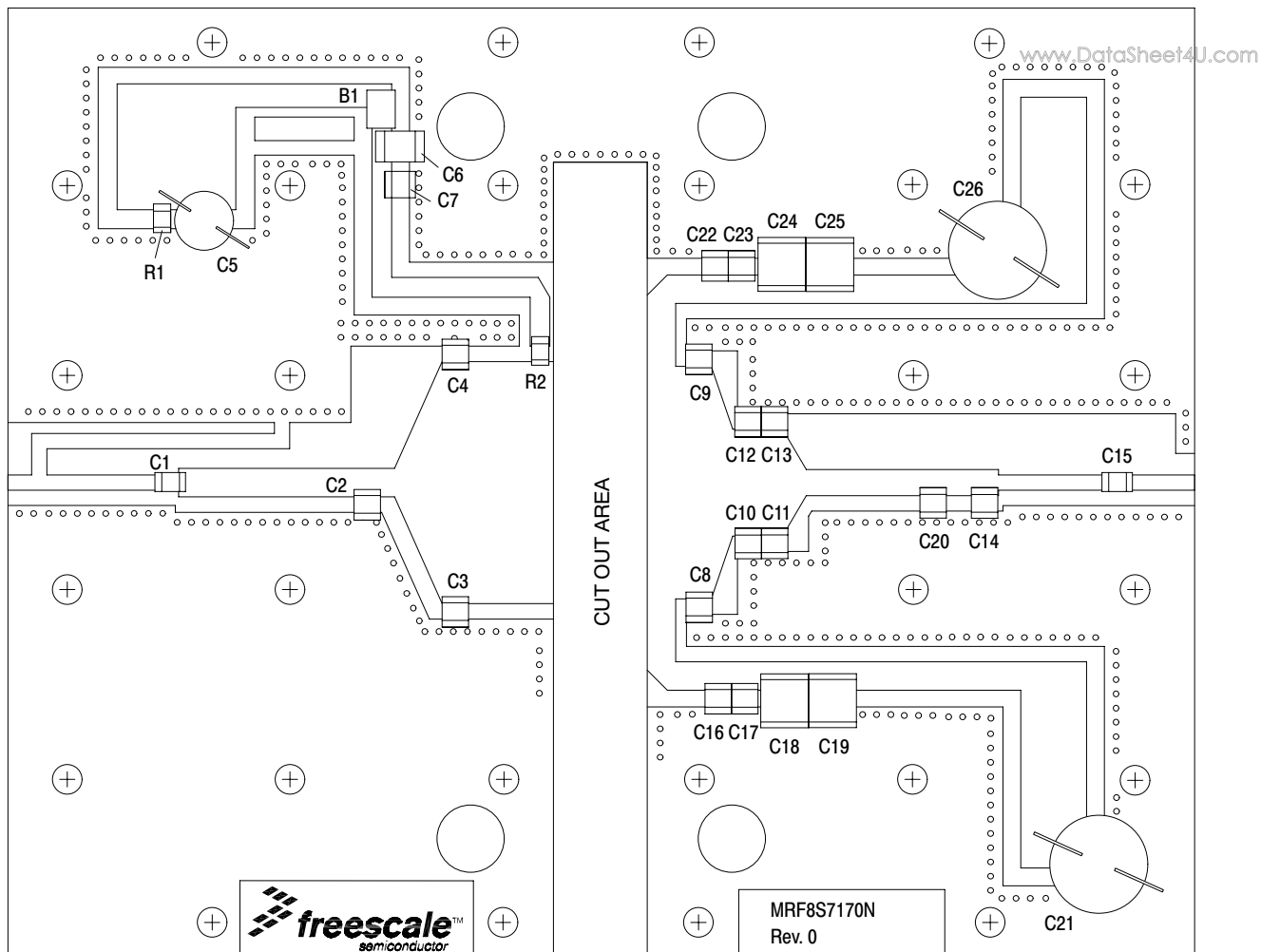


Figure 1. MRF8S7170NR3 Test Circuit Component Layout

Table 6. MRF8S7170NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead, Short	2743019447	Fair-Rite
C1	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C2	2.2 pF Chip Capacitor	ATC100B2R2JT500XT	ATC
C3, C4	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C5	47 μ F, 63 V Electrolytic Capacitor	476KXM063M	Illinois Capacitor
C6	6.8 μ F, 100 V Chip Capacitor	C4532X7R1H685KT	TDK
C7	100 pF Chip Capacitor	ATC100B101JT500XT	ATC
C8, C9	11 pF Chip Capacitors	ATC100B110JT500XT	ATC
C10, C12	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C11, C13	7.5 pF Chip Capacitors	ATC100B7R5CT500XT	ATC
C14	5.1 pF Chip Capacitor	ATC100B5R1CT500XT	ATC
C15, C16, C17, C22, C23	39 pF Chip Capacitors	ATC100B390JT500XT	ATC
C18, C19, C24, C25	10 μ F, 25 V Chip Capacitors	C5750X7R1E106KT	TDK
C20	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C21, C26	470 μ F, 63 V Electrolytic Capacitors	477KXM063M	Illinois Capacitor
R1	2K Ω , 1/4 W Chip Resistor	CRCW12062K00FKEA	Vishay
R2	4.3 Ω , 1/4 W Chip Resistor	CRCW12064R30FKEA	Vishay
PCB	0.030", $\epsilon_r = 3.5$	RF-35	Taconic

TYPICAL CHARACTERISTICS

www.DataSheet4U.com

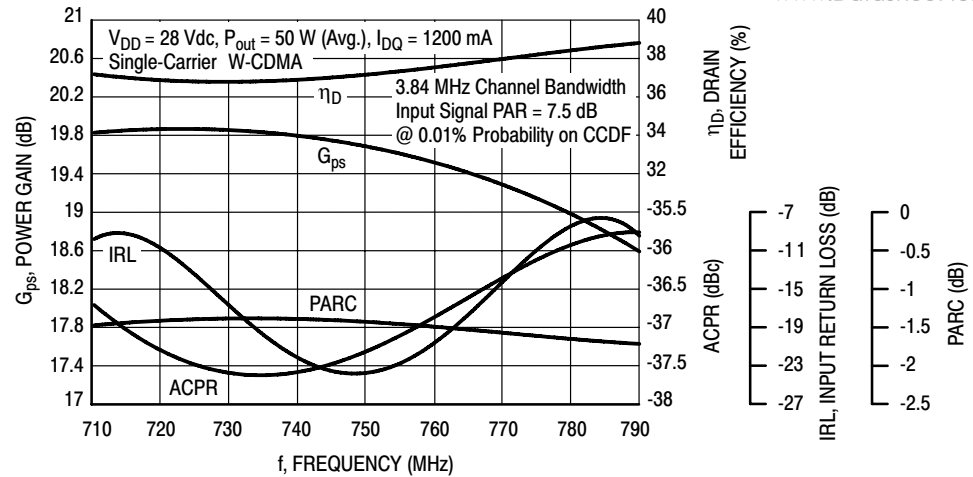


Figure 2. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 50$ Watts Avg.

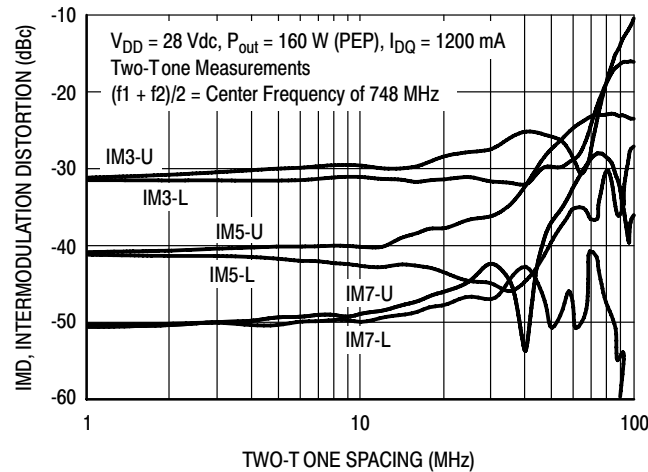


Figure 3. Intermodulation Distortion Products versus Two-Tone Spacing

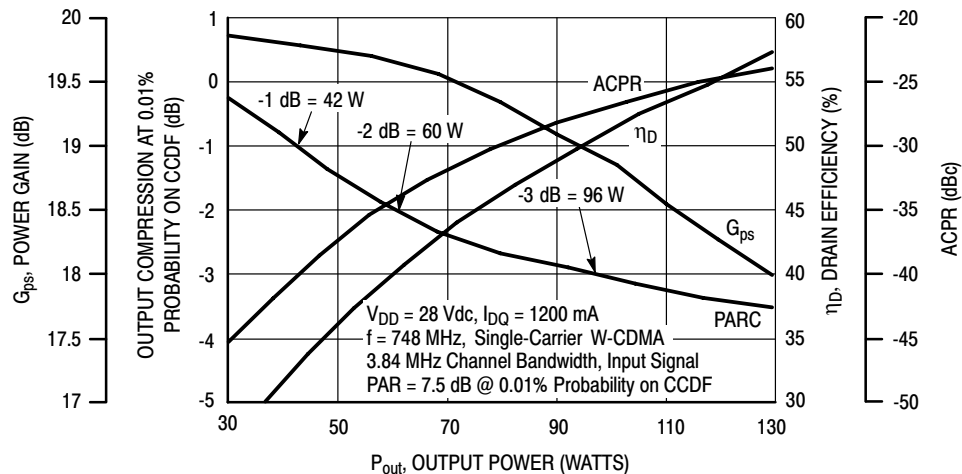


Figure 4. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

www.DataSheet

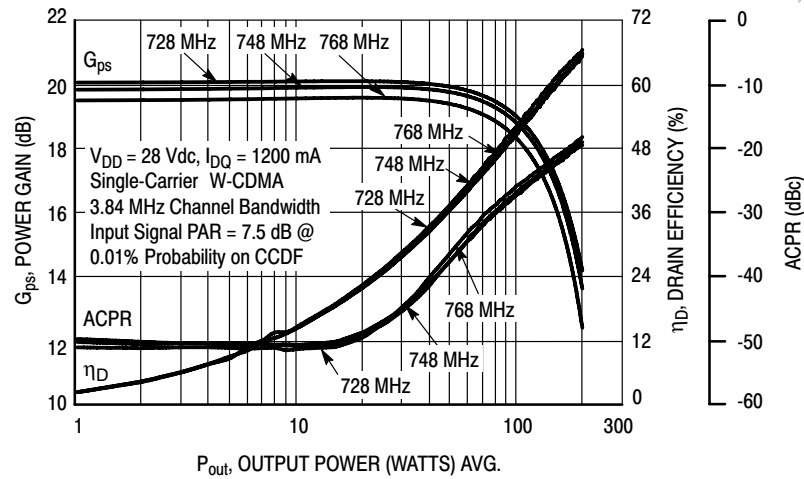


Figure 5. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

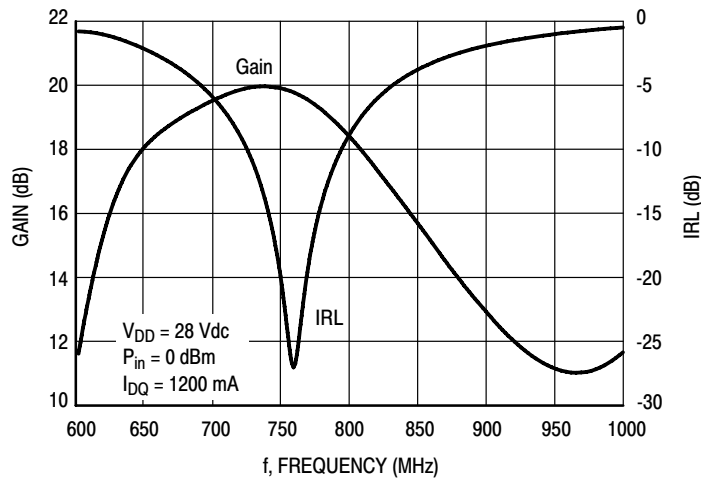


Figure 6. Broadband Frequency Response

W-CDMA TEST SIGNAL

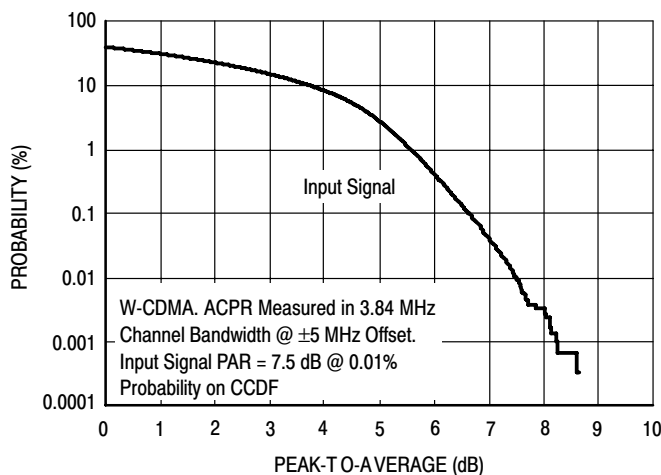


Figure 7. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

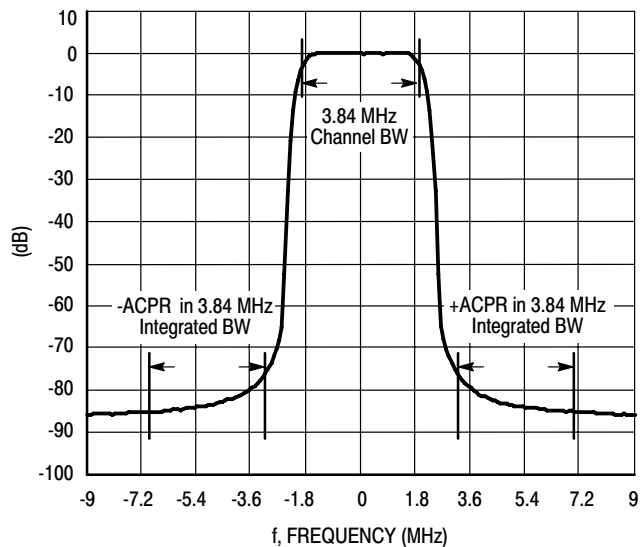


Figure 8. Single-Carrier W-CDMA Spectrum

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1200 \text{ mA}$, $P_{out} = 50 \text{ W Avg.}$

www.DataSheet4U.com

f MHz	Z_{source} Ω	Z_{load} Ω
710	$0.876 - j2.237$	$1.685 - j0.887$
720	$0.910 - j2.150$	$1.659 - j0.776$
730	$0.942 - j2.080$	$1.650 - j0.683$
740	$0.970 - j2.032$	$1.660 - j0.610$
750	$0.981 - j2.013$	$1.677 - j0.563$
760	$0.961 - j2.009$	$1.688 - j0.550$
770	$0.911 - j1.996$	$1.687 - j0.551$
780	$0.843 - j1.955$	$1.660 - j0.557$
790	$0.787 - j1.881$	$1.620 + j0.548$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

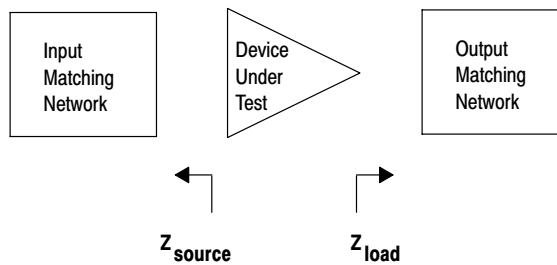
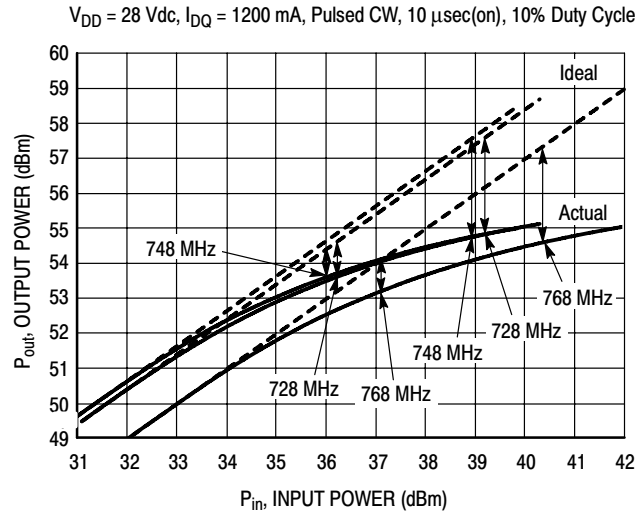


Figure 9. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

www.DataSheet4U.com



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
728	229	53.6	310	54.9
748	227	53.5	303	54.8
768	214	53.3	293	54.6

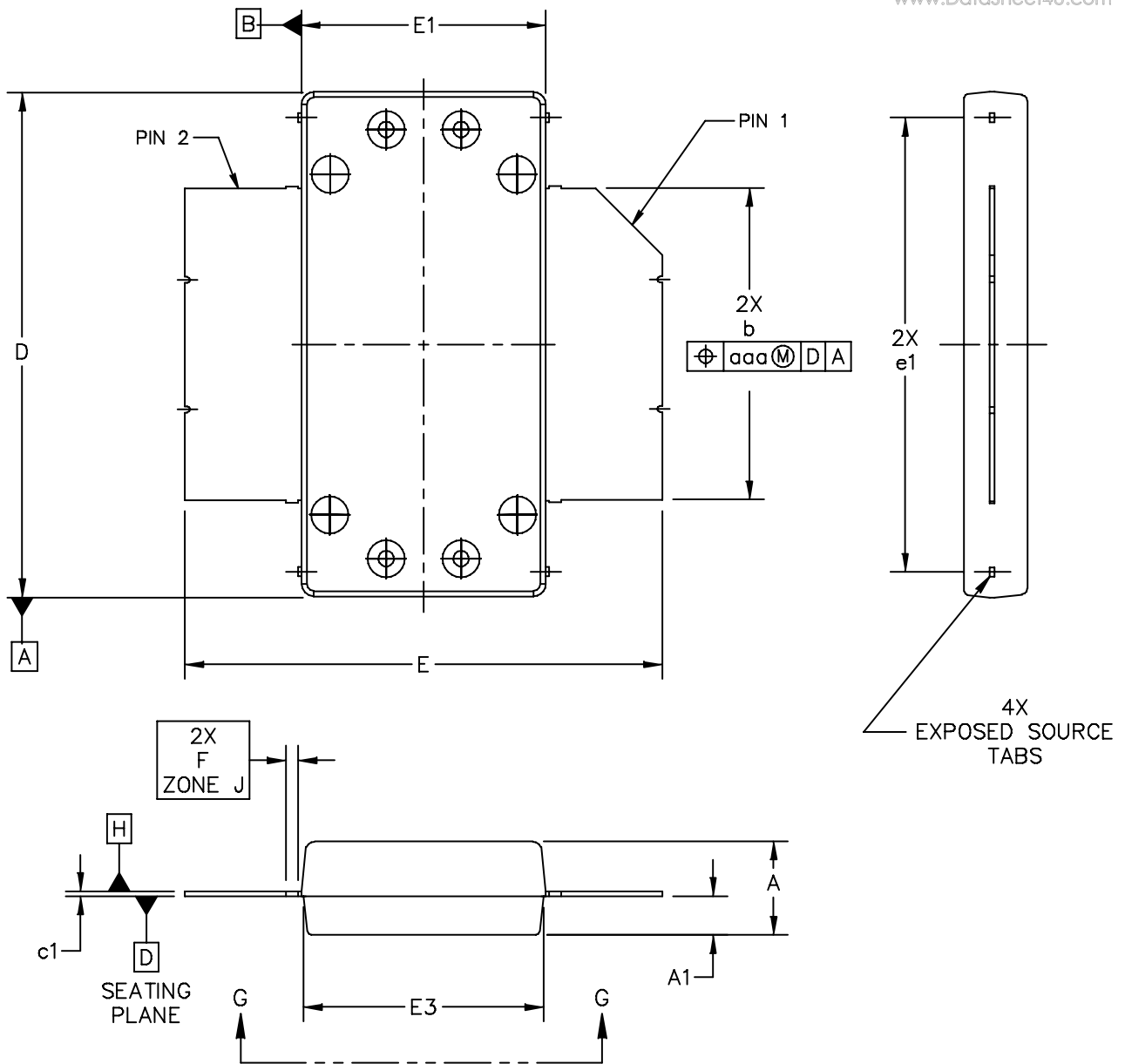
Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
728	P1dB	$0.61 - j2.32$	$0.72 - j1.32$
748	P1dB	$0.73 - j2.60$	$0.81 - j1.27$
768	P1dB	$0.72 - j2.82$	$0.58 - j1.46$

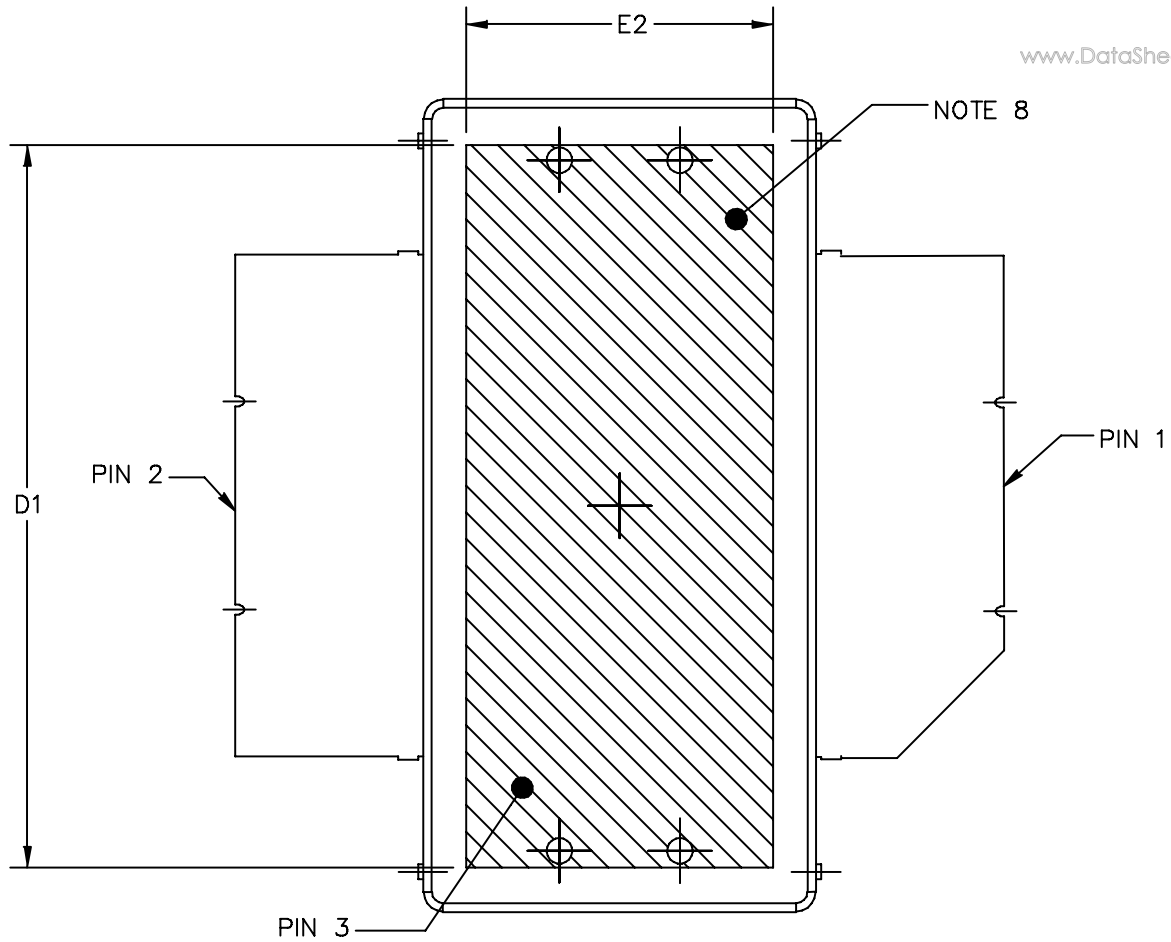
Figure 10. Pulsed CW Output Power
versus Input Power @ 28 V

PACKAGE DIMENSIONS

www.DataSheet4U.com



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM780-2 STRAIGHT LEAD		DOCUMENT NO: 98ASA10831D	REV: B
		CASE NUMBER: 2021-03	22 OCT 2009
		STANDARD: NON-JEDEC	



BOTTOM VIEW
VIEW G-G

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: OM780-2 STRAIGHT LEAD	DOCUMENT NO: 98ASA10831D		REV: B
	CASE NUMBER: 2021-03		22 OCT 2009
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH

www.DataSheet4U.com

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:

PIN 1 - DRAIN
 PIN 2 - GATE
 PIN 3 - SOURCE

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----	aaa	.004		0.10	
E	.762	.770	19.36	19.56					
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.				MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE		
TITLE: OM780-2 STRAIGHT LEAD					DOCUMENT NO: 98ASA10831D				REV: B
					CASE NUMBER: 2021-03				22 OCT 2009
					STANDARD: NON-JEDEC				

MRF8S7170NR3

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

www.DataSheet4U.com

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2010	• Initial Release of Data Sheet

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

http://www.freescale.com/support

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2010. All rights reserved.

