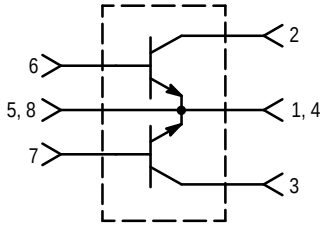
The RF Line
NPN Silicon Push-Pull RF Power Transistor

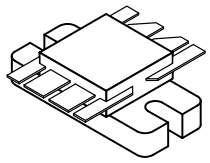
MRF392

125 W, 30 to 500 MHz
CONTROLLED "Q"
BROADBAND PUSH–PULL
RF POWER TRANSISTOR
NPN SILICON

Designed primarily for wideband large–signal output and driver amplifier stages in the 30 to 500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 125 W
  Typical Gain = 10 dB
  Efficiency = 55% (Typ)
- Built–In Input Impedance Matching Networks for Broadband Operation
- Push–Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.





CASE 744A–01, STYLE 1

The MRF392 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push–pull configuration.

PUSH–PULL TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

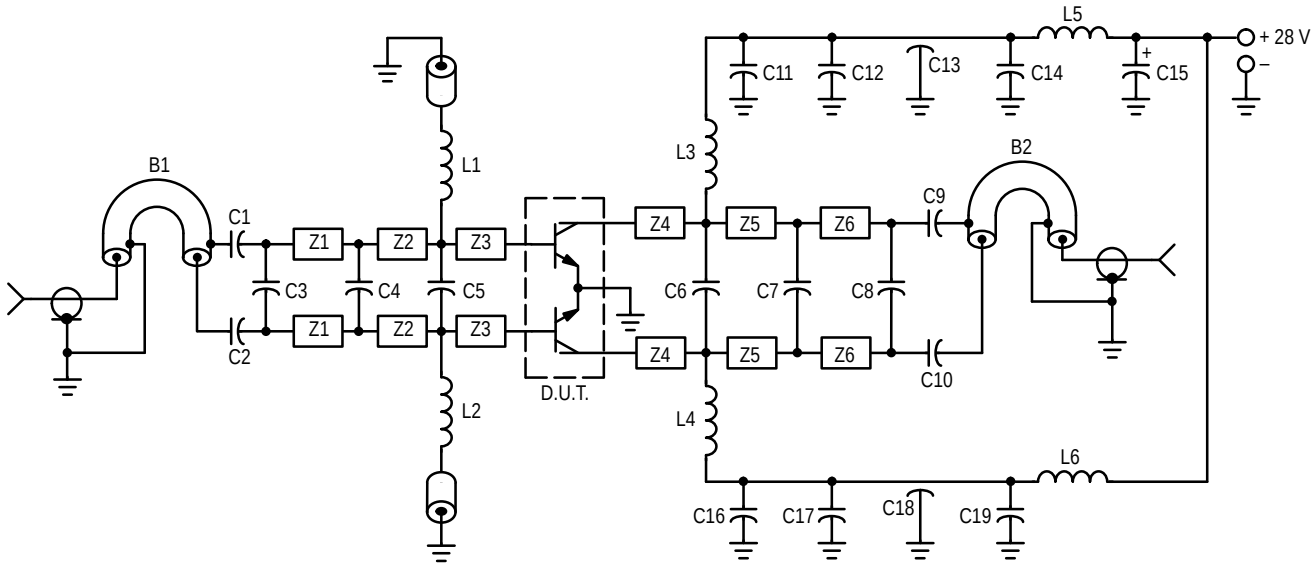
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF push–pull amplifier.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	60	100	—
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	75	95	pF
FUNCTIONAL TESTS (2) **— See Figure 1**					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	G_{pe}	8.0	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz, VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push–pull amplifier.



C1, C2 — 240 pF, 100 Mil Chip Cap (ATC) or Equivalent
C3 — 3.6 pF, 100 Mil Chip Cap (ATC) or Equivalent
C4, C8 — 8.2 pF, 100 Mil Chip Cap (ATC) or Equivalent
C5, C6 — 20 pF, 100 Mil Chip Cap (ATC) or Equivalent
C7 — 18 pF, Mini Unelco or Equivalent
C9, C10 — 270 pF, 100 Mil Chip Cap (ATC) or Equivalent
C11, C12, C16, C17 — 470 pF 100 Mil Chip Cap (ATC) or Equivalent
C13, C18 — 680 pF Feedthru
C14, C19 — 0.1 μF Erie Redcap or Equivalent
C15 — 20 μF, 50 V

L1, L2 — 0.15 μH Molded Choke With Ferrite Bead
L3, L4 — 2–1/2 Turns #20 AWG, 0.200 ID
L5, L6 — 3–1/2 Turns #18 AWG, 0.200 ID

B1 — Balun, 50 Ω Semi–Rigid Coaxial Cable 86 Mil OD, 2″ L
B2 — Balun, 50 Ω Semi–Rigid Coaxial Cable 86 Mil OD, 2″ L

Z1 — Microstrip Line 270 Mil L x 125 Mil W
Z2 — Microstrip Line 375 Mil L x 125 Mil W
Z3 — Microstrip Line 280 Mil L x 125 Mil W
Z4 — Microstrip Line 300 Mil L x 125 Mil W
Z5 — Microstrip Line 350 Mil L x 125 Mil W
Z6 — Microstrip Line 365 Mil L x 125 Mil W

Board Material — 0.0625″ Teflon Fiberglass ε_r = 2.5 ± 0.05 1 oz. Cu. CLAD, Double Sided

Figure 1. 400 MHz Test Fixture

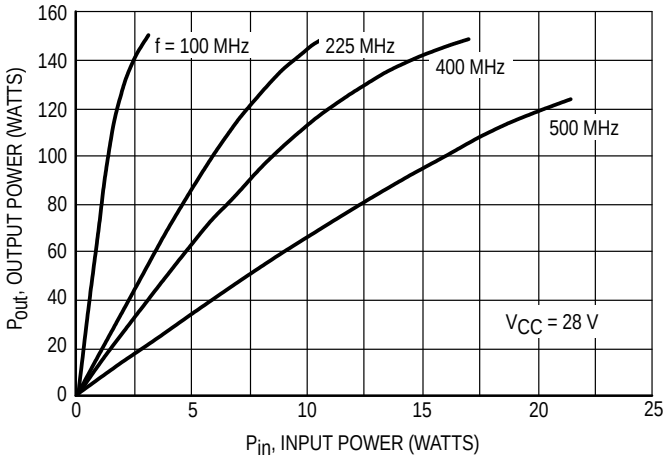


Figure 2. Output Power versus Input Power

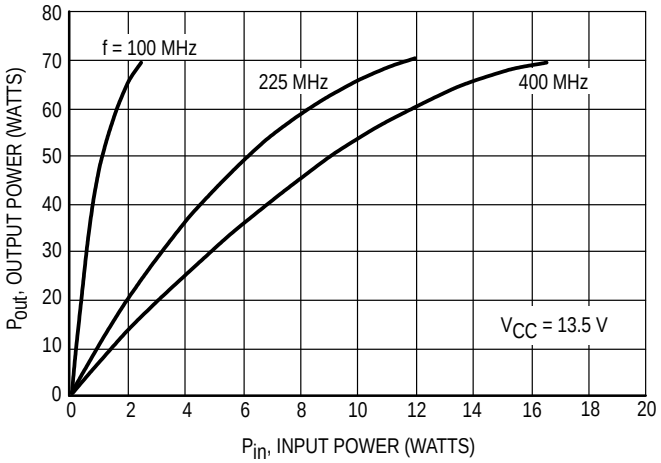


Figure 3. Output Power versus Input Power

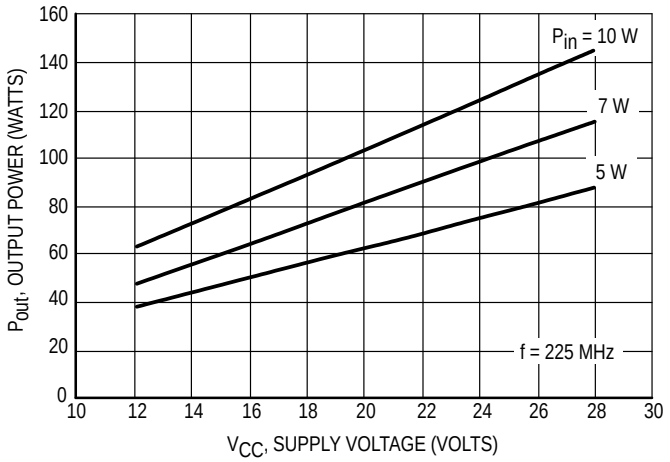


Figure 4. Output Power versus Supply Voltage

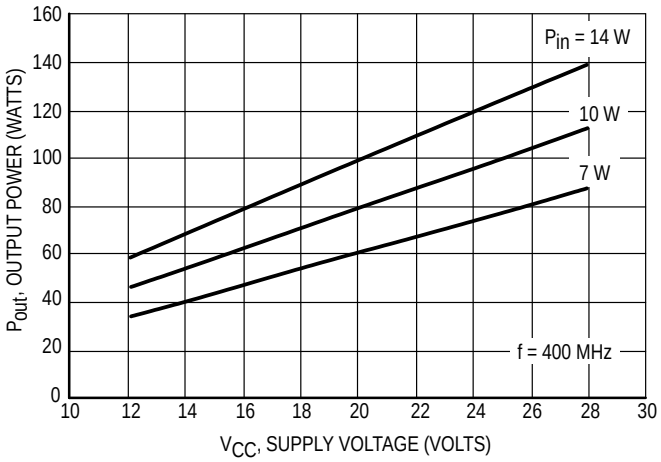
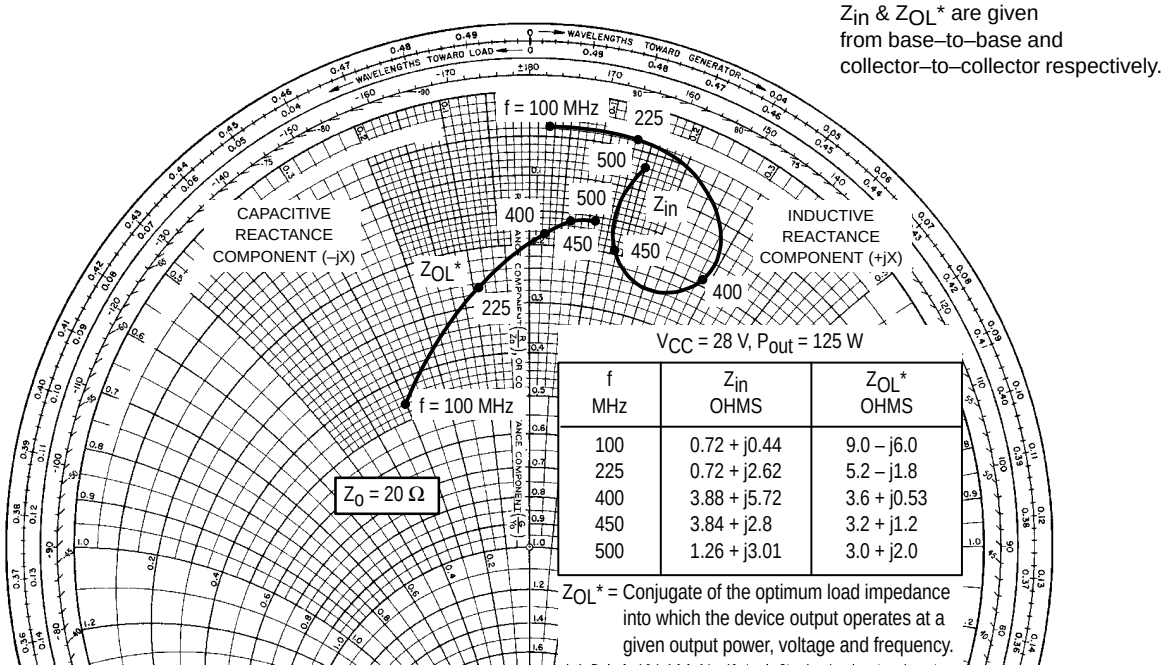


Figure 5. Output Power versus Supply Voltage

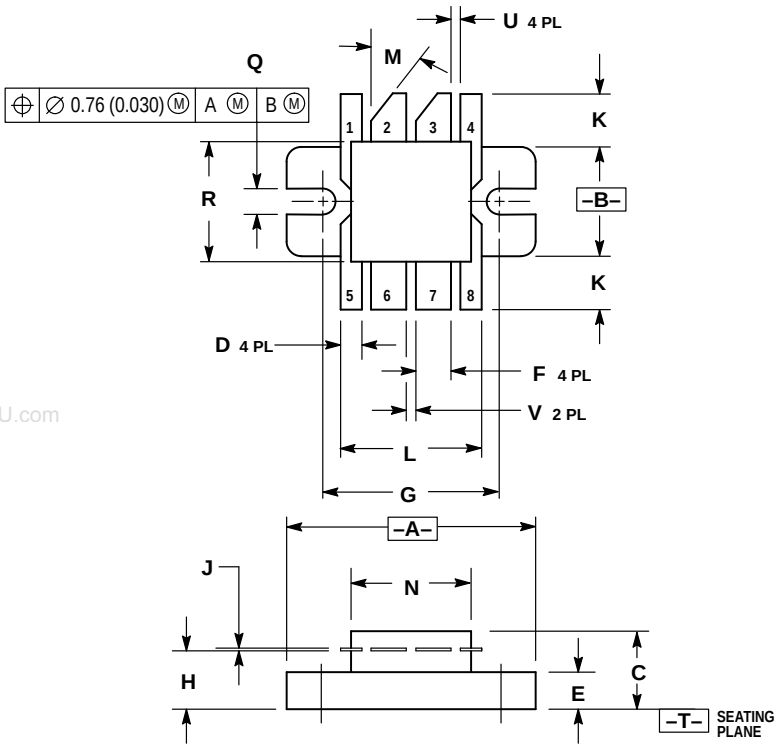


f MHz	Z_{in} OHMS	Z_{OL}* OHMS
100	0.72 + j0.44	9.0 – j6.0
225	0.72 + j2.62	5.2 – j1.8
400	3.88 + j5.72	3.6 + j0.53
450	3.84 + j2.8	3.2 + j1.2
500	1.26 + j3.01	3.0 + j2.0

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input/Output Impedance

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.60	23.11	0.890	0.910
B	9.52	10.03	0.375	0.395
C	6.65	7.16	0.262	0.282
D	1.60	1.95	0.063	0.077
E	2.94	3.40	0.116	0.134
F	2.87	3.22	0.113	0.127
G	16.51 BSC		0.650 BSC	
H	4.01	4.36	0.158	0.172
J	0.07	0.15	0.003	0.006
K	4.34	4.90	0.171	0.193
L	12.45	12.95	0.490	0.510
M	45° NOM		45° NOM	
N	1.051	11.02	0.414	0.434
Q	3.04	3.35	0.120	0.132
R	9.90	10.41	0.390	0.410
U	1.02	1.27	0.040	0.050
V	0.64	0.89	0.025	0.035

STYLE 1:
PIN 1. EMITTER (COMMON)
2. COLLECTOR
3. COLLECTOR
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE
7. BASE
8. EMITTER (COMMON)

CASE 744A–01
ISSUE C

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