MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MRF2001M

The RF Line

NPN SILICON MICROWAVE POWER TRANSISTOR

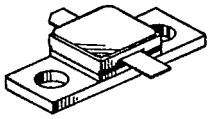
. . . designed for Class B and C *common base* broadband amplifier applications in the 1.7 to 2.3 GHz frequency range.

- Internal Input Matching for Broadband Operation
- Guaranteed Performance @ 2 GHz, 24 Vdc
  Output power = 1.0 Watt
  Minimum Gain = 8.5 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivation
- Characterized for Operation from 20 V to 28 V Supply Voltages

1.0 W 2 GHz

MICROWAVE POWER TRANSISTOR

NPN SILICON



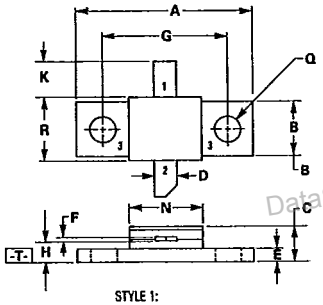
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	250	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	7.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	°C/W

(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ 0.13 (0.005) M T A M B M
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973

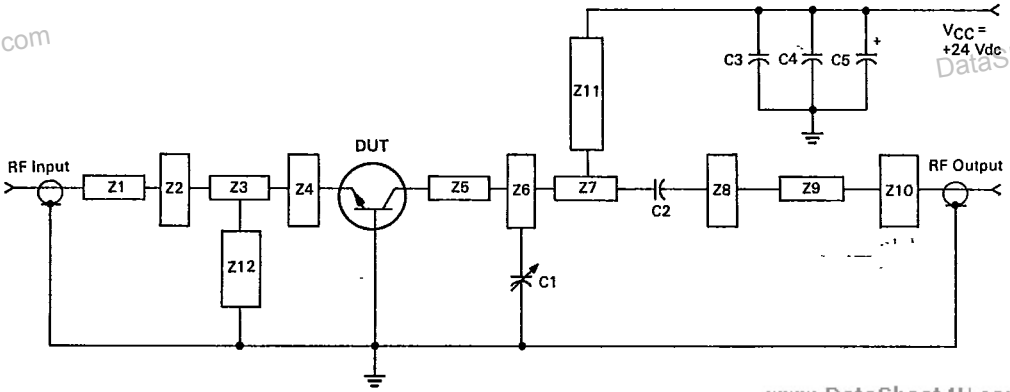
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	6.48	6.73	0.255	0.265
C	3.68	4.06	0.145	0.160
D	2.29	2.79	0.090	0.110
E	1.42	1.73	0.056	0.068
F	0.05	0.15	0.002	0.006
G	14.27 BSC		0.560 BSC	
H	2.29	2.79	0.090	0.110
K	3.43	4.19	0.135	0.165
N	7.87	8.38	0.310	0.330
Q	3.05	3.30	0.120	0.130
R	7.24	7.49	0.285	0.295

CASE 337-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	4.0	6.0	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 1.0 W, f = 2.0 GHz)	G_{PB}	8.5	9.5	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 1.0 W, f = 2.0 GHz)	η	35	40		
Load Mismatch (V_{CC} = 24 Vdc, P_{out} = 1.0 W, f = 2.0 GHz) VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1 — 2.0 GHz TEST CIRCUIT



Z1–Z12 — Microstrip, See Photomaster
C1 — 0.6–4.5 pF Johanson 7271
C2, C3 — 56 pF Chip Capacitor
C4 — 0.1 μF
C5 — 10 μF, 35 V
Board Material — 0.0312" Teflon Fiberglass
ϵ_r = 2.5 ± 0.05

FIGURE 2 — OUTPUT POWER versus INPUT POWER
(f = 1.7 GHz)

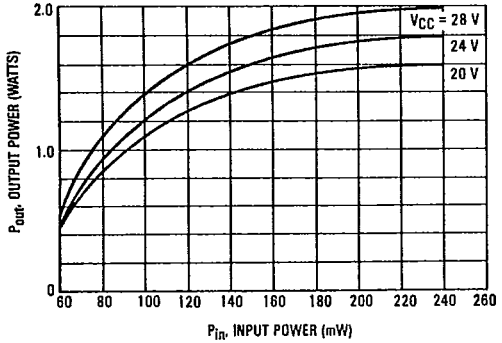


FIGURE 3 — OUTPUT POWER versus INPUT POWER
(f = 2.0 GHz)

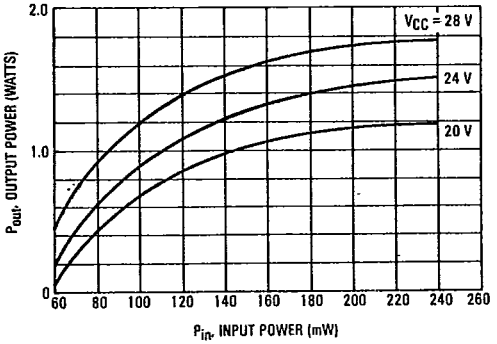


FIGURE 4 — OUTPUT POWER versus INPUT POWER
(f = 2.3 GHz)

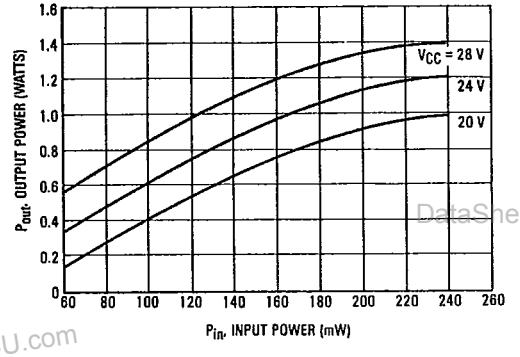


FIGURE 5 — POWER GAIN versus FREQUENCY

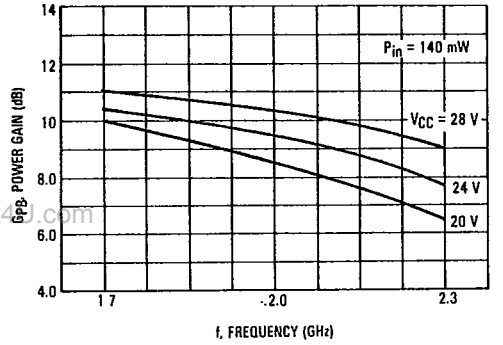
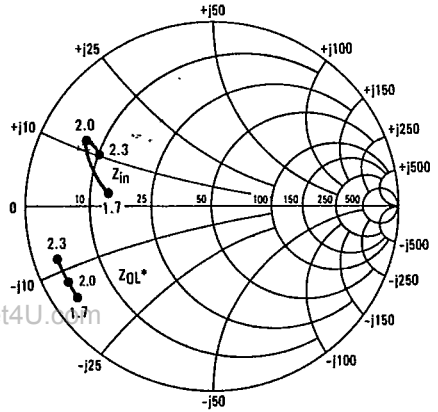


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



Coordinates in Ohms

V_{CC} = 24 V, P_{in} = 140 mW

f GHz	Z_{in} Ohms	Z_{OL}* Ohms
1.7	15.5 + j 3.0	4.5 – j15.0
2.0	7.5 + j11.0	4.0 – j12.0
2.3	10.0 + j10.0	3.0 – j 7.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 — 2 GHz TEST AMPLIFIER

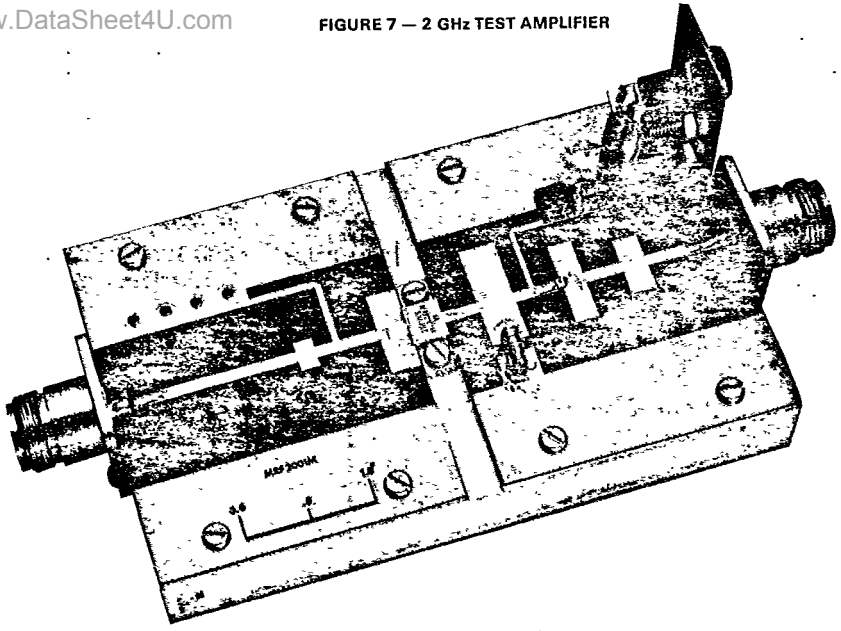
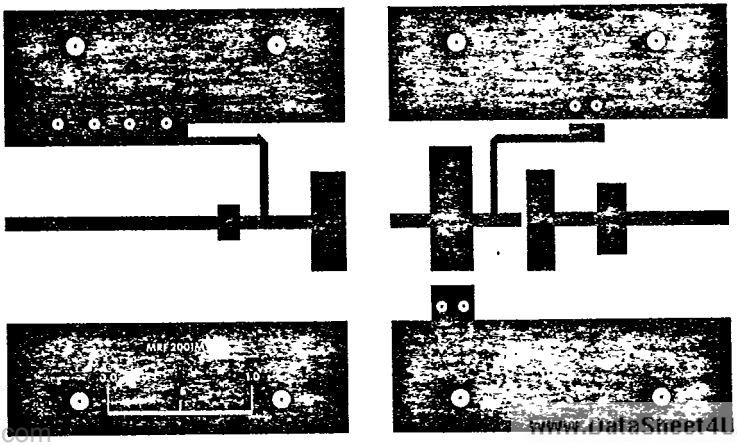


FIGURE 8 — PRINTED CIRCUIT BOARD LAYOUT — 2.0 GHz TEST CIRCUIT



◎ Denotes Eyelet

◎ 4-40 Screw Placement

NOTE: The Printed Circuit Board shown is 75% of the original.