MR36V08G57C

262,144–Page × 1,024 x 32–Bit P2ROM (LVNROM)

FEATURES

■ Memory Configuration
- 262,144 x 1,024 x 32 bit
- Multiplexed Command/Address/Data

■ Page Read Operation
- Page Size : 4,096 byte
- Random access time : 1.0us (max) for block read
  1.8us (max) for random read
- Sequential Read : 40ns (min)
- Read Mode
  Continuous Read : no wait for next page.
  Page Read : need wait time for next page

■ Power Supply Voltage
- Vcc = 3.0 V to 3.6 V

PACKAGES

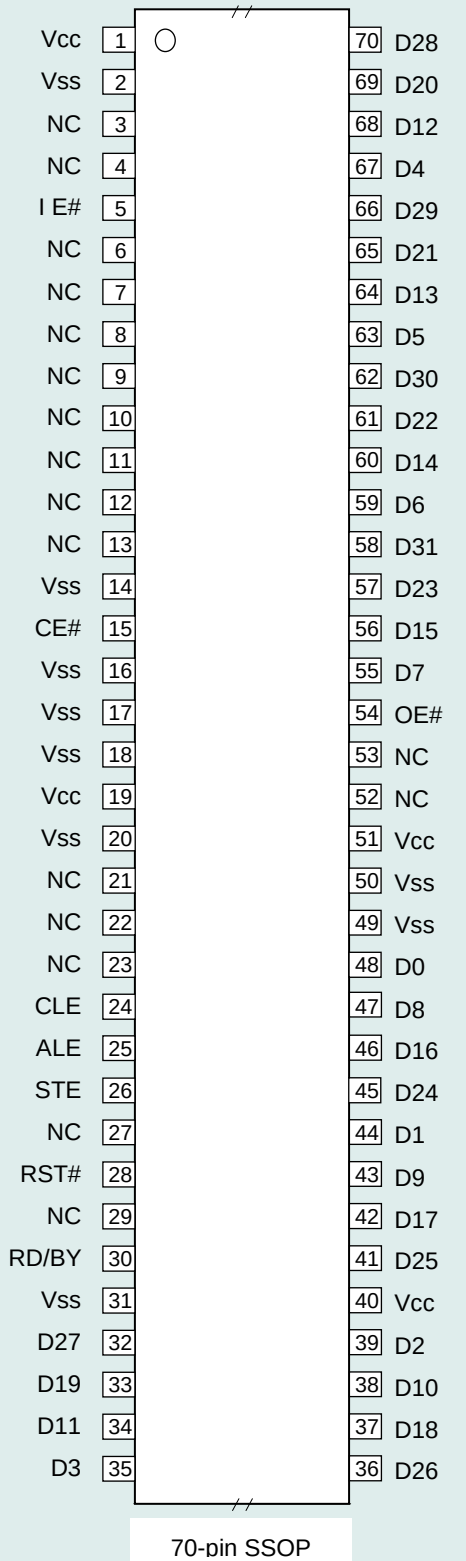
·70-pin plastic SSOP (P-SSOP70-500-0.80-EK-MC)

P2ROM ADVANCED TECHNOLOGY

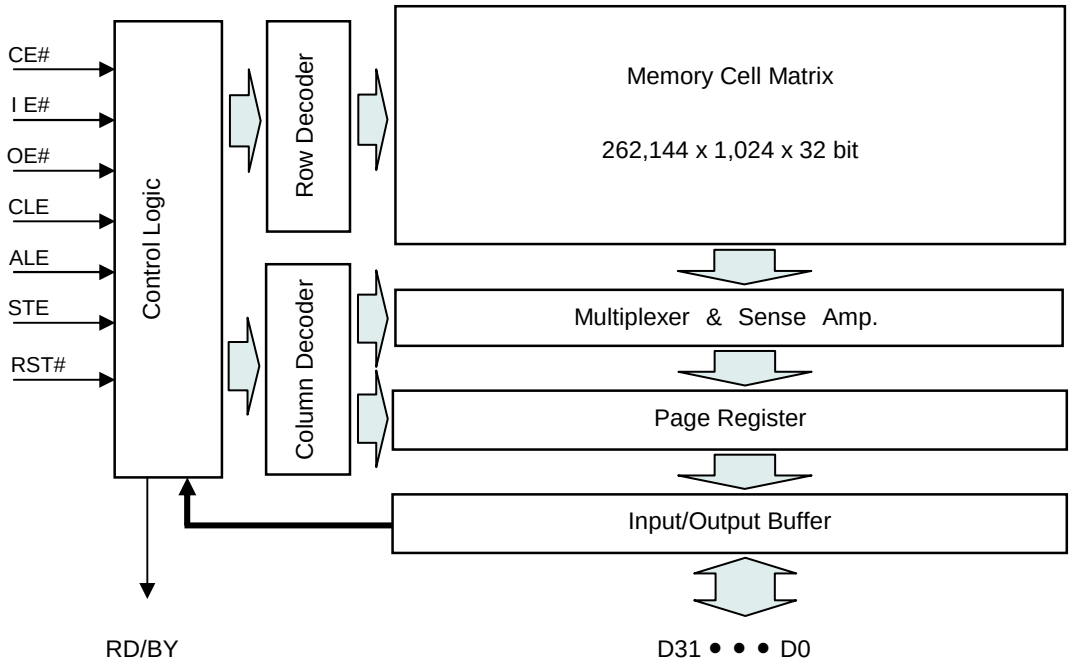
P2ROM stands for Production Programmed ROM. This exclusive LAPIS Semiconductor's technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

· **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
· **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
· **No additional programming charge,** unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
· **Custom Marking is** available at no additional charge.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin name	I/O	Functions
D31 to D0	I/O	**Command/Address Input, Data Outputs** The Data I/O are used to input command and address, and to output data during read operation. The Data I/O float to high-z when the device is deselected or the outputs are disabled.
CE#	I	**Chip Enable** The CE# input activates the read operation. The CE# input shall stay “low” during the read operation. The CE# input goes to “high”, the device returns to standby mode.
IE#	I	**Input Enable** The IE# input controls the sequential data input during the read operation. Commands and address are latched on the rising edge of the IE# pulse.
OE#	I	**Output Enable** The OE# input controls the sequential data output during read operation. Data is valid tOEA after the falling edge of OE# pulse, and the Data I/O goes to high-z tOEZ after the rising edge of OE# pulse.
CLE	I	**Command Latch Enable** The CLE input activates the latch of command inputs. When CLE is “high”, the inputs are latched on the rising edge of IE# pulse.
ALE	I	**Address Latch Enable** The ALE input activates the latch of address inputs. When ALE is “high”, the inputs are latched on the rising edge of IE# pulse.
STE	I	**Status Output Enable** The STE input activates the output of status. When STE is “high”, the status is valid tOEA after the falling edge of OE# pulse, and the Data I/O goes to high-z at tOEZ after the rising edge of OE# pulse.
RD/BY	O	**Ready/Busy Output** The RD/BY output indicates the status of the device operation. When the RD/BY is “low”, it indicates the read operation is not ready. When the read operation is ready, the RD/BY goes “high”.
RST#	I	**Reset** The RST# reset the whole circuits with low state. The RST# must be low at power on.
V_{CC}	-	**Power**
V_{SS}	-	**Ground**
NC	-	**No Connection**

COMMAND INPUT

The lower 8 bits, D7 to D0, of the data inputs are valid, and the upper 24 bits, D31 to D8, of the data inputs are "don't care" in the command input.
Both Read and Stop command inputs are allowed in the ready state (RD/BY output = "high") only. The Reset command input is allowed in any states.

Command	1st Cycle (CMD1)	2nd Cycle (CMD2)	NOTE
Continuous Read	00[H]	33[H]	This command is to read data sequentially from the start address. This command continues until the next command is entered, the maximum logic address is reached. This command does NOT go to "busy" state at each page boundary.
Page Read	00[H]	30[H]	This command is to read data sequentially from the start address. This command continues until the next command is entered, the maximum logic address is reached. This command goes to "busy" state (RD/BY = "low") at each page boundary. The page size is 4K-Byte.
Stop	F0[H]	—	This command is to stop the read command.
Reset	FF[H]	—	This command is to reset (software reset) in any operations.

ADDRESS INPUT

The lower 8 bits, D7to D0, of the data inputs are valid, and the upper 24 bits, D31 to D8, of the data inputs are "don't care" in the address input.

The 1st cycle and 2nd cycle of the address input set up the column address. The column address can be set from 000[H] to 3FF[H]. The 3rd cycle to 5th cycle of the address input set up the row address. The row address can be set from 00000[H] to 3FFFF[H].

Address Inputs	D[31:8]	D7	D6	D5	D4	D3	D2	D1	D0
1st (CA0)	Don't care	A7	A6	A5	A4	A3	A2	A1	A0
2nd (CA1)	Don't care	L	L	L	L	L	L	A9	A8
3rd (RA0)	Don't care	A17	A16	A15	A14	A13	A12	A11	A10
4th (RA1)	Don't care	A25	A24	A23	A22	A21	A20	A19	A18
5th (RA2)	Don't care	L	L	L	L	L	L	A27	A26

STATUS OUTPUT

The lower 8bits, D7 to D0, and another 8bits, D23 to D16, of the data outputs are used to output the status bits. Other bits of the data outputs fixed “low” during status output.

Status Output Bit	Status value	NOTE
D7 (D23)	0	—
D6 (D22)	Ready/Busy	This field indicates RD/BY output, Ready = H and Busy = L. This status value is the same behavior with the RD/BY output signal.
D5 (D21)	0	—
D4 (D20)	CMD End	This field indicates command operation status. “H” indicates the command operation is completed, and “L” indicates the command operation is in process.
D3 (D19)	CMD Error	This field indicates command input status. “H” indicates an error command input such as invalid command code or invalid address. “L” indicates a correct command input.
D2 (D18)	0	—
D1 (D17)	0	—
D0 (D16)	0	—

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Ta	—	0 to 70	°C
Storage temperature	Tstg		–55 to 125	°C
Input voltage	V_I	relative to V_{SS}	–0.3 to V_{CC}+0.3	V
Output voltage	V_O		–0.3 to V_{CC}+0.3	V
Power supply voltage	V_{CC}		–0.3 to 4.6	V
Output short circuit current	Ios	—	10	mA
Power dissipation per package	P_D	Ta=25°C	1.0	W

PIN CAPACITANCE

(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	V_I = 0 V	—	—	20	pF
Output	C_{OUT}	V_O = 0 V	—	—	20	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{CC}	—	—	20	µA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}	—	—	20	µA
V_{CC} power supply current (Read)	I_{CCA1}	tOEC = 50ns Output Load = 50 pF	—	—	180	mA
V_{CC} power supply current (Standby)	I_{CCS}	CE# = V_{IH}	—	—	40	mA
Input “H” level	V_{IH}	—	2.0	—	V_{CC}+0.3*	V
Input “L” level	V_{IL}	—	–0.3**	—	0.7	V
Output “H” level	V_{OH}	I_{OH} = –2 mA	2.4	—	—	V
Output “L” level	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V

Voltage is relative to V_{SS}.

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC Characteristics

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

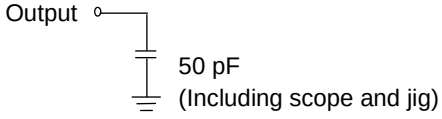
Parameter	Symbol	Min.	Max.	Unit
CLE/ALE/STE Setup time for OE#	t_{ASO}	5	—	ns
CLE/ALE/STE Hold time for OE#	t_{AHO}	5	—	ns
CE# Setup time for OE#	t_{CESO}	5	—	ns
CE# Hold time for OE#	t_{CEHO}	5	—	ns
CE# high time	t_{CEH}	10	—	ns
OE# Cycle time	t_{OEC}	40	—	ns
OE# Pulse width	t_{OEP}	24	—	ns
OE# High Hold time	t_{OEH}	14	—	ns
OE# Access Time	t_{OEA}	—	20	ns
OE# High to Output High-Z	t_{OEZ}	—	15	ns
CLE/ALE/STE Setup time for IE#	t_{ASS}	5	—	ns
CLE/ALE/STE Hold time for IE#	t_{AHS}	5	—	ns
CE# Setup time for IE#	t_{CESS}	5	—	ns
CE# Hold time for IE#	t_{CEHS}	5	—	ns
IE# Cycle time	t_{IEC}	40	—	ns
IE# Pulse width	t_{IEP}	19	—	ns
IE# High Hold time	t_{IEH}	19	—	ns
Data Setup time	t_{DS}	10	—	ns
Data Hold time	t_{DH}	5	—	ns
IE# High to Busy	t_{IEB}	—	25	ns
OE# High to Busy	t_{OEB}	—	25	ns
Ready to IE# Low	t_{RIE}	25	—	ns
Ready to OE# Low	t_{ROE}	25	—	ns
CMD to Ready (Continuous Read)	t_{BSY1}	800	1800	ns
CMD to Ready (Page Read)	t_{BSY2}	800 / 125[*1]	1800 / 500[*1]	ns
Wait for Page read	t_{BSYR}	125	500	ns
Wait after STOP CMD while Read	t_{BSYS}	125	500	ns
Reset time	t_{RST}	125	500	ns

(*1) When the continuous address from the previous read cycle is input, "CMD to Ready (t_{BSY2})" is the same as "Wait for Page Read (t_{BSYR})".

Measurement conditions

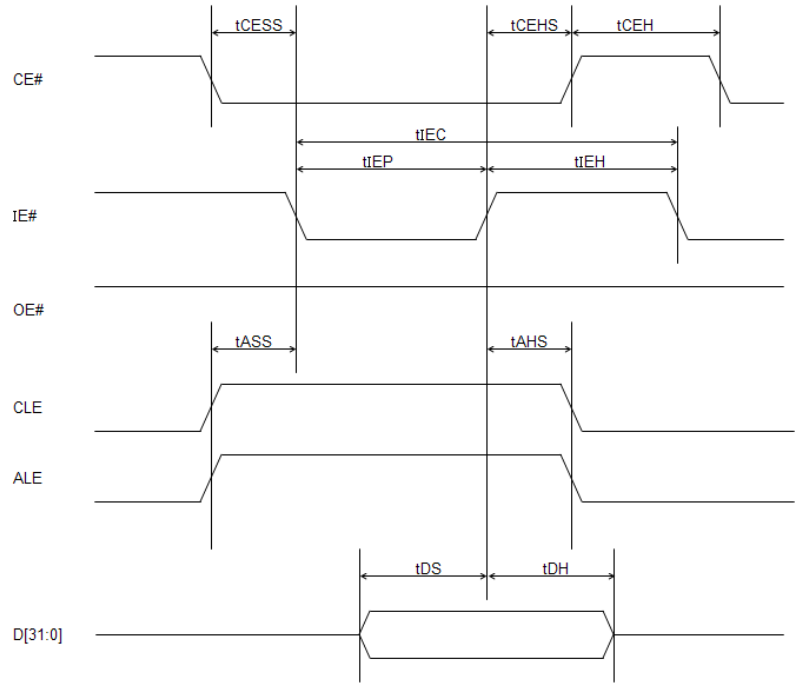
Input signal level---------- 0 V/3 V
Input timing reference level ---------- 1/2Vcc
Output load ---------- 50 pF
Output timing reference level---------- 1/2Vcc

Output load

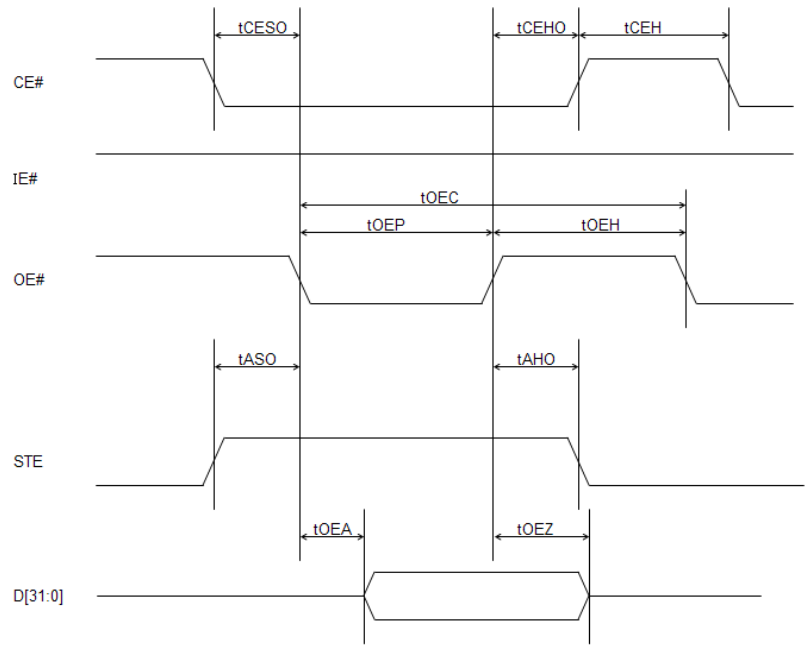


TIMING CHART (READ CYCLE)

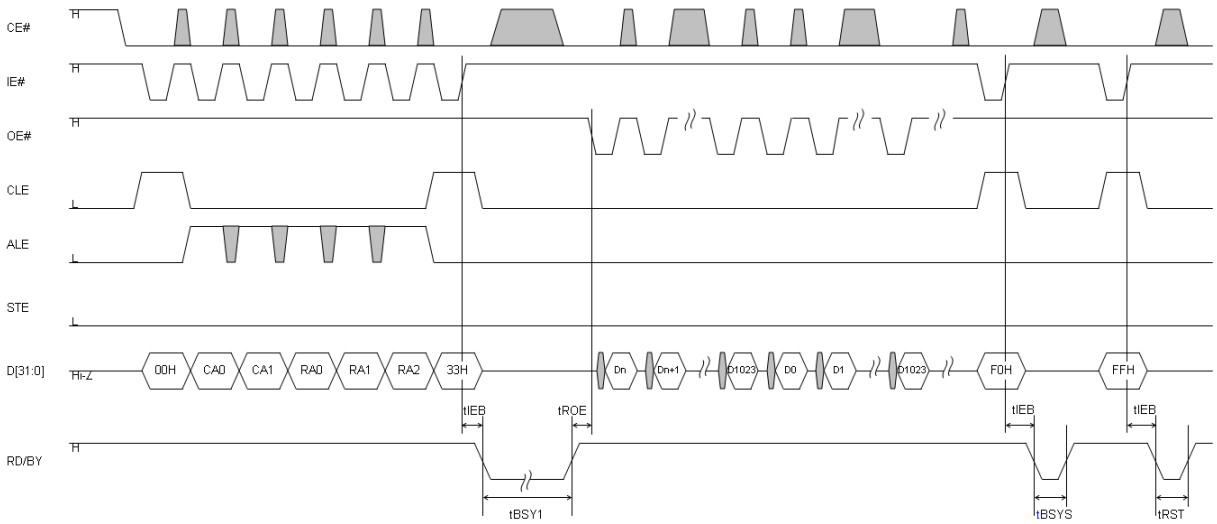
Data Input Cycle



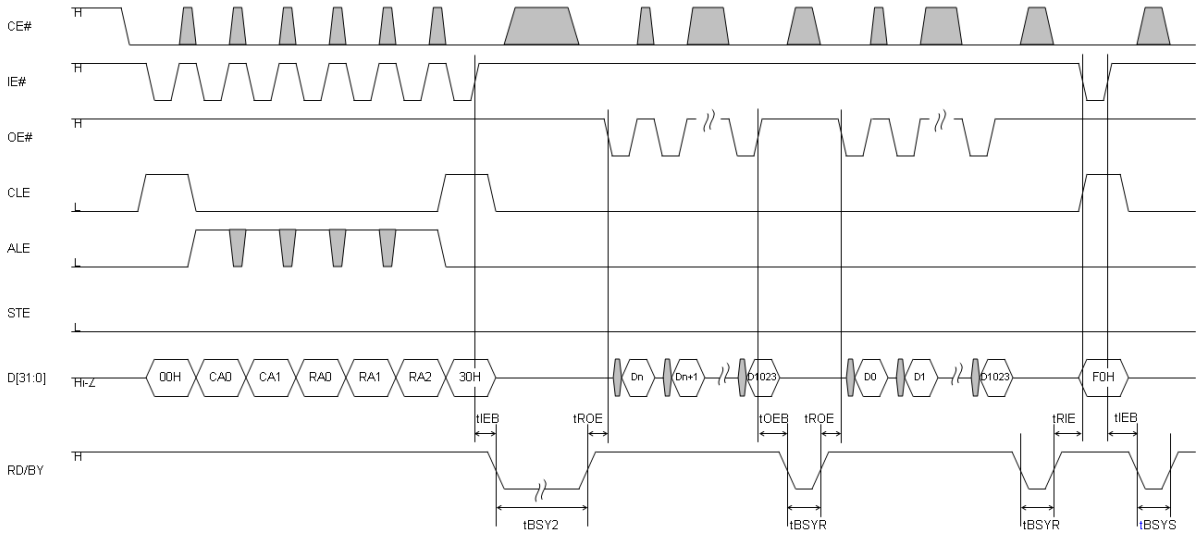
Data Output Cycle



Data Read Cycle (Continuous Read)



Data Read Cycle (Page Read)



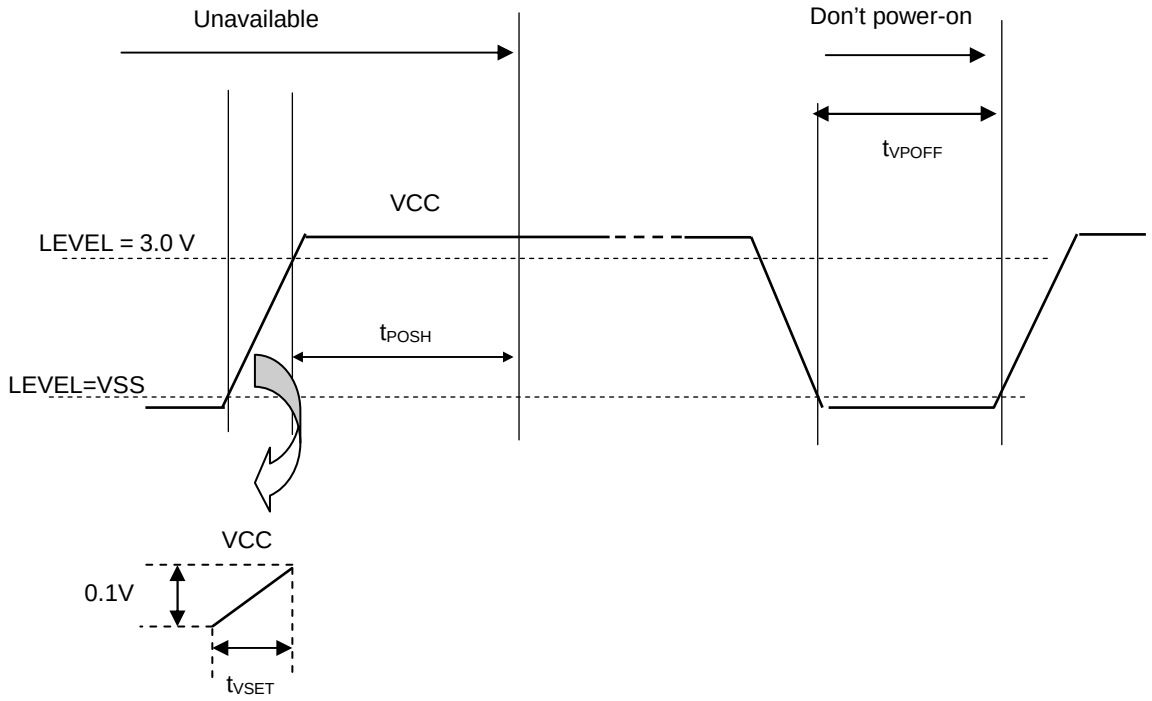
Note: Data Read Cycle would end without a stop command (F0h) after reading the end address.
At that time, RD/BY signal would be LOW once for tBSYS.

Power ON Characteristics / Reset

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

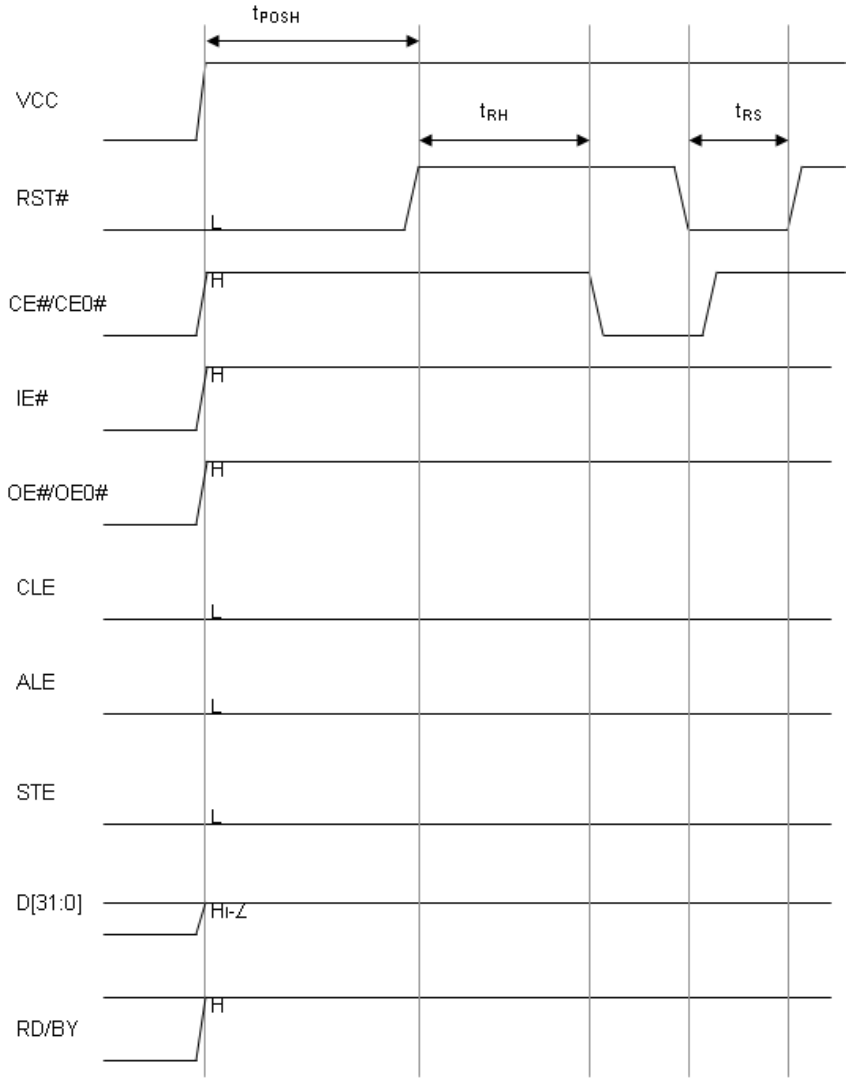
Parameter	Symbol	Condition	Min.	Max.	Unit
VCC set up time	t_{VSET}	—	5	270	us
Power on sequence hold time	t_{POSH}	—	1	—	ms
Power off hold time	t_{VPOFF}	—	1	—	ms
Reset hold time	t_{RH}	—	1	—	ms
Rest time	t_{RS}	—	100	—	ns

TIMING CHART (POWER ON)



Note: A start-up delay of 1ms is required after power-on.
If you power-off VCC ,you must wait 1ms to power-on.
CE# must be HIGH and RST# must be LOW while VCC power on sequence.

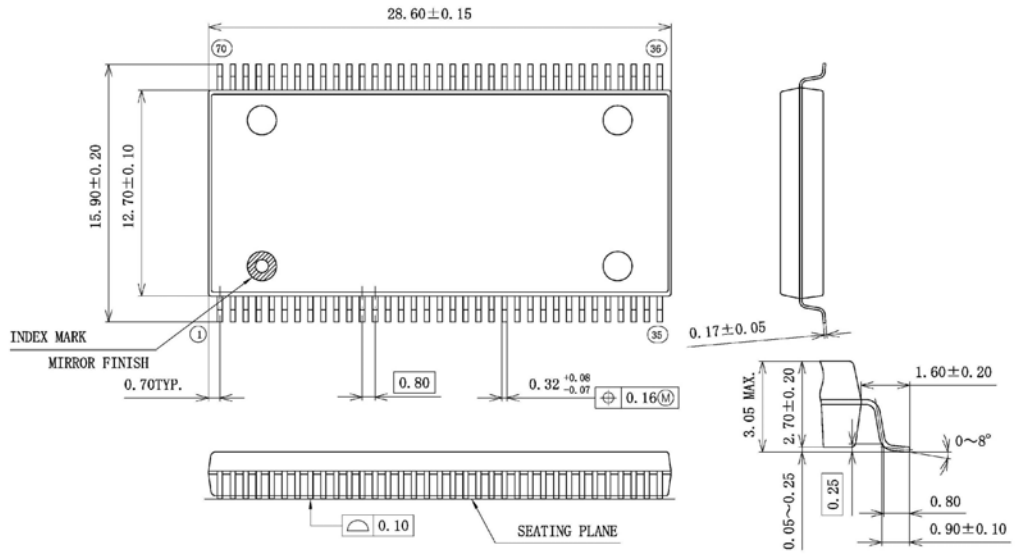
TIMING CHART (RESET)



PACKAGE DIMENSIONS

(Unit: mm)

P-SSOP70-500-0.80-EK-MC



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	2.23 TYP.
Rev. No./Last Revised	2/Oct. 10, 2008

LAPIS Semiconductor Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR36V08G57C-002-01	Mar. 25 2010	–	–	Edition 1
FEDR36V08G57C-002-02	Sep. 15 2010	1,7,8	1,7,8	t_{BSY} defined separately to t_{BSY1} and t_{BSY2}.
		9	9	t_{RST} description added.
		10,11	10,11	t_{RS} description added.

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