

# MQ1470VP LDMOS TRANSISTOR

Document Number: MQ1470VP  
Preliminary Datasheet V1.0

## 750W, 50V High Power RF LDMOS FETs

### Description

The MQ1470VP is a 750-watt, high performance, internally matched LDMOS FET, designed for avionics applications with frequencies 1.2 to 1.4GHz

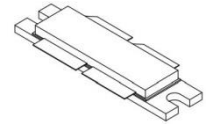
It is featured for high power and high ruggedness.

**It is recommended to use this device under pulse condition only**

- Typical Pulse Performance (on innogration wide band test fixture with device soldered):

$V_{ds} = 50\text{ V}$ ,  $I_{dq} = 50\text{ mA}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$

### MQ1470VP



Test signal	Freq(MHz)	P1dB(W)	Gp(dB)@P1dB	Eff(%)@P1dB	P3dB(W)
Pulse width:100uS Duty cycle: 10%	1200	1016	12.9	45	1101
	1280	985	14.3	49	1025
	1400	855	13.4	45	1015
Pulse width:100uS Duty cycle: 20%	1200	930	12.7	43	995
	1280	914	14	47	1026
	1400	785	13.1	43	922

### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	115	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+55	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}\text{C}$
Case Operating Temperature	$T_c$	+150	$^{\circ}\text{C}$
Operating Junction Temperature	$T_j$	+225	$^{\circ}\text{C}$

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,Case Temperature 80°C, 870W Pout, Pulse width: 100us, duty cycle: 10%, $V_{ds}=50\text{ V}$ , $I_{DQ} = 100\text{ mA}$	$R_{\theta JC}$	0.02	$^{\circ}\text{C/W}$

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
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Human Body Model (per JESD22--A114)	Class 2
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**Table 4. Electrical Characteristics** (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>DC Characteristics</b>					
Drain-Source Breakdown Voltage (V <sub>GS</sub> =0V; I <sub>D</sub> =100uA)	V <sub>DSS</sub>	115			V
Zero Gate Voltage Drain Leakage Current (V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V)	I <sub>DSS</sub>			10	μA
Gate--Source Leakage Current (V <sub>GS</sub> = 6 V, V <sub>DS</sub> = 0 V)	I <sub>GSS</sub>			1	μA
Gate Threshold Voltage (V <sub>DS</sub> = 50V, I <sub>D</sub> = 600 uA)	V <sub>GS(th)</sub>		1.6		V
Gate Quiescent Voltage (V <sub>DD</sub> = 50 V, I <sub>DQ</sub> = 50 mA, Measured in Functional Test)	V <sub>GS(Q)</sub>		3		V

**Functional Tests (In Innogration test fixture, 50 ohm system) :** Pulse CW Signal Measurements. (Pulse Width=100s, Duty cycle=10%), Pin=46dBm

Power Gain @ Pout	Gp		13.3		dB
1dB compressed point	P1dB	750	850		W
Drain Efficiency@Pout	η <sub>D</sub>		45.0		%
Input Return Loss	IRL		-7		dB

## Reference Circuit of Test Fixture

(Layout file upon request) PCB: Roger 4350B, 30mils

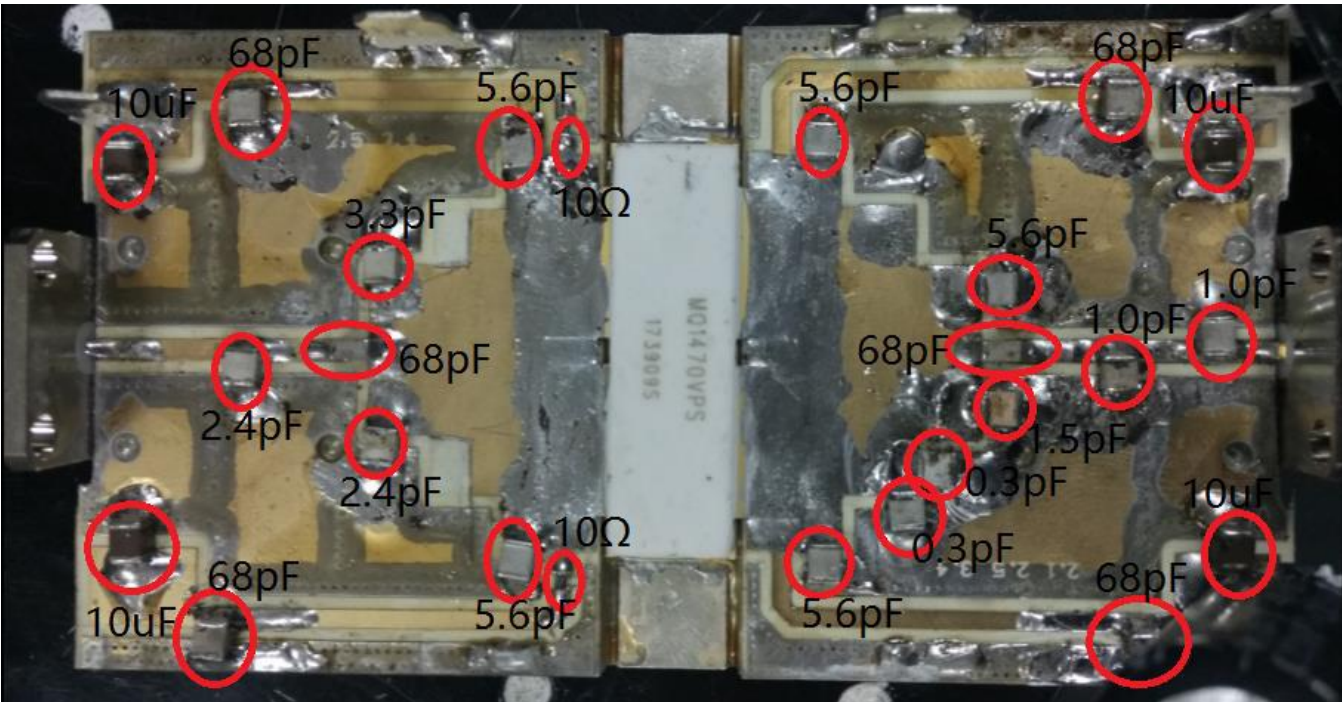


Figure 1. Test Circuit Component Layout

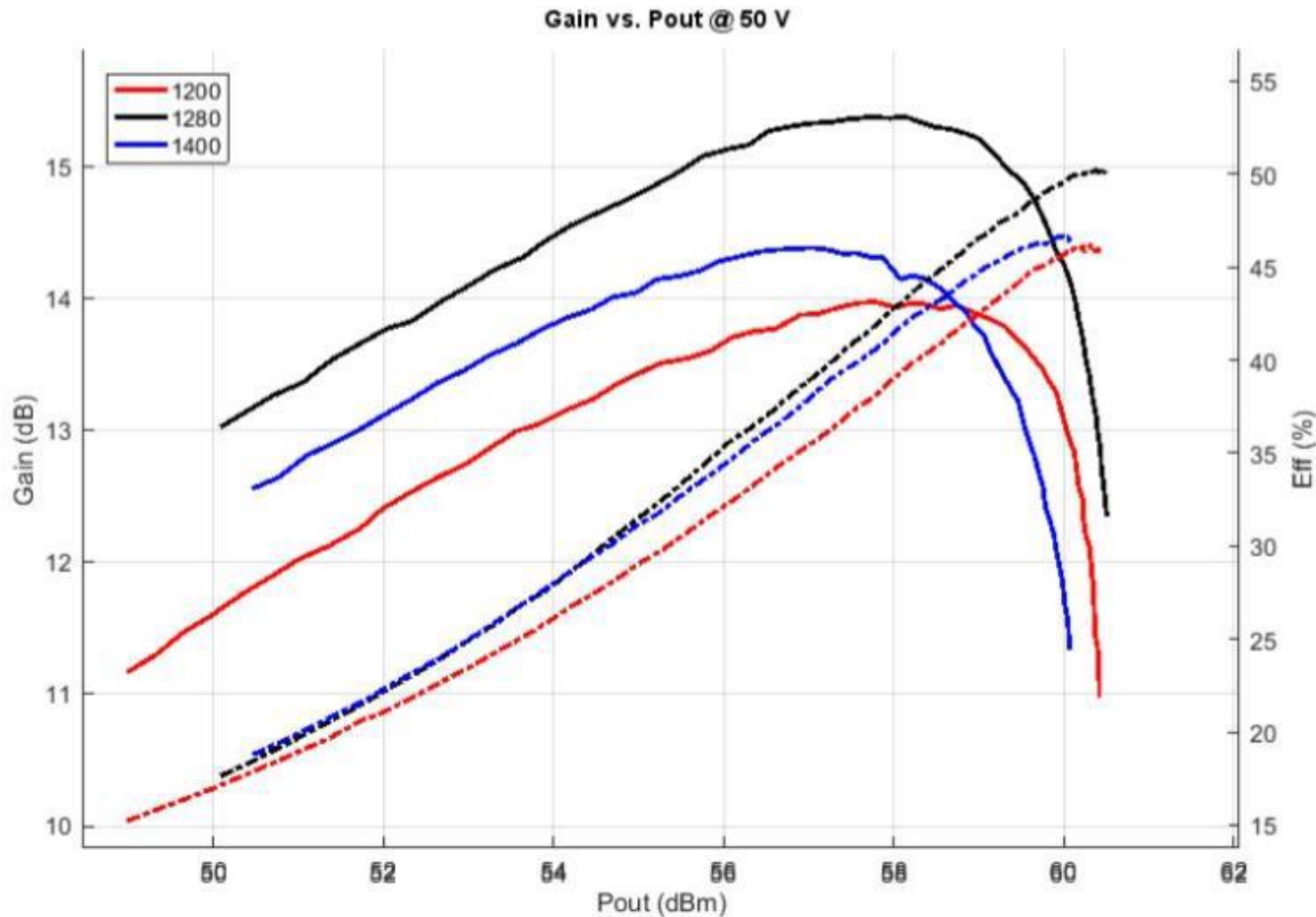
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## TYPICAL CHARACTERISTICS

Pulse width:100uS, duty cycle: 10%, Vds = 50 V, Idq = 100 mA, TA = 25 °C

Figure 2: Power gain and Efficiency as a Function of Pout



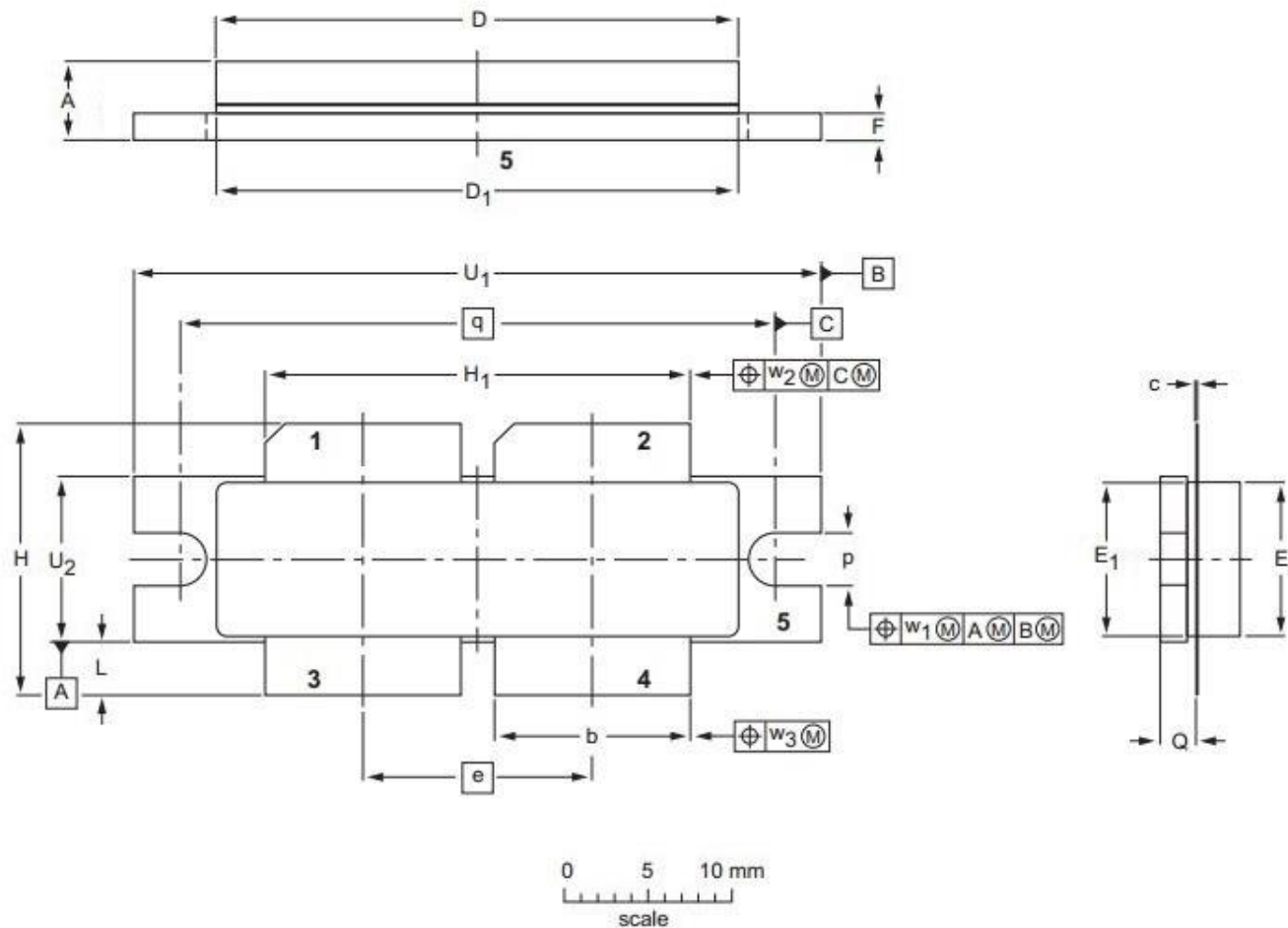
Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1200	60.07	1016.48	45.79	12.93	60.42	1101.46	45.72
1280	59.94	985.72	49.41	14.32	60.51	1124.31	50.04
1400	59.32	855.11	45.55	13.39	60.07	1015.86	46.34

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## Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	W <sub>1</sub>	W <sub>2</sub>	W <sub>2</sub>
Mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	3.30	2.26	35.56	41.28	10.29	0.25	0.51	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
Inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.130	0.089	1.400	1.625	0.405	0.01	0.02	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

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## Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2018/8/4	Rev 1.0	Preliminary Datasheet Creation

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