High Voltage PNP Epitaxial Planar Transistor

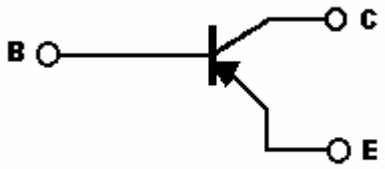
MPSA94

Description

- High breakdown voltage. (BV_{CEO}=-400V)
- Low saturation voltage, typically $V_{CE(sat)}$ = -0.08V at Ic/I_B =-10mA/-1mA.
- Wide SOA (safe operation area).
- Complementary to MPSA44.
- Pb-free lead plating and halogen-free package.

Symbol

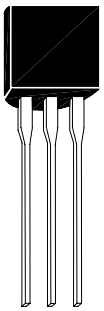
MPSA94



B：Base
C：Collector
E：Emitter

Outline

TO-92



E B C

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-400	V
Collector-Emitter Voltage	V_{CEO}	-400	V
Emitter-Base Voltage	V_{EBO}	-6	V
Collector Current	I_C	-300	mA
Power Dissipation	P_D	625	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-400	-	-	V	I_C=-50μA
BV_{CEO}	-400	-	-	V	I_C=-1mA
BV_{EBO}	-6	-	-	V	I_E=-50μA
I_{CBO}	-	-	-10	μA	V_{CB}=-400V
I_{EBO}	-	-	-10	μA	V_{EB}=-6V
I_{CES}	-	-	-10	μA	V_{CE}=-400V, V_{BE}=0V
$V_{CE(sat)}$ 1	-	-	-0.2	V	I_C=-1mA, I_B=-0.1mA
*$V_{CE(sat)}$ 2	-	-0.08	-0.3	V	I_C=-10mA, I_B=-1mA
*$V_{CE(sat)}$ 3	-	-0.12	-0.6	V	I_C=-50mA, I_B=-5mA
*$V_{BE(sat)}$	-	-	-0.9	V	I_C=-20mA, I_B=-2mA
h_{FE} 1	70	-	-	-	V_{CE}=-10V, I_C=-1mA
*h_{FE} 2	82	-	270	-	V_{CE}=-10V, I_C=-10mA
*h_{FE} 3	50	-	-	-	V_{CE}=-10V, I_C=-50mA
*h_{FE} 4	40	-	-	-	V_{CE}=-10V, I_C=-100mA
Cob	-	-	8	pF	V_{CB}=-10V, I_E=0A,f=1MHz

*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

Classification Of h_{FE} 2

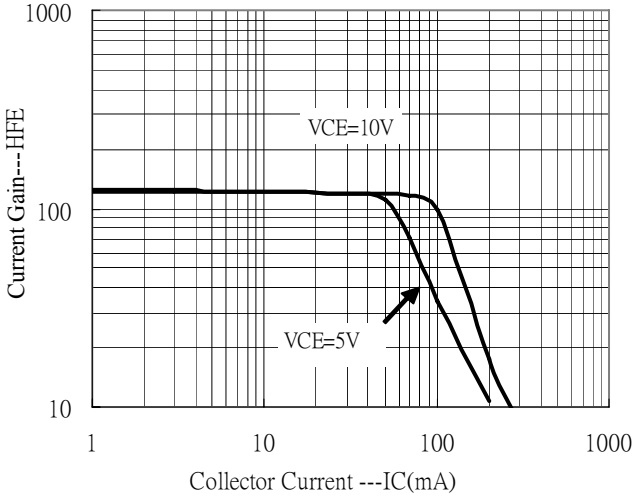
Rank	P	Q
Range	82~180	120~270

Ordering Information

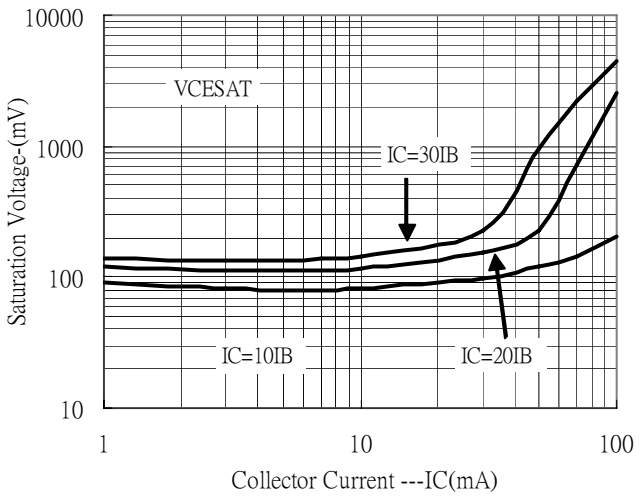
Device	Package	Shipping
MPSA94, T/B	TO-92 (Pb-free lead plating and halogen-free)	2000 pcs / Tape & Box
MPSA94, bulk	TO-92 (Pb-free lead plating and halogen-free)	1000 pcs/ bag, 10 bags/box, 10boxes/carton

Typical Characteristics

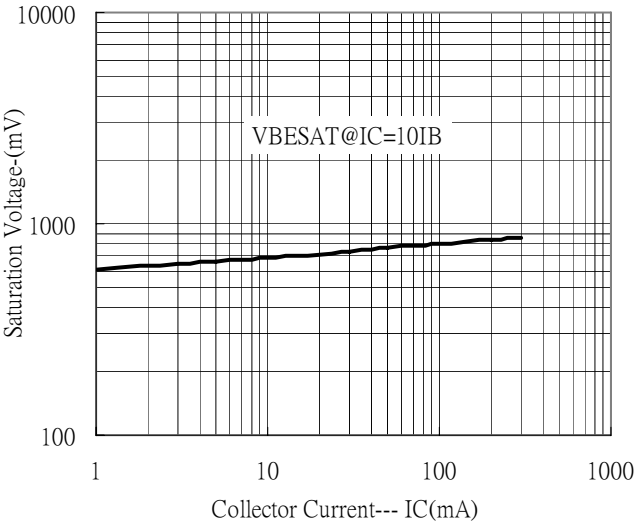
Current Gain vs Collector Current



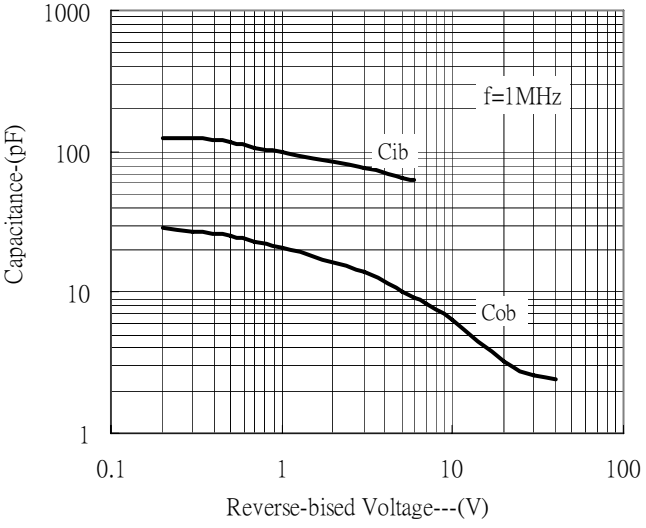
Saturation Voltage vs Collector Current



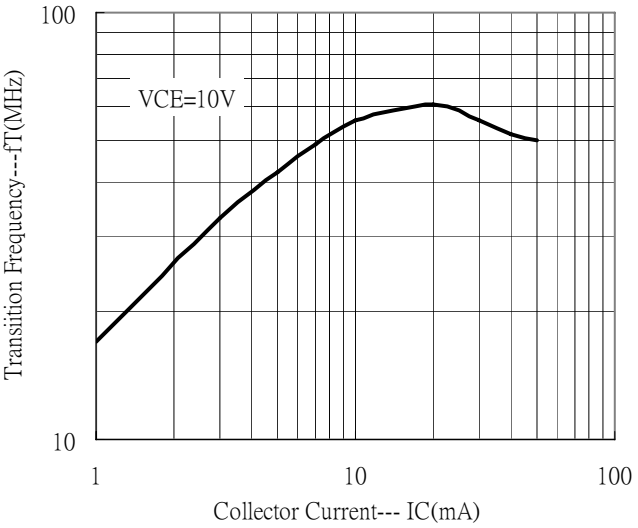
Saturation Voltage vs Collector Current



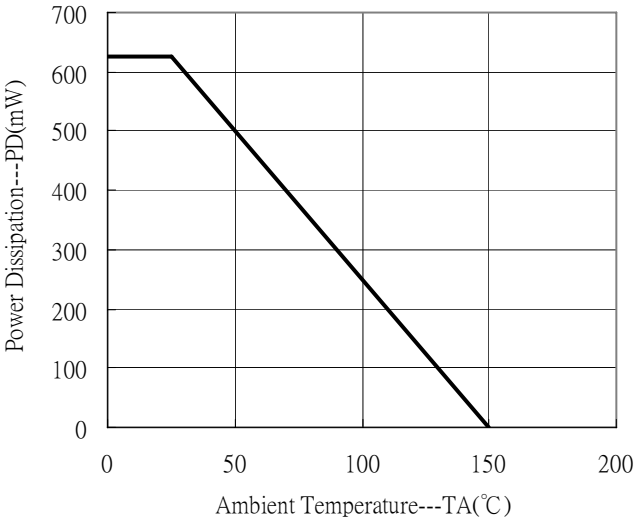
Capacitance Characteristics



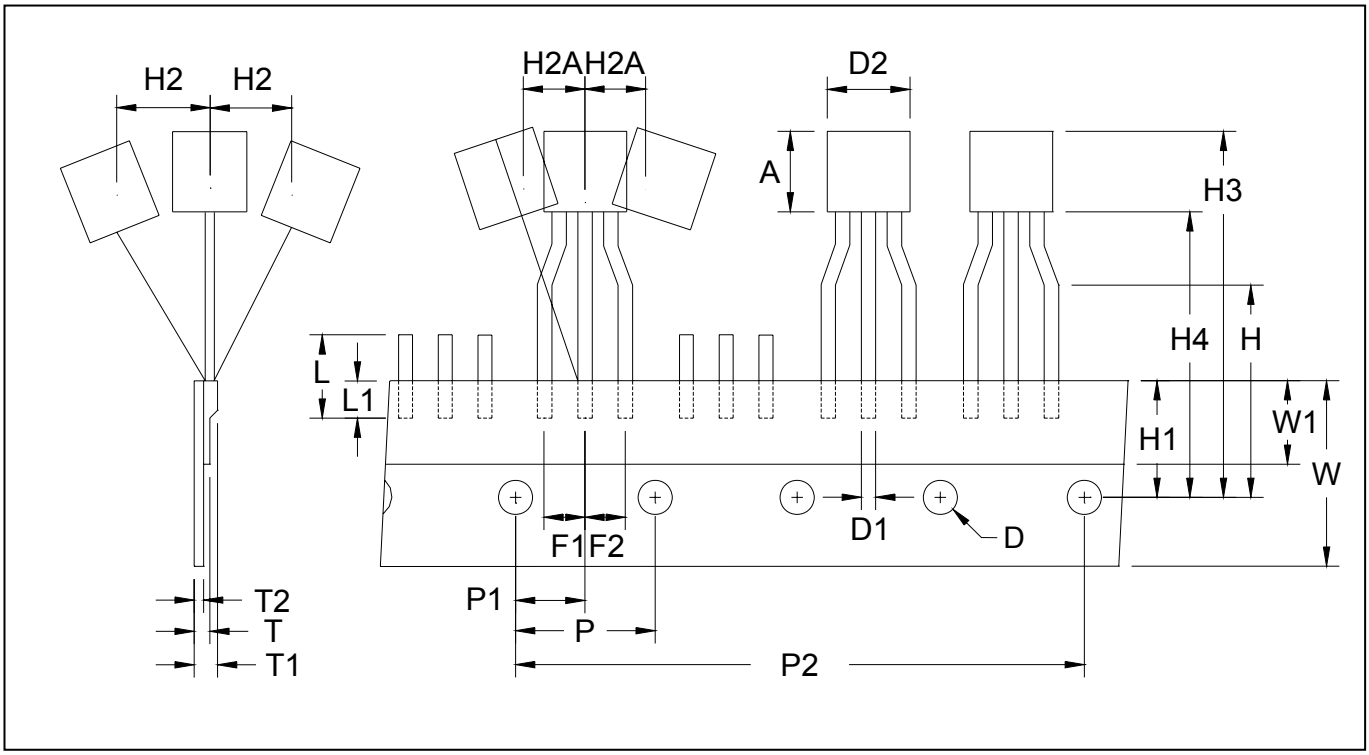
Transition Frequency vs Collector Current



Power Derating Curve



TO-92 Taping Outline



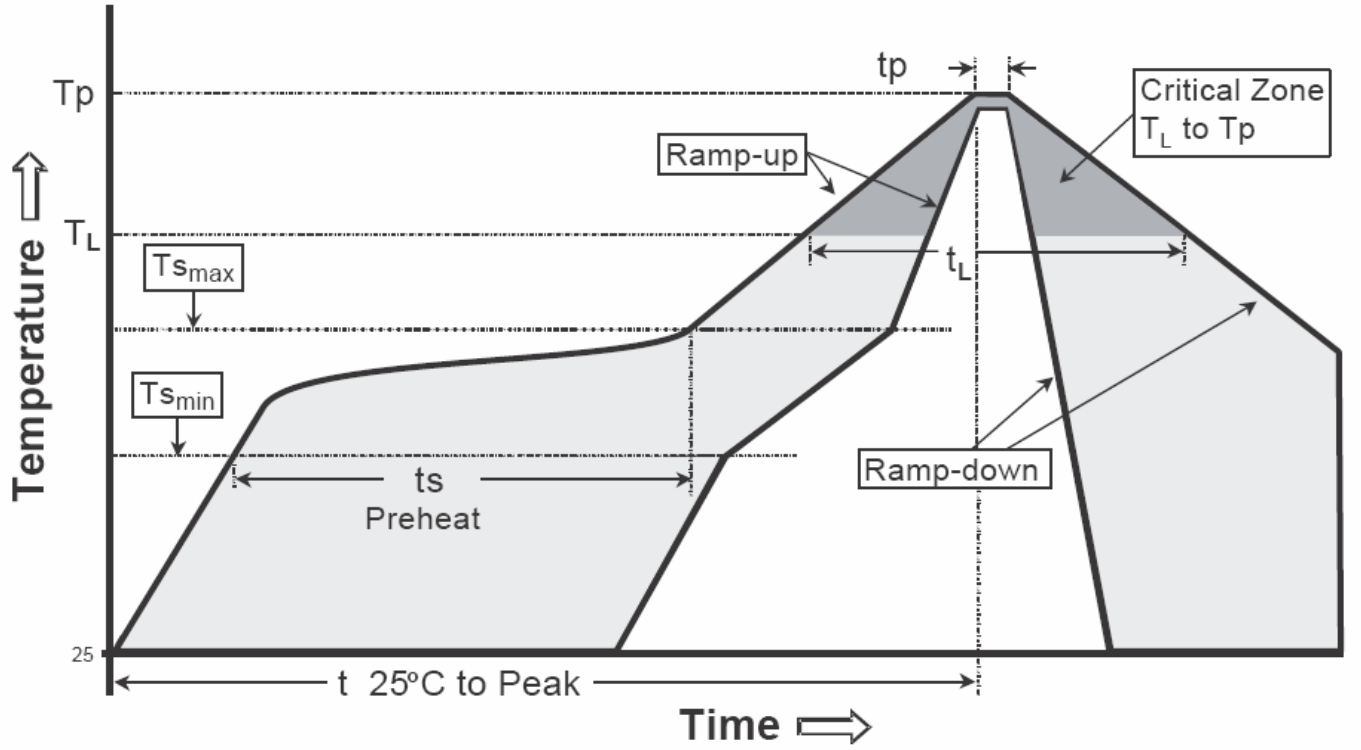
DIM	Item	Millimeters	
		Min.	Max.
A	Component body height	4.33	4.83
D	Tape Feed Diameter	3.80	4.20
D1	Lead Diameter	0.36	0.53
D2	Component Body Diameter	4.33	4.83
F1,F2	Component Lead Pitch	2.40	2.90
F1,F2	F1-F2	-	±0.3
H	Height Of Seating Plane	15.50	16.50
H1	Feed Hole Location	8.50	9.50
H2	Front To Rear Deflection	-	1
H2A	Deflection Left Or Right	-	1
H3	Component Height	-	27
H4	Feed Hole To Bottom Of Component	-	21
L	Lead Length After Component Removal	-	11
L1	Lead Wire Enclosure	2.50	-
P	Feed Hole Pitch	12.50	12.90
P1	Center Of Seating Plane Location	5.95	6.75
P2	4 Feed Hole Pitch	50.30	51.30
T	Over All Tape Thickness	-	0.55
T1	Total Taped Package Thickness	-	1.42
T2	Carrier Tape Thickness	0.36	0.68
W	Tape Width	17.50	19.00
W1	Adhesive Tape Width	5.00	7.00
-	20 pcs Pitch	253	255

Note : All temperatures refer to topside of the package, measured on the package body surface.

Recommended wave soldering condition

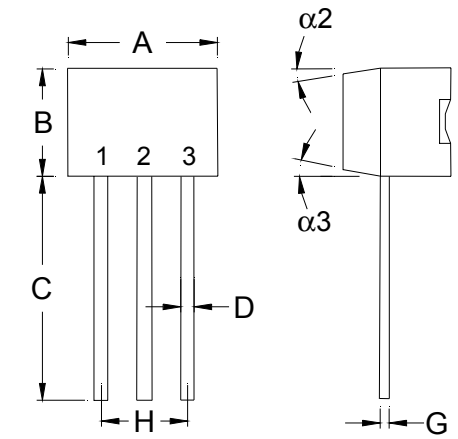
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

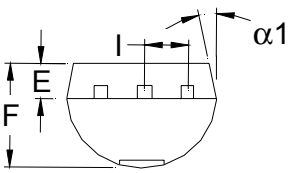
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

TO-92 Dimension





Marking:

Product Name

A94
□□

Date Code: Year+Month

Year: 0→2010, 1→2011

Month: 1→1, 2→2, ・・・,
9→9, A→10, B→11, C→12

Style: Pin 1.Emitter 2.Base 3.Collector

3-Lead TO-92 Plastic Package
CYStek Package Code: A3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	α1	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	α2	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	α3	-	*2°	-	*2°

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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