

65C23 TRI-PORT INTERFACE

CONCEPT...

The 65C23 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It has three dedicated 8-bit I/O ports which provide 24 individually programmable I/O lines.

FEATURES:

- 24 individually programmable I/O lines
- Completely static operation
- Two TTL Drive Capability
- 6 directly addressable registers
- 1 MHz operation

65C23 Addressing

65C23 REGISTERS (Direct Addressing)

*000	R0	PRA — Port Register A
001	R1	PRB — Port Register B
010	R2	PRC — Port Register C
011	R3	DDRA — Data Direction Register A
100	R4	DDRB — Data Direction Register B
101	R5	DDRC — Data Direction Register C
110	}	Illegal States
111		Illegal States

*NOTE: RS2, RS1, RS0 respectively

ORDER NUMBER:

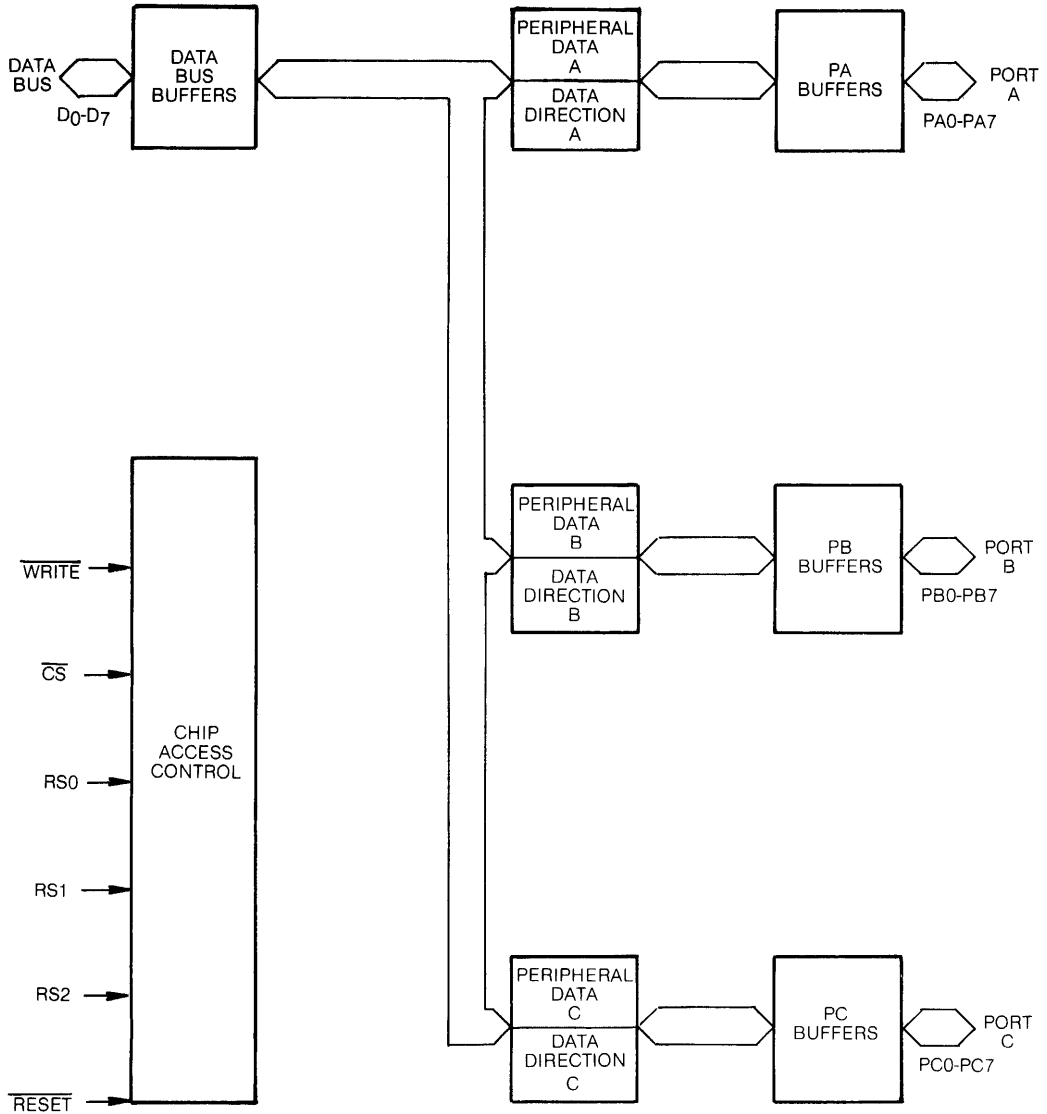
MXS 65C23

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

65C23 PIN CONFIGURATION

V _{SS}	1	40	DB7
PA0	2	39	DB6
PA1	3	38	DB5
PA2	4	37	DB4
PA3	5	36	DB3
PA4	6	35	DB2
PA5	7	34	DB1
PA6	8	33	DB0
PA7	9	32	PC7
PB0	10	31	PC6
PB1	11	30	PC5
PB2	12	29	PC4
PB3	13	28	PC3
PB4	14	27	PC2
PB5	15	26	PC1
PB6	16	25	PC0
PB7	17	24	RS0
CS	18	23	RS1
WRITE	19	22	RS2
V _{DD}	20	21	RST

65C23 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

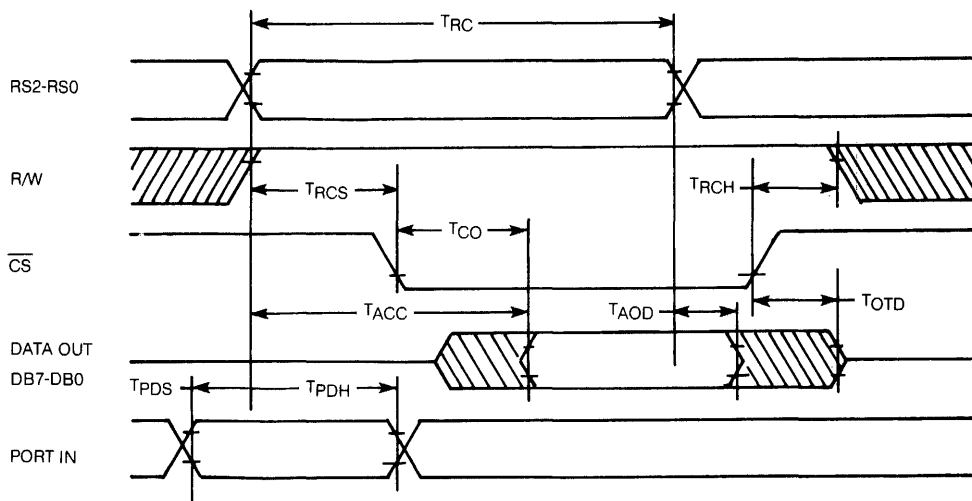
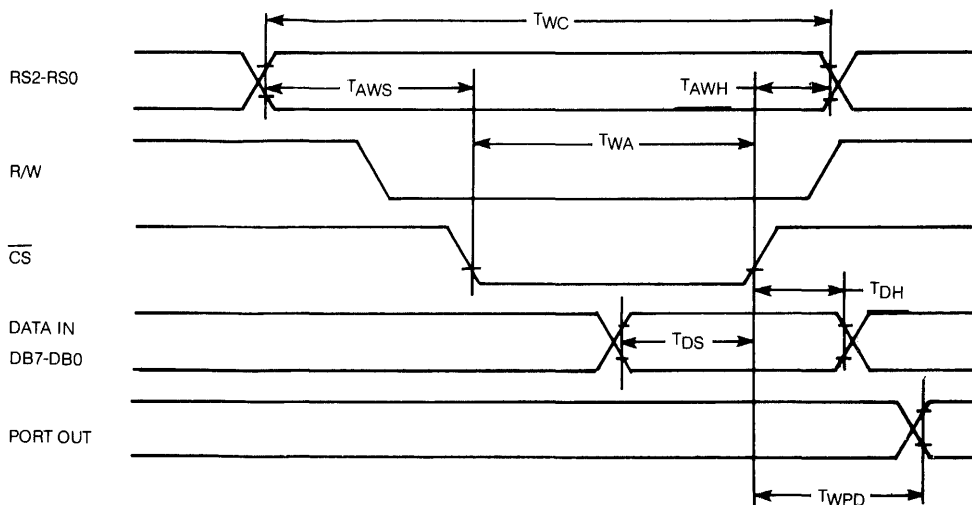
RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	-0.3 to +7.0	V _{dc}
INPUT VOLTAGE	V_{in}	-0.3 to +7.0	V _{dc}
OPERATING TEMPERATURE RANGE	T_A	0 to +70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = 0\text{V}$, $T_A = 0^\circ \text{ to } 70^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	V _{dc}
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	+0.8	V _{dc}
Input Leakage Current $V_{in} = 0 \text{ to } 5.0 \text{ Vdc}$ WRITE $\overline{RST}$, CS, $\overline{RS_0}$, $\overline{RS_1}$	I_{IN}	0	± 1.0	± 2.5	μAdc
Three-State (Off State) Input Current $(V_{in} = 0.4 \text{ to } 2.4 \text{ Vdc}, V_{CC} = \text{max})$ D0-D7, PA0-PA7, PB0-PB7, PC0-PC7	I_{TSI}	0	± 2.0	± 10	μAdc
Output High Voltage ($V_{CC} = \text{min}$, Load = 200 μAdc)	V_{OH}	2.4	3.5	V_{CC}	V _{dc}
Output Low Voltage ($V_{CC} = \text{min}$, Load = 3.2 mAdc)	V_{OL}	V_{SS}	0.2	+0.4	V _{dc}
Output High Current (Sourcing) ($V_{OH} = 2.4 \text{ Vdc}$)	I_{OH}	-200	-1000	—	μAdc
Output Low Current (Sinking) ($V_{OL} = 0.4 \text{ Vdc}$)	I_{OL}	32	—	—	mAdc
Supply Current	I_{CC}	—	—	10	mA
Input Capacitance $(V_{in} = 0\text{V}, T_A = 25^\circ\text{C}, f = 1.0 \text{ MHz})$ D0-D7, PA0-PA7, PB0-PB7, PC0-PC7 WRITE $\overline{RST}$, $\overline{RS_0}$, $\overline{RS_2}$, CS	C_{in}	—	7	10	pF
Output Capacitance $(V_{in} = 0, T_A = 25^\circ\text{C}, f = 1.0 \text{ MHz})$	C_{out}	—	7	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE

WRITE CYCLE


Note: All timings referenced to V_{ILmax} , V_{IHmin} on inputs and V_{OLmax} , V_{OHmin} on outputs.

READ CYCLE

Symbol	Parameter	MIN	MAX	UNITS
T _{RC}	Read Cycle	450	—	nS
T _{ACC}	Access Time ¹	—	450	nS
T _{CO}	$\overline{CS}$ to Output Valid	—	270	nS
T _{RCS}	R/W high to $\overline{CS}$ Setup	0	—	nS
T _{RCH}	R/W high to $\overline{CS}$ Hold	0	—	nS
T _{OD}	$\overline{CS}$ to Output Off Delay	20	120	nS
T _{AOD}	Address to Output Delay	50	—	nS
T _{PDS}	Port Input Setup	120	—	nS
T _{PDH}	Port Input Hold	150	—	nS

Note 1: Access Time measured from later of $\overline{WRITE}$ high or RS stable.

WRITE CYCLE

Symbol	Parameter	MIN	MAX	UNITS
T _{WC}	Write Cycle	450	—	nS
T _{WA}	Write Active Time ²	420	—	nS
T _{AWS}	Address to R/W low Setup	0	—	nS
T _{AWH}	Address to R/W low Hold	0	—	nS
T _{DS}	Data bus in Setup	150	—	nS
T _{DH}	Data bus in Hold	0	—	nS
T _{WPD}	Write active to Port out Delay	—	1000	nS

Note 2: T_{WA} is the time while both $\overline{CS}$ and R/W are low.

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