# MPQ86940



40A Intelli-Phase<sup>™</sup> Solution in TQFN-21 (4mmx5mm) Package, AEC-Q100 Qualified

### DESCRIPTION

The MPQ86940 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It can achieve up to 40A of continuous output current ( $I_{OUT}$ ) across a wide input voltage ( $V_{IN}$ ) range.

The integrated MOSFETs and drivers achieve high efficiency through an optimized dead time (DT) and reduced parasitic inductance.

The MPQ86940 is compatible with tri-state output controllers. It also includes generalpurpose current sensing and temperature sensing.

The MPQ86940 is ideal for autonomous driving applications where efficiency and compact size are at a premium. It is available in a TQFN-21 (4mmx5mm) package.

### FEATURES

- Wide Operating Input Voltage (VIN) Range
- 40A Output Current (I<sub>OUT</sub>)
- Accepts Tri-State Pulse-Width Modulation (PWM) Signal
- Built-In Bootstrap (BST) Switch
- Quiet Switcher<sup>™</sup> Technology
- Accu-Sense<sup>™</sup> Current Sense
- Temperature Sense
- Current-Limit Protection and Fault Flag
- Over-Temperature Protection (OTP) and Fault Flag
- Compatible with Multi-Phase Operation
- Available in a TQFN-21 (4mmx5mm) Package
- Available in AEC-Q100 Grade 1

#### APPLICATIONS

- Autonomous Driving System-on-Chips (SoCs)
- Infotainment Systems

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#### **ORDERING INFORMATION**

Part Number*	Package	Top Marking	MSL Rating
MPQ86940GVTE-AEC1	TQFN-21 (4mmx5mm)	See Below	1

\* For Tape & Reel, add suffix -Z (e.g. MPQ86940GVTE-AEC1-Z).

### **TOP MARKING**

## MPSYWW M86940 LLLLLL

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MPS: MPS prefix Y: Year code WW: Week code M86940: Part number LLLLLL: Lot number E: Wettable flank

#### **PACKAGE REFERENCE**



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### **PIN FUNCTIONS**

Pin #	Name	Description	
1, 14	VIN	<b>Input supply voltage.</b> Place input ceramic capacitors $(C_{IN})$ close to the device to support the switching current with minimal parasitic inductance.	
2, 3, 4	SW	Phase node.	
5	VDRV	<b>Driver voltage.</b> Connect the VDRV pin to the 3.3V supply. Decouple VDRV using a $1\mu$ F to $4.7\mu$ F ceramic capacitor.	
6, 7, 8, 9, 10, 11, 12, 13	PGND	Power ground.	
15	EN	<b>Enable.</b> Pull the EN pin high to enable the device; pull EN low to disable the device and force SW into a high-impedance (Hi-Z) state.	
16	IOUT	<b>Current-sense output.</b> Connect an external resistor to the IOUT pin to adjust the IOUT voltage ( $V_{IOUT}$ ), which is proportional to the inductor current ( $I_L$ ).	
17	TOUT/FLT	Single-pin temperature sense and fault reporting. If a fault occurs, the TOUT/FLT pin is pulled up to the VDD voltage ( $V_{DD}$ ).	
18	PWM	<b>Pulse-width modulation (PWM) input.</b> Float the PWM pin or drive PWM to a middle-state to force SW into a high-impedance (Hi-Z) state.	
19	VDD	<b>3.3V power supply for the internal logic.</b> Connect the VDD pin to a 3.3V external power supply via a $2.2\Omega$ resistor. Decouple VDD with a 1µF capacitor connected to AGND. Connect AGND and PGND at the VDD capacitor.	
20	AGND	Analog ground.	
21	BST	<b>Bootstrap.</b> The BST pin requires a $0.1\mu$ F to $1\mu$ F capacitor to drive the power MOSFET's gate above the supply voltage. Connect this capacitor between the SW and BST pins to form a floating supply across the power MOSFET driver.	

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