MPQ4483

3A, 36V, Step-Down Converter with DCP and CDP Mode and Ground Short to Battery Protection for Automotive, AEC-Q100 Qualified

DESCRIPTION

The MPQ4483 is a high-frequency, synchronous rectified, step-down, switch-mode converter. It achieves 3A output current over a wide input supply range with excellent load and line regulation. The MPQ4483 has synchronous mode operation for higher efficiency over the output load range.

The MPQ4483 has a constant current (CC) limit function for the output with two adjustable CC limit thresholds. The MPQ4483 also supports BC 1.2 DCP mode and CDP mode.

Fault condition protection includes hiccup current limiting, OVP, ground short to battery protection, and thermal shutdown (TSD).

The MPQ4483 requires a minimum number of readily available, standard, external components. The MPQ4483 is available in a QFN25 (4mmx5mm) package.

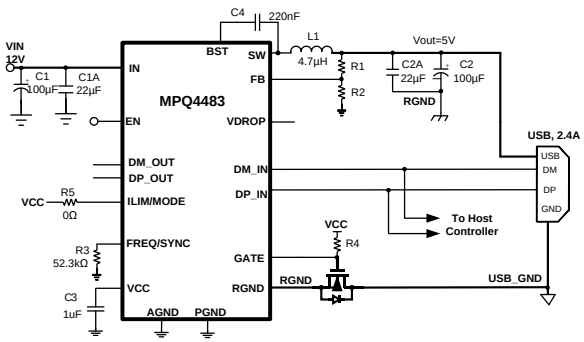
FEATURES

- Supports BC1.2 CDP Mode
- Supports BC1.2 DCP Mode, Apple Divider Mode, 1.2V/1.2V Mode
- Supports Bidirectional USB2.0 High-Speed Data Switch
- 4.2V to 36V Operating Input Voltage Range
- 3A Output Current
- Internal Auto EN Pull-Up
- 25mΩ/20mΩ Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- Integrated 4mΩ Ground Sensing Resistor
- Frequency Adjustable (200kHz to 2.2MHz)
- Constant Current Limit, 2 Level Adjustable
- Forced PWM Mode
- Frequency SYNC from 200kHz to 2.2MHz
- Spread Spectrum Option with 450kHz fs
- EN Shutdown Discharge
- Low Dropout Mode
- Battery Short to Ground Protect Driver
- Output Over-Voltage Protection
- Adjustable Line Drop Compensation
- Support 1V to 20V Output Adjustable
- QFN25 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

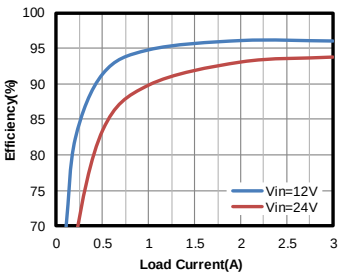
- USB Charging Ports
- Automotive Infotainment System
- Automotive USB Hub

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT}=5V, F_S=450kHz, L=4.7µH, DCR=7mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ4483GV-AEC1	QFN-25 (4mmx5mm)	*See Below*
MPQ4483GV-FD-AEC1	QFN-25 (4mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ4483GV-AEC1–Z, MPQ4483GV-FD-AEC1–Z);

DEVICE COMPARISON INFORMATION

Part Number	Frequency Spread Spectrum
MPQ4483GV-AEC1	No
MPQ4483GV-FD-AEC1	Yes

TOP MARKING

MPSYWW

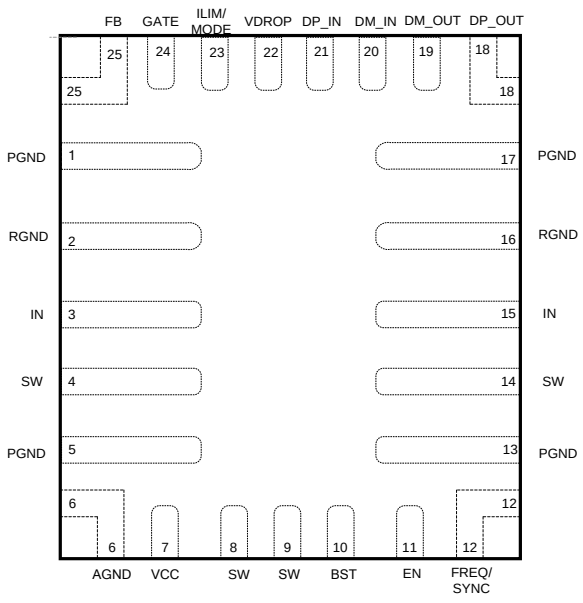
MP4483

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP4483: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-25 (4mmx5mm)

PIN FUNCTIONS

QFN 4x5 Pin #	Name	Description
1, 5, 13, 17	PGND	**Power ground.** Reference ground of the regulated output voltage. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias. **All PGND pins must be connected together.**
2, 16	RGND	**Remote power ground.** There is an internal sense resistor from RGND to PGND (pin 1, 17).
3,15	IN	**Supply voltage.** The MPQ4483 operates from a 4.2V to 36V input voltage. C_{IN} prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible. IN is the drain of the internal power device. Also, IN provides the power supply for the entire chip.
4, 8, 9, 14	SW	**Switch output.** SW pins must be connected together by a PCB trace. Use a wide PCB trace to make the connection.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 5V LDO regulator output.** Decouple with a 1µF capacitor.
10	BST	**Bootstrap.** A 0.22µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
11	EN	**On/off control input.** Internal auto pull-up with 7µA current source. EN has two stage thresholds: when EN is higher than ~1V, the VCC and bias circuitry will be enabled; when EN is higher than 2V, the buck switcher starts to work.
12	FREQ/SYNC	**Switching frequency program input.** Connect a resistor from FREQ to GND to set the switching frequency. This pin also serves as a frequency-synchronous clock input.
18	DP_OUT	**D+ data output to USB host.**
19	DM_OUT	**D- data output to USB host.**
20	DM_IN	**D- data line to USB connector.** Input/output used for handshaking with portable devices.
21	DP_IN	**D+ data line to USB connector.** Input/output used for handshaking with portable devices.
22	VDROP	**Line drop amplitude selection**. 3 levels can be programmable by pulling VDROP to GND/Float/VCC.
23	ILIM/MODE	**Multifunction pin.** ILIM/MODE can set the current limit threshold and USB charging mode (CDP or DCP mode): GND: 2.75A current limit/DCP Mode Float: 3.75A current limit/DCP Mode High: 2.75A current limit/CDP Mode
24	GATE	Ga**te drive for external low side N-channel power MOSFET.** Open drain structure. GATE is pulled low to turn off the power MOSFET when the secondary current limit is triggered.
25	FB	**Feedback.** Connect to the tap of an external resistor divider from the output to GND to set the output voltage.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN})..... 40V
V_{SW}..... –0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST}..... V_{SW} + 5.5V
V_{EN}.....-0.3V to +10V(2)
All Other Pins.....–0.3V to +5.5V
Continuous Power Dissipation (T_A = +25°C) (3) (5)
QFN-25 (4mm x 5mm)..... 4.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (4)

Operation Input Voltage Range .....4.2V to 36V
Output Voltage Range .....1V to V_{IN}*D_{MAX}
Output Current 3A
Operating Junction Temp…….. -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-25 (4mmx5mm)			
EVQ4483-V-00A(5)	27	7	°C/W
JESD51-7(6)	44	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS Max rating, please refer to page12, EN control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EVQ4483-V-00A, 4-layer PCB, 50mmx50mm
6) Measured on JESD51-7, 4-layer PCB. The value of θJA given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C(7), Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN}=0V		15	25	μA
Supply current (quiescent)	I_Q	No Switching		1	2	mA
EN rising threshold	V_{EN_Rising}		1.96	2.06	2.16	V
EN hysteresis	$V_{EN\_Falling}$			200		mV
EN pull-up current	I_{EN}	V_{EN} =3V	3	7	11	μA
Thermal shutdown(8)	T_{STD}			165		°C
Thermal hysteresis(8)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}	I_{CC}=0mA	4.65	5.05	5.45	V
VCC load regulation	V_{CC_LOG}	I_{CC}=50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		3.7	3.95	4.2	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			500		mV
HS switch on resistance	R_{DSON_HS}			25	40	mΩ
LS switch on resistance	R_{DSON_LS}			20	40	mΩ
Feedback voltage	V_{FB}		0.985	1	1.015	V
Sync frequency range	f_{SYNC}		0.2		2.2	MHz
Low-side current limit	I_{LS_LIMIT}			-2		A
Switch leakage	SW_{LKG}	V_{EN}=0V, V_{SW}=36V, T_J=+25°C			1	μA
		V_{EN}=0V, V_{SW}=36V, T_J=-40°C to +125°C			5	
High-side current limit	I_{LIMIT1}		9	17		A
Output current limit	I_{LIMIT2}	ILIM/MODE = Float (For 3A continuous Iout application), T_J=+25°C	3.45	3.75	4.25	A
		ILIM/MODE = GND or VCC (For 2.4A continuous Iout application),T_J=+25°C	2.45	2.75	3.05	
Oscillator frequency	f_{SW1}	R_{FREQ}=97.6kΩ	170	235	300	kHz
	f_{SW2}	R_{FREQ}=9.53kΩ	1800	2200	2600	
	f_{SW3}	R_{FREQ} = 52.3kΩ	330	430	530	
Frequency spread spectrum(8) (MPQ4483GV-FD-AEC1)	F_{SS}	R_{FREQ} = Float, based on 430kHz.		10		%
Maximum on time	T_{ON_MAX}	Dropout mode, Max Duty Cycle D_{MAX}= T_{ON_MAX}/(T_{ON_MAX}+ T_{OFF_MIN})	6	10		μs
Minimum off time	T_{OFF_MIN}			120		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C(7), Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum on time(8)	T_{ON_MIN}			130		ns
Soft-start time	tss	10-90% Vout	0.4	1.1	1.8	ms
ILIM/MODE logic low voltage	V_{LOW}	GND: 2.75A current limit/DCP Mode			50	mV
ILIM/MODE logic high voltage	V_{HIGH}	High: 2.75A current limit/CDP Mode	VCC-0.2			V
Line drop compensate gain (From I_{RTN} to I_{FB})	Gain1	VDROP pin=GND, T_J=+25°C		0.7		µA/A
	Gain2	VDROP pin=Float, T_J=+25°C		3.3		µA/A
	Gain3	VDROP pin=VCC, T_J=+25°C		6.6		µA/A
OVP						
OVP rising threshold	V_{OVP1_RISE}		110%	115%	120%	V_{REF}
OVP falling threshold	V_{OVP_FALL}			105%		V_{REF}
OVP delay(8)	T_{OVPDEL}			2		µs
External RGND Current Limit						
RGND to PGND resistor	R_{SENSE}			4	12	mΩ
Second current limit threshold	V_{SENSE_TH}		8	12	16	A
GATE pull-low resistance	R_{GATE_L}		30	100	170	Ω
Second current limit off time	$t_{EXT\_CUR\_RES}$			2		s
DCP MODE (ILIM/MODE Pin=GND)						
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_Short}	V_{DP}=0.8V, I_{DM}=1mA, T_J=+25°C		85	155	Ω
		V_{DP}=0.8V, I_{DM}=1mA, T_J=-40°C to +125°C		85	160	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_Divider}$		2.55	2.7	2.85	V
DP/DM output impedance	$R_{DP/DM\_Divider}$	T_J=+25°C	14	22	32	kΩ
		T_J=-40°C to +125°C	12	22	36	
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT}=5V, T_J=+25°C	1.12	1.2	1.28	V
		V_{OUT}=5V, T_J=-40°C to +125°C	1.1	1.2	1.3	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J=+25°C	70	105	150	kΩ
		T_J=-40°C to +125°C	60	105	170	
CDP MODE (ILIM/MODE Pin=5V)						
DM CDP output voltage	V_{DM_SRC}	V_{DP}=0.6V	0.5	0.6	0.7	V
DP rising lower window threshold for V_{DM_SRC} EN	V_{DAT_REF}		0.25	0.35	0.4	V
DP rising lower window threshold hysteresis	$V_{DAT\_REF\_HYS}$			50		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C[7], Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DP rising upper window threshold for V_{DM_SRC}	V_{LGC_SRC}		0.8		2	V
DP rising upper window threshold hysteresis	$V_{LGC\_SRC\_HYS}$			100		mV
V_{DM_SRC} on/off deglitch time	$V_{DM\_SRC\_Degh}$			5	20	ms
RDP_Down, RDM_Down	R_{DP/DM_Down}		14.25	19.5	24.8	kΩ
DP/DM on resistance	$R_{ON\_DP/DM}$			2	4	Ω
DP_IN and DP_OUT to GND Capacitance [8]	C_{DP}	Same for DM Switch		5.3		pF
3dB bandwidth of analog data SW[8]			500			MHz

Notes:

7) All min/max parameters are tested at T_J=25°C. Limits over temperature are guaranteed by design, characterization and correlation.

8) Guaranteed by engineering sample characterization

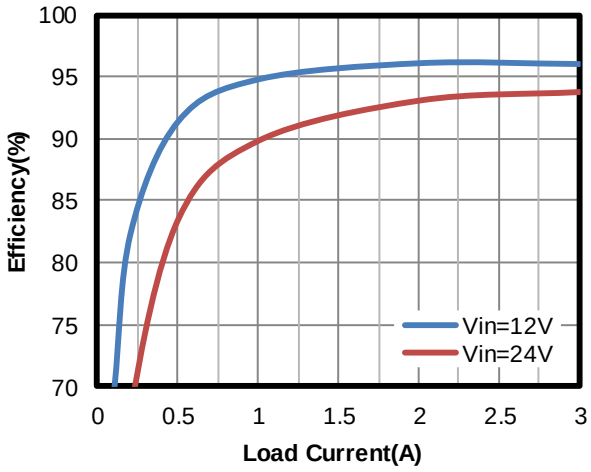
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L =4.7µH, Fs=450kHz, T_A = 25°C, unless otherwise noted.

Note: All waveforms are tested based on bypassing the external MOSFET, except short battery to ground.

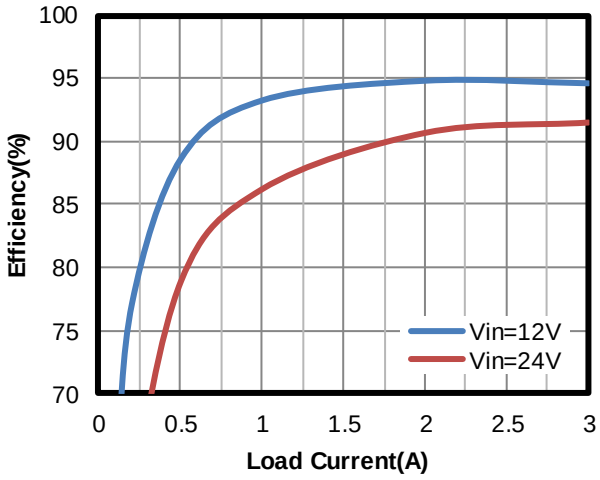
Efficiency vs. Load Current

V_{OUT}=5V



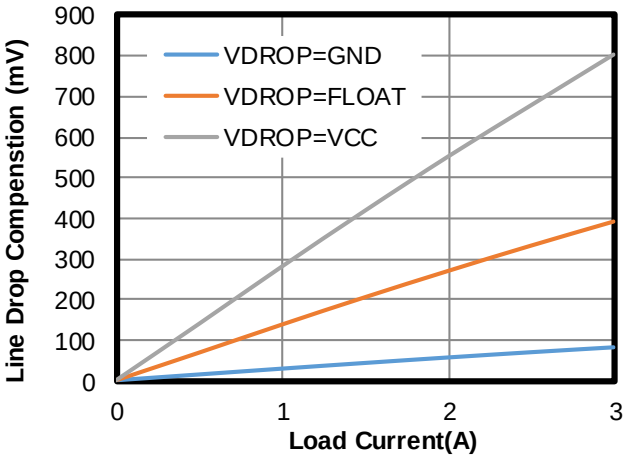
Efficiency vs. Load Current

V_{OUT}=3.3V



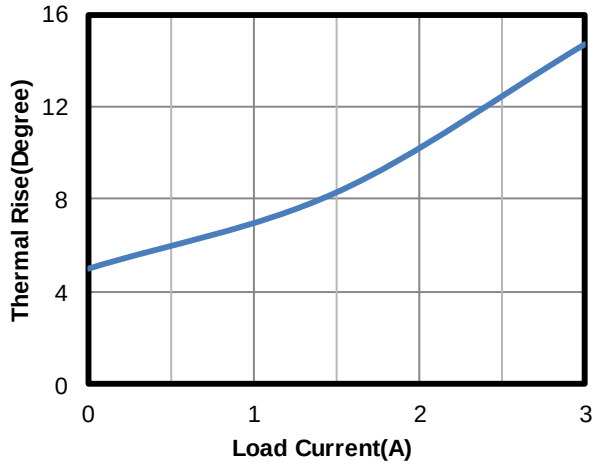
Line Drop Compensation vs. Load Current

R1=40.2KΩ



Thermal Rise vs. Temperature

4 Layers, size: 5cmx5cm

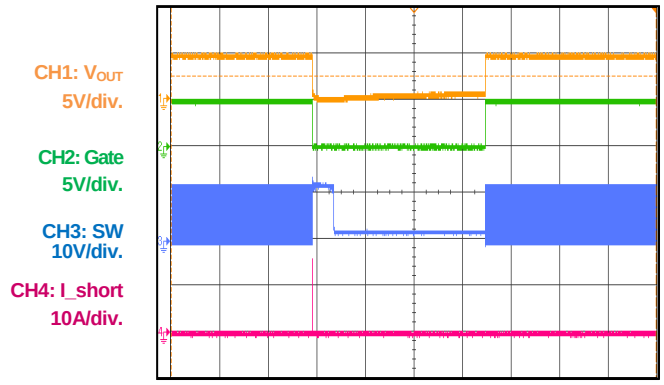


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L =4.7µH, Fs=450kHz, T_A = 25°C, unless otherwise noted.

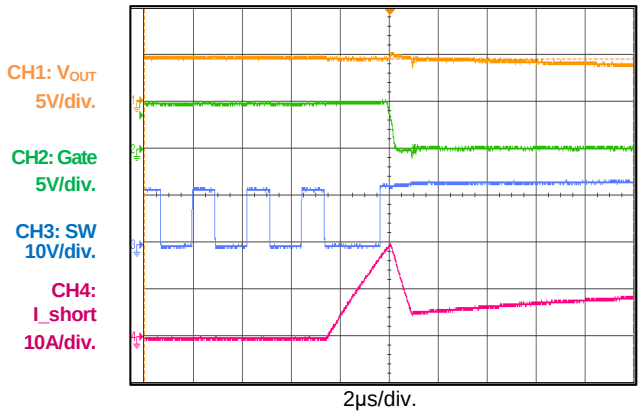
Note: All waveforms are tested based on bypassing the external MOSFET, except short battery to ground.

Battery Short to USB_GND



500ms/div.

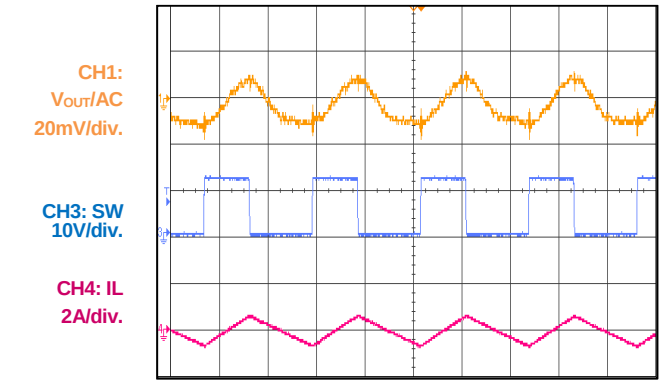
Battery Short to USB_GND ZOOM IN



2µs/div.

Output Ripple

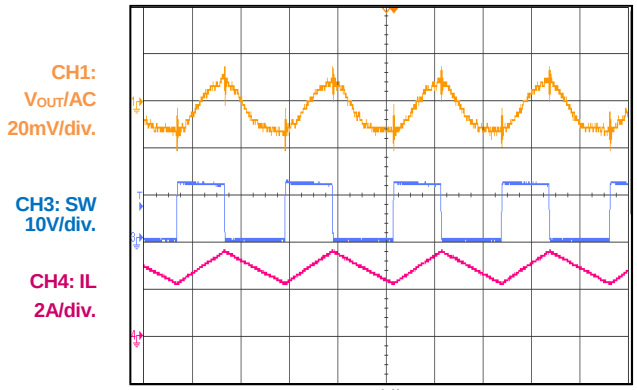
USB_I_{OUT}=0A



1µs/div.

Output Ripple

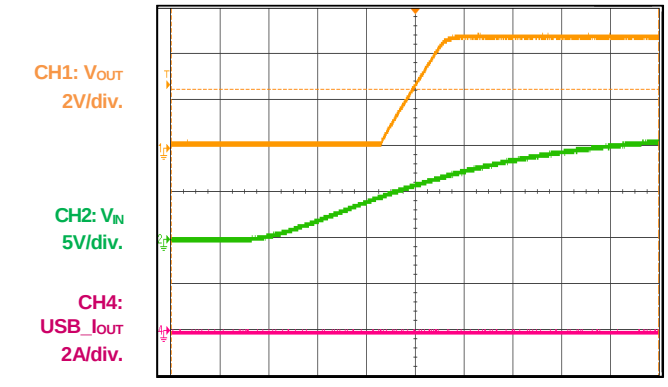
USB_I_{OUT}=3A



1µs/div.

Power Start-Up

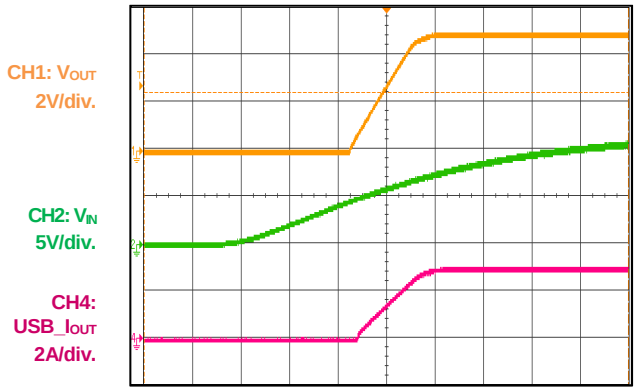
USB_I_{OUT}=0A



1ms/div.

Power Start-Up

USB_I_{OUT}=3A



1ms/div.

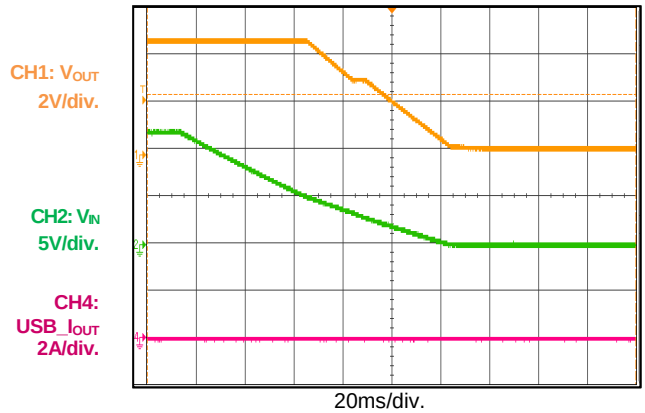
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L =4.7µH, Fs=450kHz, T_A = 25°C, unless otherwise noted.

Note: All waveforms are tested based on bypassing the external MOSFET, except short battery to ground.

Power Shutdown

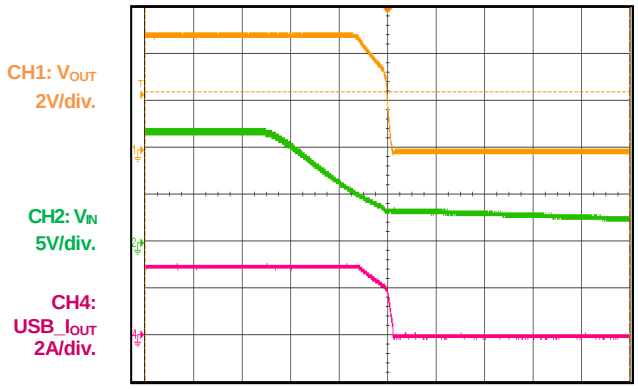
USB_I_{OUT}=0A



20ms/div.

Power Shutdown

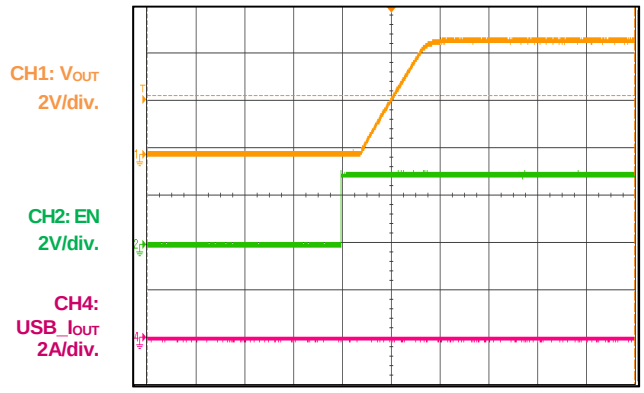
USB_I_{OUT}=3A



2ms/div.

EN ON

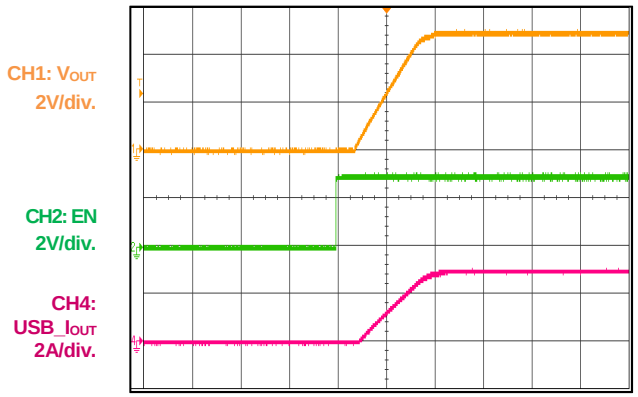
USB_I_{OUT}=0A



1ms/div.

EN ON

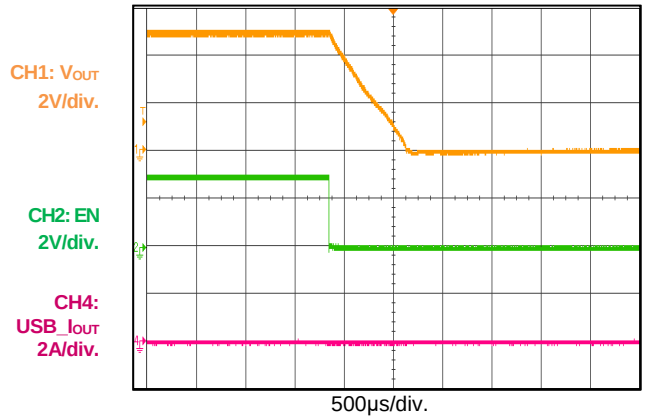
USB_I_{OUT}=3A



1ms/div.

EN OFF

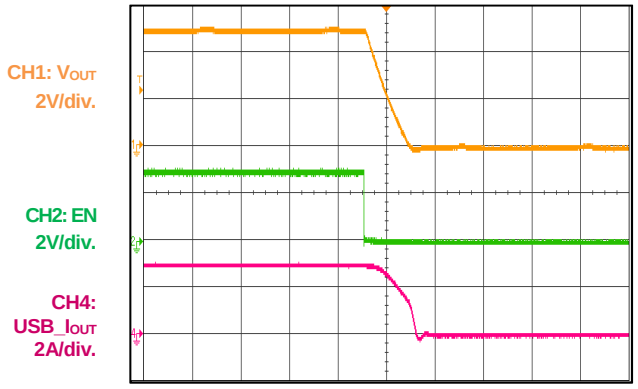
USB_I_{OUT}=0A



500µs/div.

EN OFF

USB_I_{OUT}=3A



200µs/div.

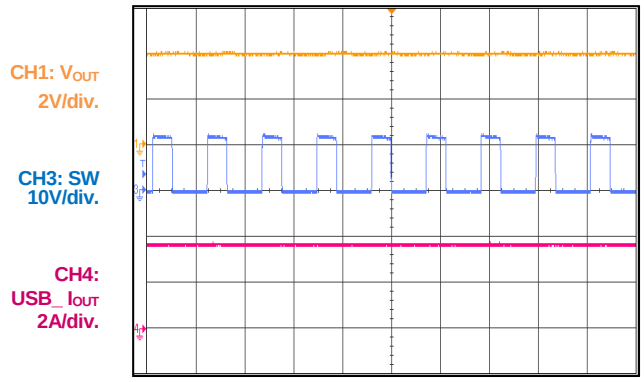
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L =4.7µH, Fs=450kHz, T_A = 25°C, unless otherwise noted.

Note: All waveforms are tested based on bypassing the external MOSFET, except short battery to ground.

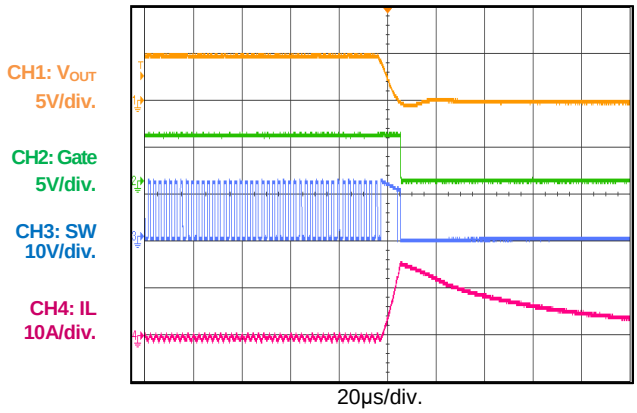
Constant Current Limit Mode

ILIM/MODE=FLOAT, CV to 4Vout with E-load



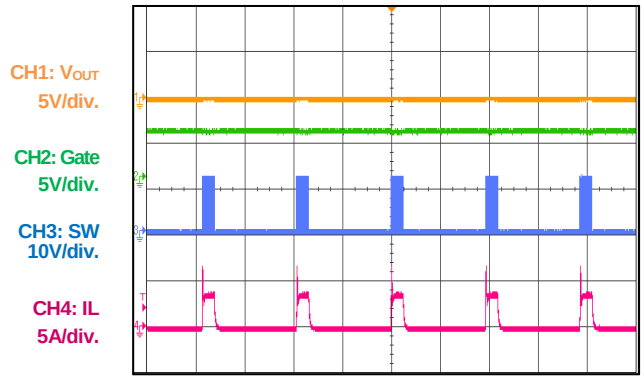
2µs/div.

Vout Short to USB_GND Entry



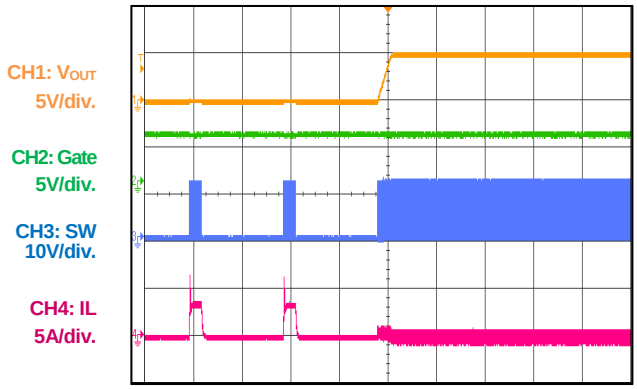
20µs/div.

Vout Short to USB_GND Steady State



5ms/div.

Vout Short to USB_GND Entry



5ms/div.

BLOCK DIAGRAM

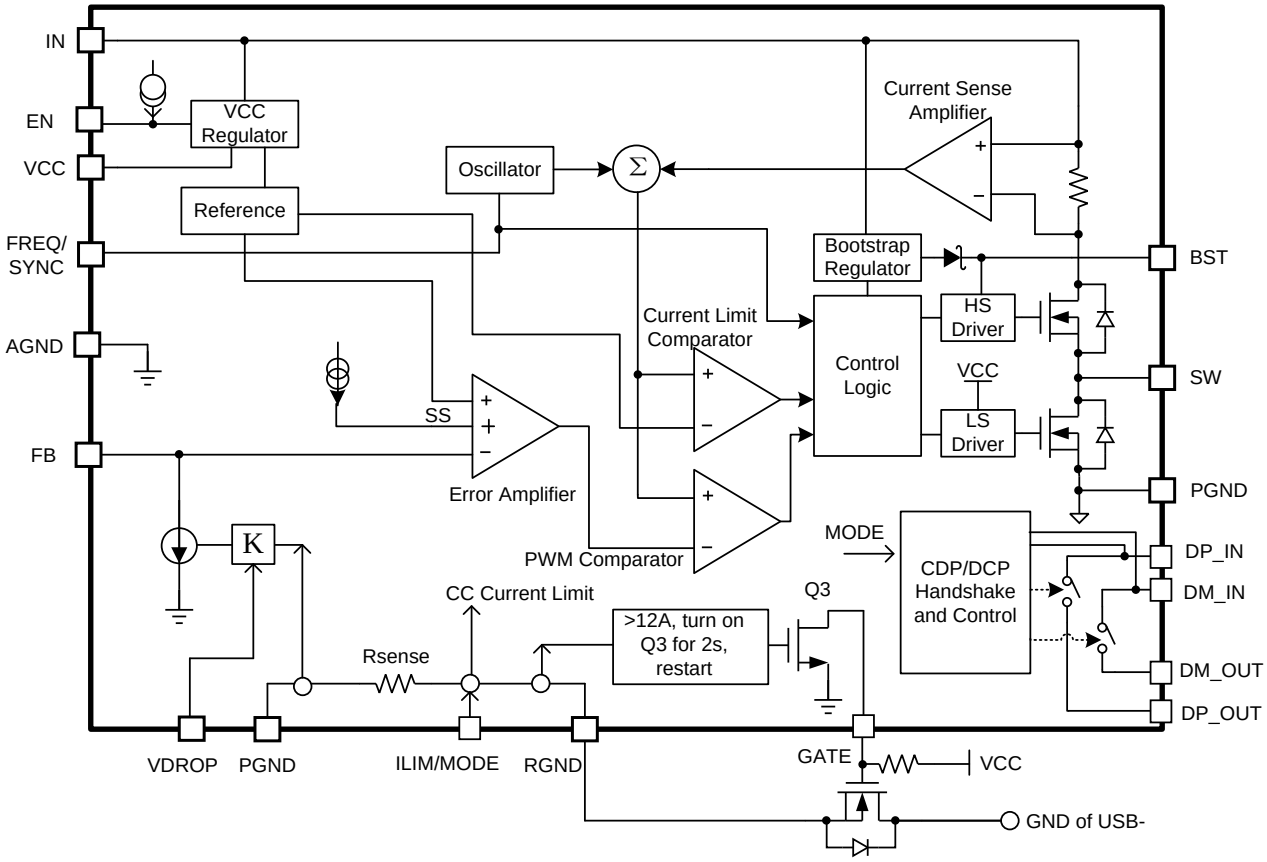


Figure 1: Functional Block Diagram

OPERATION

The MPQ4483 integrates a monolithic synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a compact solution to achieve 3A of continuous output current over a wide input supply range with excellent load and line regulation.

The MPQ4483 operates in a fixed frequency, peak-current–mode control to regulate the output voltage. The internal clock initiates the PWM cycle, which turns on the integrated high-side power MOSFET. The high-side MOSFET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle begins.

Low Dropout Operation

The operation frequency will auto decrease when the input voltage is close to the output voltage. This can achieve a low dropout voltage.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal 1V reference (REF) and outputs a COMP voltage. This COMP voltage controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5V, the output of the regulator is in full regulation. If the V_{IN} is less than 5V, the output decreases with the V_{IN}. VCC requires an external 1μF ceramic decoupling capacitor.

Enable Control (EN)

The MPQ4483 has an enable control (EN). There is an internal 7μA pull-up current, which allows floating EN to auto start-up. Pull EN high, or float, to enable the IC; pull EN low to disable the IC.
EN is clamped internally using a 7.6V series Zener diode, and a 10V break-down voltage of the ESD cell (see Figure 2).

Connecting EN through a pull-up resistor to V_{IN} can enhance the EN pull-up current ability. It requires limiting the EN voltage below 10V or limiting the EN input current to less than 500μA, if the EN pull up voltage is larger than 10V.

For example, if connecting EN to V_{IN}=36V, R_{PULLUP} ≥ (36V – 10V)/500μA = 52kΩ.

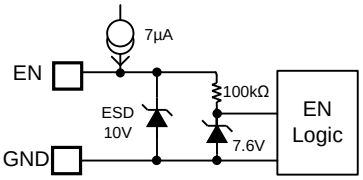


Figure 2: Zener diode between EN and GND

Setting the Frequency

Connect a resistor from FREQ to ground to set the switching frequency. The value of the frequency can be calculated approximately using equation (1):

$$FREQ(kHz) = \frac{1000}{0.04 \times RFREQ(K\Omega) + 0.1} \quad (1)$$

The frequency vs. R_{FREQ} is shown in Figure 3.

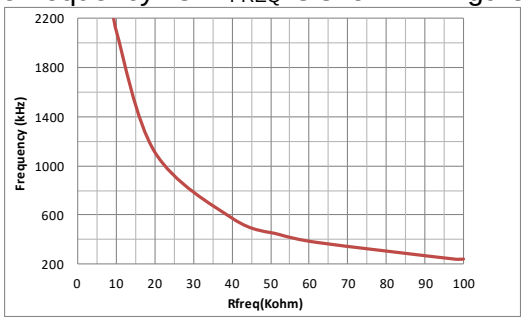


Figure 3: Switching Frequency vs R_{FREQ}

FREQ cannot be floating or tied to VCC or GND. FREQ should be connected to GND through a resistor.

In order to avoid tripping the minimum on-time limitation at a high frequency and high input voltage condition, the MPQ4483 adopts a frequency fold back mechanism when the switching frequency is higher than 1.2MHz, and the input voltage is larger than 15V. The MPQ4483 will decrease the switching frequency gradually until the frequency is decreased to half of the setting value.

Frequency Spread Spectrum

The MPQ4483-FD is the switching frequency spread spectrum version of MPQ4483. The

purpose of spread spectrum is to minimize the peak emissions at specific frequencies.

The MPQ4483-FD uses a 4KHz triangle wave (rising 125µs, falling 125µs) to modulate the internal oscillator. The frequency span of spread spectrum operation is ±10%. See Figure 4.

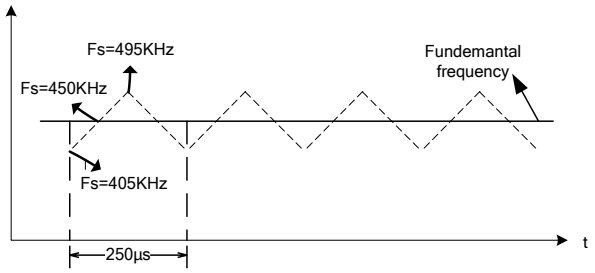


Figure 4: Frequency Spread Spectrum

The MPQ4483-FD frequency is only determined by internal trimming. It has no relationship with the FREQ pin status.

Frequency Synchronizing

The MPQ4483 can be synchronized to an external clock with a range from 200kHz to 2.2MHz through SYNC in series with a 10pF capacitor. The internal clock rising edge is synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 3.95V; its falling threshold is 3.45V.

Internal Soft-Start (SS)

Soft-start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is set to 1.1ms internally.

If the output of the MPQ4483 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

EN Shutdown Discharge

When EN is pulled low, the MPQ4483 will enter output discharge mode. Meanwhile, the internal soft-start capacitor starts to discharge. The discharge mode keeps working until the soft-start capacitor is discharged to very low. In this mode, the low-side switch remains on until the low-side current reaches -2A. The LS will turn on again after a clock cycle.

CC Mode Over-Current Protection

The MPQ4483 senses the ground current and uses this information to limit the output current, so it does not exceed a certain threshold. If the I_{OUT} current exceeds the set current limit threshold, the MPQ4483 will enter constant current limit mode (CC mode). In this mode the current amplitude is limited. As the load resistance reduces, the output voltage drops until the feedback voltage falls below the under voltage (UV) threshold—typically 30% below the reference. Once UV is triggered, the MPQ4483 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4483 exits hiccup mode once the over-current condition is removed.
Pull ILIM to GND, float, or VCC can set two different CC current limit threshold.
In addition to the ground current limit, the MPQ4483 also has high-side peak current limit.

Over-Voltage Protection (OVP)

The MPQ4483 monitors a resistor divided feedback voltage to detect over voltage. When the feedback voltage becomes higher than 115% of the target voltage, the controller will enter Dynamic Regulation Period. During this period, the LS is on until the LS current drops to -2A. This will discharge the output and try to keep it within the normal range. If OV still exists, the LS will turn on again after a fixed delay time. The part will exit this regulation period when the feedback voltage falls below 105% of the reference voltage.

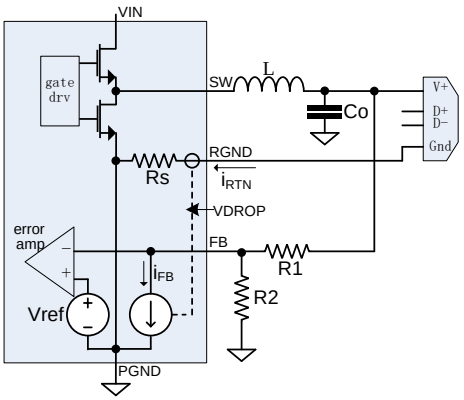
During OV protection, if the input voltage is boosted up to 40V, the MPQ4483 will stop the

OVP discharge function until Vin drops to 38V.

Output Line Drop Compensation

The MPQ4483 is capable of compensating an output voltage drop, such as high impedance caused by a long trace, to keep a fairly constant load-side voltage.

The MPQ4483 uses the sensed load current through the internal ground current sensing MOSFET to sink a current (I_{FB}) at FB. See equation (2):



$$i_{FB} = G \cdot i_{RTN} \quad (2)$$

Then

$$v_o = \left(\frac{R_1}{R_2} + 1\right) v_{ref} + R_1 G \cdot i_{RTN} \quad (3)$$

So the line drop compensation amplitude at certain output current conditions is equal to R1*G*Iout. Where G is Gain1, Gain2, or Gain3, which can be programmed by VDROP. For the three gain levels, refer to the EC table.

The R1 value can also be used to adjust the line drop compensation amplitude.

For example, at 3A output current, pull VDROP=0, choose 40.2k R1, and the line drop compensation is ~85mV.

Short RGND and PGND pins to disable the line drop compensation.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 5). The BST capacitor C4 voltage will be charged up quickly by VCC through M1. The 2.5μA input to the BST current source can charge the BST capacitor when the low-side switch doesn't turn-on.

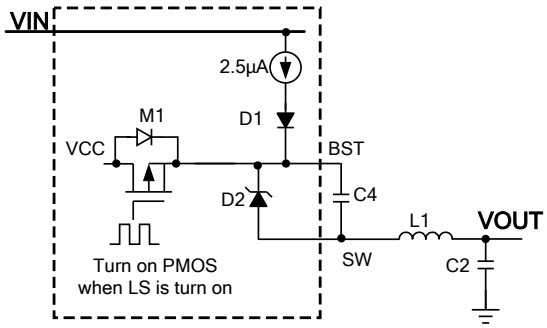


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, and thermal shutdown. In shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, it shuts down the entire chip. When the temperature falls below its lower threshold, 145°C typically, the chip is enabled.

Selectable Charging Mode (CDP/DCP)

ILIM/MODE can preset the charging mode, either DCP or CDP mode. The ILIM/MODE logic level should be set before power on. After power on, the user can't dynamically change the pin logic level. There are three logic levels: pull to ground, float this pin, and tie to VCC.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). R2 can be calculated with equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{1V} - 1} \quad (4)$$

The external resistor divider is shown in Figure 6.

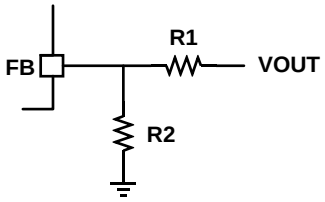


Figure 6: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT}(V)	R1(kΩ)	R2(kΩ)
3.3	40.2	17.5
5	40.2	10
9	40.2	4.99

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. Equation (5) derives the inductor value for most designs:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current at 30%~50% of the maximum load current. The maximum inductor peak current is calculated with equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Selecting the Buck Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For CLA application, a 100µF electrolytic capacitor and one 22µF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated with equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For

simplification, the output ripple can be approximated with equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

For polymer capacitor designs, the ESR zero frequency needs to be higher than that of the internal high frequency compensation pole. ESR<=1 / (2 x π x Cout x fp2).

A 100μF capacitor with an ESR less than 50mΩ (e.g.: polymer or tantalum capacitors) and one 22μF ceramic capacitor are recommended in applications (see Table 2).

Table 2: Recommended External Components

Switching frequency	Inductor	Buck output capacitor
450kHz	4.7μH	22μF ceramic cap + 100μF Polymer cap
2.2MHz	2.2μH	22μF ceramic cap + 100μF Polymer cap

PC Board Layout [9]

Efficient PCB layout is critical for standard operation and thermal dissipation. Refer to Figure 7 and follow the PCB layout guidelines below to ensure an effective layout design:

1) Place the high-current paths (GND, IN and SW) very close to the device with short, direct, and wide traces.

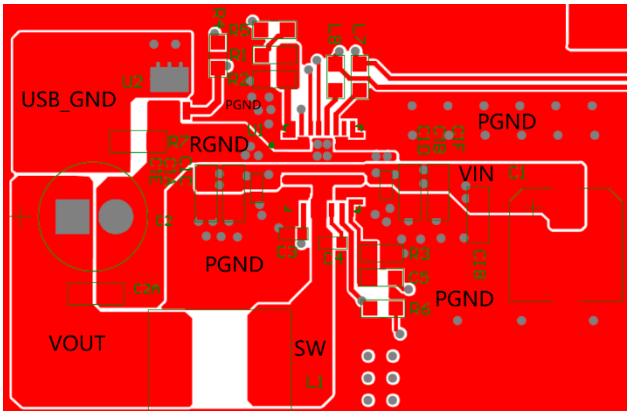
2) Place a large copper plane for RGND and PGND. Add multiple vias to improve thermal dissipation. Connect AGND to PGND.

3) Place a large copper plane for SW. Add multiple vias.

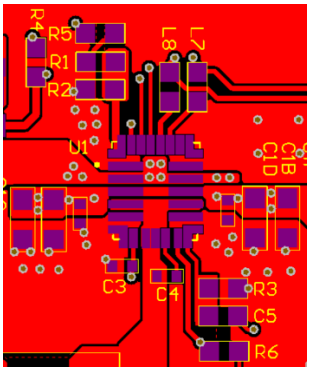
4) Place two ceramic input decoupling capacitors as close as possible to IN and PGND to improve EMI performance.

5) Place the VCC decoupling capacitor as close as possible to VCC.

Notes:
(9) The recommended layout is based on the typical application circuit on the next page.



Top Layer



Layout Zoom in

Figure 7: PC Board Layout

TYPICAL APPLICATION CIRCUITS

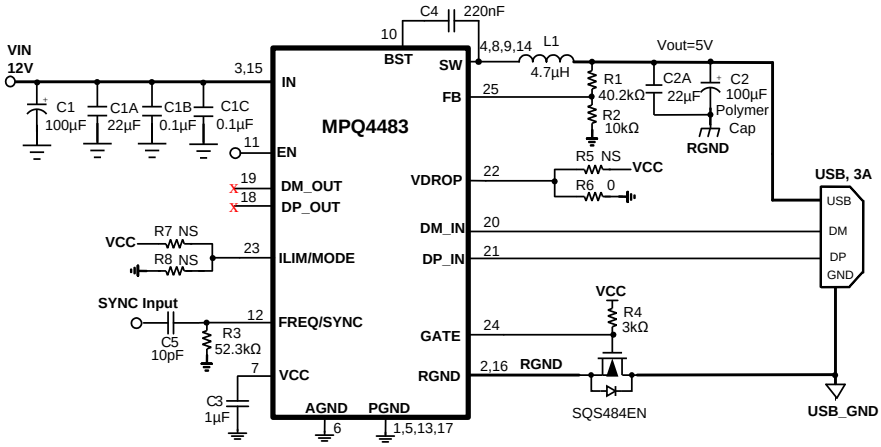


Figure 8: V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, f_S=450KHz, DCP Mode, with GND Short to Battery Protection

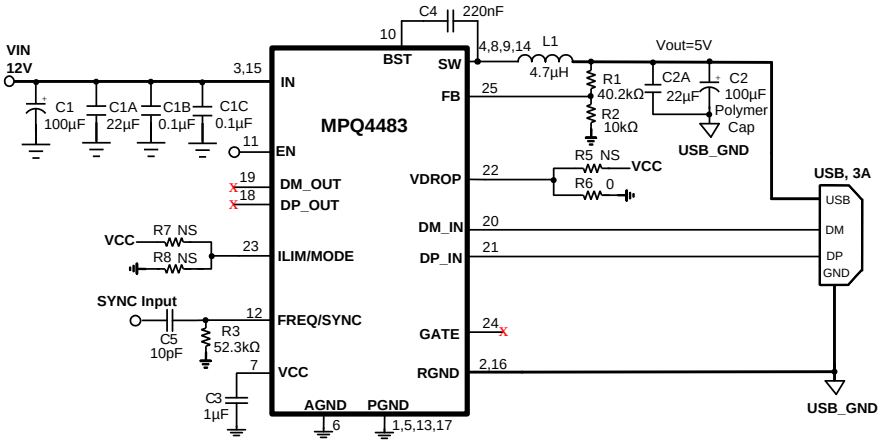


Figure 9: V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, DCP Mode, Without GND Short to Battery Protection

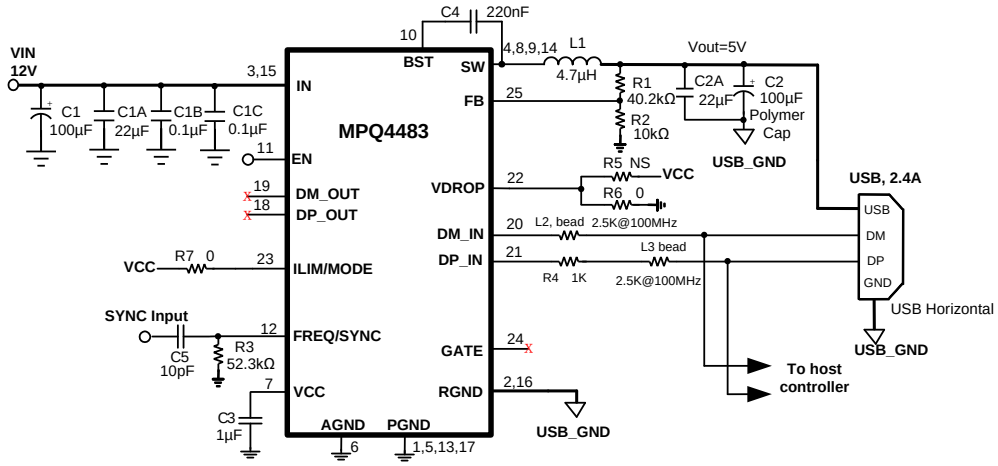
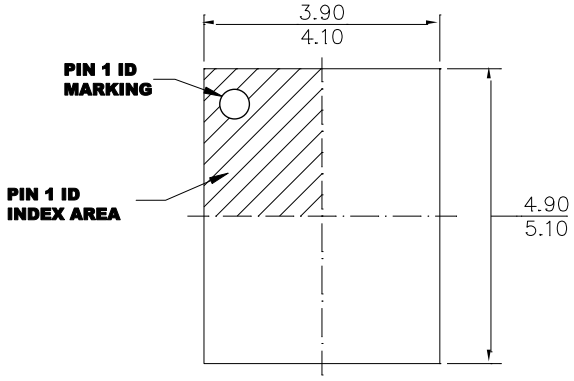


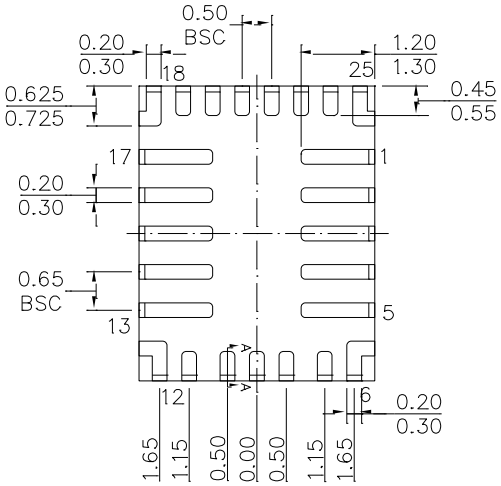
Figure 10: V_{IN}=12V, V_{OUT}=5V, I_{OUT}=2.4A, CDP Mode, without GND Short to Battery Protection, Bypass Internal DP_OUT, DM_OUT Switches.

PACKAGE INFORMATION

QFN-25 (4mm x 5mm)

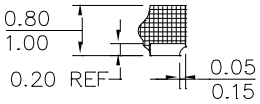


TOP VIEW

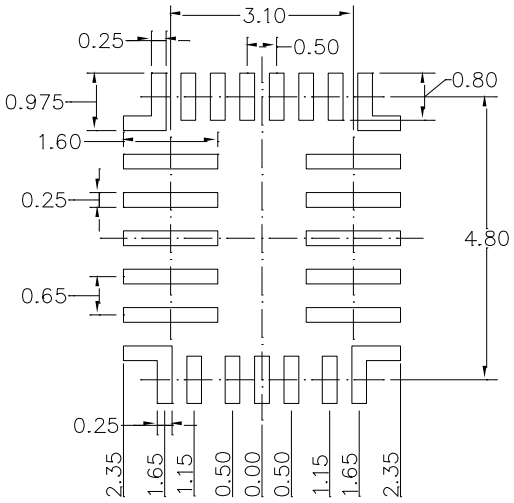


BOTTOM VIEW

SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) LAND PATTERNS OF PIN1~5 AND 13~17 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.