MPQ4323C

42V Load Dump Tolerant, 3A, Ultra-Compact, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4323C is a configurable-frequency (350kHz to 2.5MHz), synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs. The device provides 3A of highly efficient output current (I_{OUT}) with peak current mode control.

The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance accommodates a variety of step-down applications in automotive input environments. A 1µA shutdown mode quiescent current allows use in battery-powered applications.

An open-drain power good (PG) signal indicates that the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

A high duty cycle and low-dropout mode are provided for the automotive cold-crank condition.

The MPQ4323C is available in QFN-12 (2mmx3mm), QFN-12 (3mmx4mm), and QFN-14 (2.5mmx3.5mm) packages.

FEATURES

- Designed for Automotive Applications:
  - Survives 42V Load Dump
  - Supports 3.1V Cold Crank
  - 3A Continuous Output Current (I_{OUT})
  - Continuous Operation Up to 36V
  - Junction Temperature Operation from -40°C to +150°C
- Increases Battery Life:
  - 1µA Shutdown Supply Current
- High Performance for Improved Thermals:
  - Integrated 70mΩ High-Side and 50mΩ Low-Side MOSFETs
  - 65ns Minimum On Time and 50ns Minimum Off Time
- Optimized for EMC/EMI:
  - Frequency Spread Spectrum Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - 350kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good Output
  - Forced Continuous Conduction Mode (FCCM)
  - Low-Dropout Mode
  - Hiccup Over-Current Protection (OCP)
  - Available in QFN-12 (2mmx3mm), QFN12 (3mmx4mm), or QFN-14 (2.5mmx3.5mm) Packages with Wettable Flanks
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

TYPICAL APPLICATION

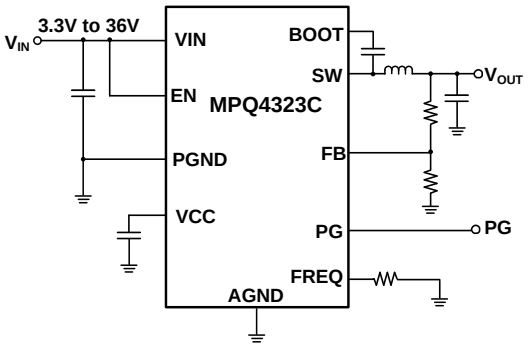


Figure 1: Typical Application (Adjustable Output)

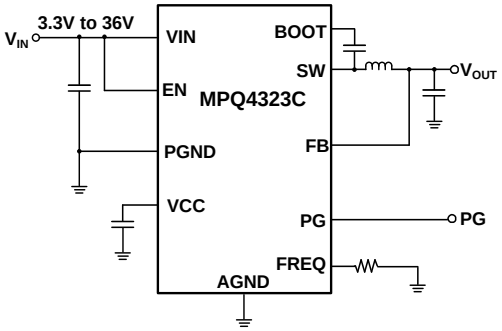
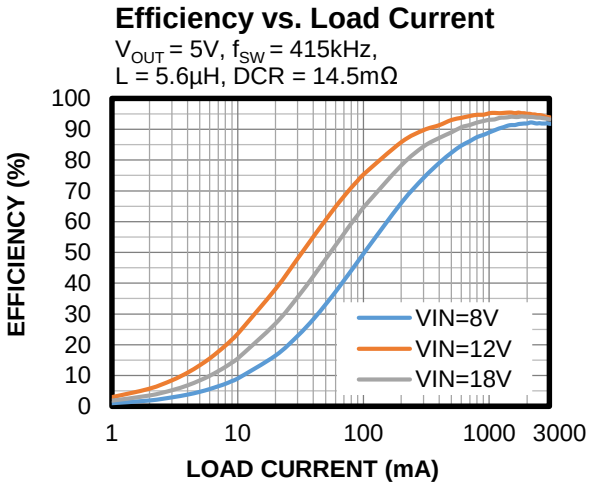


Figure 2: Typical Application (Fixed Output)



ORDERING INFORMATION

Part Number [1]*	Package	Top Marking	MSL Rating**
MPQ4323CGDE-AEC1***	QFN-12 (2mmx3mm)	*See Below*	1
MPQ4323CGRHE-AEC1***	QFN-14 (2.5mmx3.5mm)	*See Below*	1
MPQ4323CGLE-AEC1***	QFN-12 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4323CGDE-AEC1-Z).

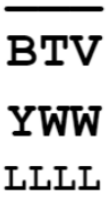
**Moisture Sensitivity Level Rating

***Wettable flank

Note:

1) Contact MPS for the details regarding fixed output versions.

TOP MARKING (MPQ4323CGDE-AEC1)



BTV: Production code
Y: Year code
WW: Week code
LLLL: Lot number

TOP MARKING (MPQ4323CGRHE-AEC1)

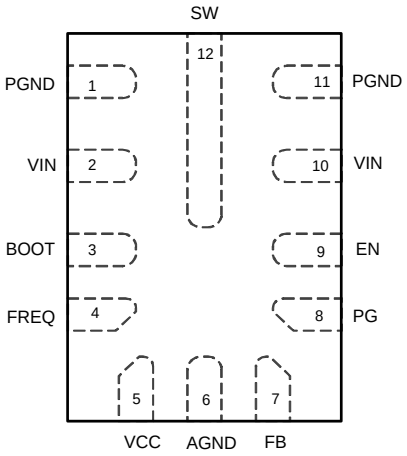
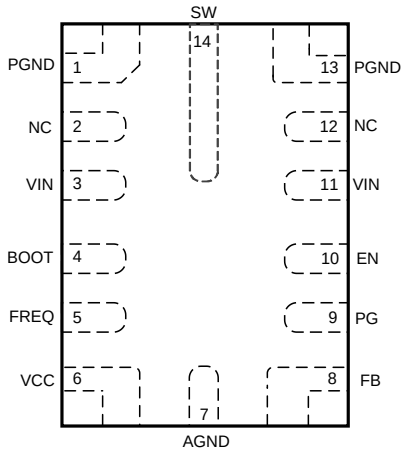
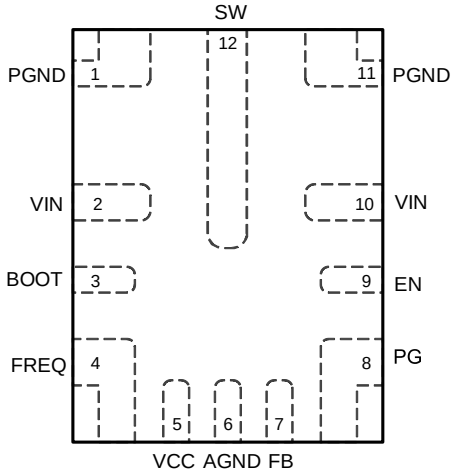
BTQ: Production code
Y: Year code
WW: Week code
LLL: Lot number

TOP MARKING (MPQ4323CGLE-AEC1)

MPYW
4323
CLLL
E

MP: MPS prefix
Y: Year code
W: Week code
4323C: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW	TOP VIEW	TOP VIEW
		
QFN-12 (2mmx3mm)	**QFN-14 (2.5mmx3.5mm)**	**QFN-12 (3mmx4mm)**

PIN FUNCTIONS

QFN-12 Pin #	QFN-14 Pin #	Name	Description
1, 11	1, 13	PGND	**Power ground.**
2, 10	3, 11	VIN	**Input supply.** VIN supplies power to all the internal control circuitry and the power switch connected to SW. The two VIN pins are connected internally. Connect a decoupling capacitor from VIN to ground (and close to each VIN pin) to minimize switching spikes.
3	4	BOOT	**Bootstrap.** BOOT is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BOOT and SW.
4	5	FREQ	**Switching frequency configuration.** Connect a resistor from FREQ pin to ground to set the switching frequency.
5	6	VCC	**Bias supply.** VCC is the output of the internal regulator that supplies power to the internal control circuit and gate drivers. Connect a minimum 1μF decoupling capacitor from VCC to ground, and place it as close as possible to the VCC pin.
6	7	AGND	**Analog ground.**
7	8	FB	**Feedback input.** For fixed output versions, connect this pin to the output voltage directly. For the adjustable output version, connect this pin to the middle point of external feedback divider between output and AGND to set the output voltage.
8	9	PG	**Power good output.** The output of PG is an open drain. If PG is used, it must be connected to a power source through a pull-up resistor. PG goes high if the output voltage is within 94.5% to 105.5% of the nominal voltage; PG goes low if the output voltage is above 107% or below 93% of the nominal voltage. Float the PG pin if it is not used.
9	10	EN	**Enable.** Pull the EN pin below the specified threshold (about 0.85V) to shut down the chip. Pull EN above the specified threshold (about 1.02V) to enable the chip. The EN pin does not require an internal pull-up or pull-down resistor. Do not float the EN pin.
12	14	SW	**Switch node.** SW is the source of the high-side MOSFET and the drain of the low-side MOSFET.
	2, 12	NC	**No connection.** Can be tied to GND.

ABSOLUTE MAXIMUM RATINGS (2)

VIN, EN…… 42V for automotive load dump (3)
VIN, EN…….....-0.3V to +40V
SW…… -0.3V to $V_{IN(MAX)}$ + 0.3V
BOOT……..... V_{SW} + 5.5V
FREQ, VCC……..….5.5V
All other pins…… .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (4)
QFN-12 (2mmx3mm) ……..... 3.5W (8)
QFN-14 (2.5mmx3.5mm) ……... 3.7W (9)
QFN-12 (3mmx4mm) ……..... 3.6W (10)
Operating junction temperature ..... +150°C
Lead temperature……..... +260°C
Storage temperature…….. -65°C to +150°C

ESD Ratings

Human body model (HBM) ……..……Class 2 (5)
Charged device model (CDM).....Class C2b (6)

Recommended Operating Conditions

Supply voltage (V_{IN})…….3.3V to 36V
Minimum V_{IN} for start-up ……3.9V
Minimum V_{IN} after start-up ……..…….....3.1V
Output voltage (V_{OUT})…….....0.8V to 0.95 x V_{IN}
Operating junction temp (T_J) ……..
……-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-12 (2mmx3mm)
JESD51-7…..…..……60…....7.3…..°C/W (7)
EVQ4323C-D-00A ……...35.5.....3.5.....°C/W (8)
QFN-14 (2.5mmx3.5mm)
JESD51-7 …..…..48.6.....7.4.....°C/W (7)
EVQ4323C-RH-00A.…..33.6.....3.6.....°C/W (9)
QFN-12 (3mmx4mm)
JESD51-7 …..…..50.....7.5.....°C/W (7)
EVQ4323C-L-00A……..34.3.....3.7...°C/W (10)

Notes:

2) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
3) Refer to ISO16750.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002.
6) Per AEC-Q100-011.
7) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
8) Measured on an MPS MPQ4323CGDE standard EVB: 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.
9) Measured on an MPS MPQ4323CGRHE standard EVB: 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.
10) Measured on an MPS MPQ4323CGLE standard EVB: 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} under-voltage lockout (UVLO) rising threshold	VIN_{UVLO_RISING}		3.4	3.65	3.9	V
V_{IN} UVLO falling threshold	$VIN_{UVLO\_FALLING}$		2.6	2.9	3.1	V
V_{IN} UVLO hysteresis	VIN_{UVLO_HYS}			750		mV
V_{IN} active current (switching) (11)	I_{Q_ACTIVE}	CCM, no load		1200		µA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V		1	10	µA
V_{IN} over-voltage protection (OVP) rising threshold	VIN_{OVP_RISING}		35.5	37.5	40	V
V_{IN} OVP falling threshold	$VIN_{OVP\_FALLING}$		34.5	36.5	39	V
V_{IN} OVP hysteresis	VIN_{OVP_HYS}			1		V
Switches and Frequency						
Switching frequency without frequency spread spectrum (FSS)	f_{SW}	R_{FREQ} = 86.6kΩ	332	415	498	kHz
		R_{FREQ} = 34.8kΩ	900	1000	1100	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
FSS span				±10		%
FSS modulation frequency				15		kHz
Minimum on time (11)	t_{ON_MIN}			65	80	ns
Minimum off time (11)	t_{OFF_MIN}			50	70	ns
Maximum duty cycle	D_{MAX}		98	99.5		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = 25°C)		0.01	1	µA
		V_{EN} = 0V, V_{SW} = V_{BOOT} = 0V or V_{IN} (T_J = -40°C to +150°C)		0.01	5	µA
High-side MOSFET (HS-FET) on resistance	R_{ON_HS}	V_{BOOT} - V_{SW} = 5V		70	130	mΩ
Low-side MOSFET (LS-FET) on resistance	R_{ON_LS}	V_{CC} = 5V		50	90	mΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output and Regulation						
FB voltage (adjustable output version)	V_{FB}	T_J = 25°C	0.794	0.8	0.806	V
		T_J = -40°C to +150°C	0.790	0.8	0.810	V
FB input current	I_{FB}	Adjustable output version		0	100	nA
V_{OUT} discharge current	$I_{DISCHARGE}$	V_{EN} = 0V, V_{OUT} = 0.3V	2	4		mA
BOOT						
BOOT - SW refresh rising	V_{BOOT_RISING}			2.5	2.9	V
BOOT - SW refresh falling	$V_{BOOT\_FALLING}$			2.3	2.7	V
BOOT - SW refresh hysteresis	V_{BOOT_HYS}			0.2		V
EN						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN\_FALLING}$		0.8	0.85	0.9	V
EN threshold hysteresis	V_{EN_HYS}			170		mV
Soft Start and VCC						
Soft-start time	t_{SS}	EN high to SS finishes	3	5	7	ms
VCC voltage	V_{CC}	I_{VCC} = 0	4.7	5	5.3	V
VCC regulation		I_{VCC} = 30mA		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	70		mA
Power Good (PG)						
PG rising threshold (V_{FB} / V_{REF})	PG_{VTH_RISING}	V_{OUT} rising	93	94.5	96	%
		V_{OUT} falling	104	105.5	107	
PG falling threshold (V_{FB} / V_{REF})	$PG_{VTH\_FALLING}$	V_{OUT} falling	91.5	93	94.5	
		V_{OUT} rising	105.5	107	108.5	
PG threshold hysteresis (V_{FB} / V_{REF})	PG_{VTH_HYS}			1.5		
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t_{PG_R}			70		µs
PG falling deglitch time	t_{PG_F}			60		µs
Protections						
High-side (HS) peak current limit	I_{LIMIT_HS}	Duty cycle = 30%	4.3	5.8	7.3	A
Low-side (LS) valley current limit	I_{LIMIT_LS}		3	4.4	5.7	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$			1.8		A
Thermal shutdown (11)	T_{SD}		160	175	185	°C
Thermal shutdown hysteresis(11)	T_{SD_HYS}			20		°C

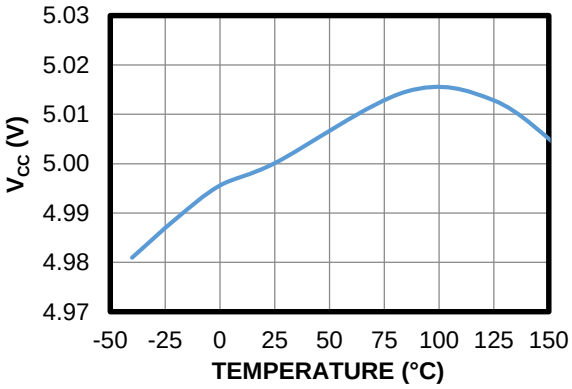
Note:

11) Not tested in production and guaranteed by design and characterization.

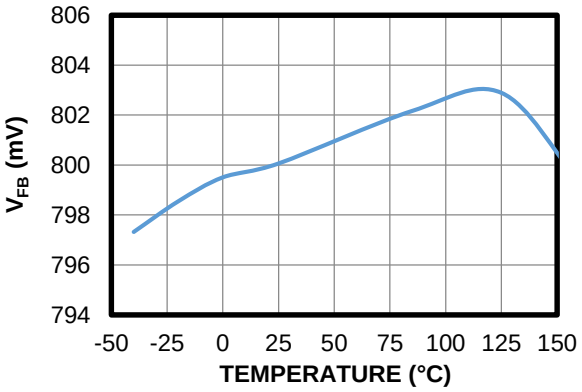
TYPICAL CHARACTERISTICS

V_{IN} = 12V, unless otherwise noted.

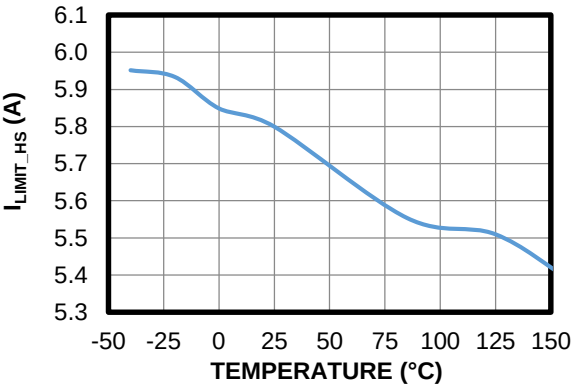
V_{cc} vs. Temperature



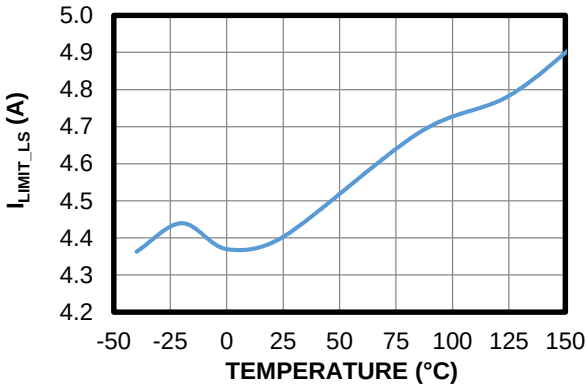
V_{FB} vs. Temperature



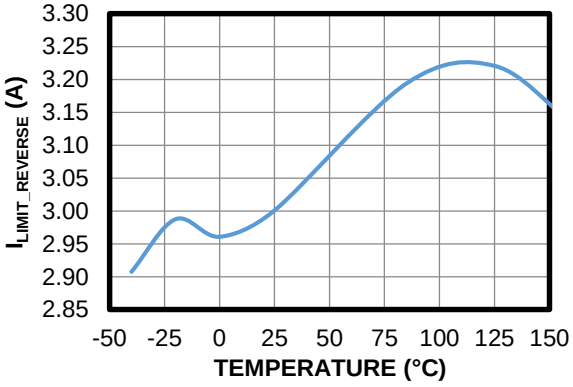
I_{LIMIT_HS} vs. Temperature



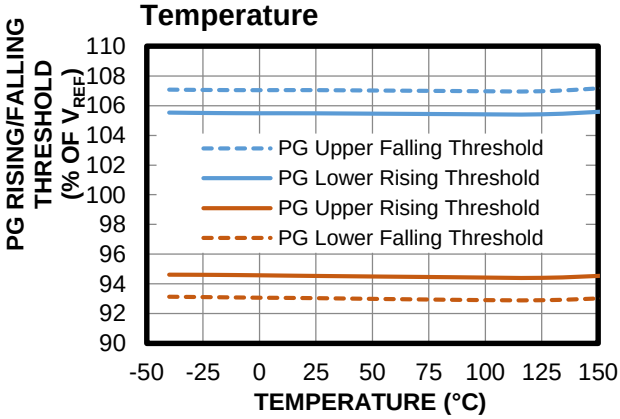
I_{LIMIT_LS} vs. Temperature



$I_{LIMIT\_REVERSE}$ vs. Temperature



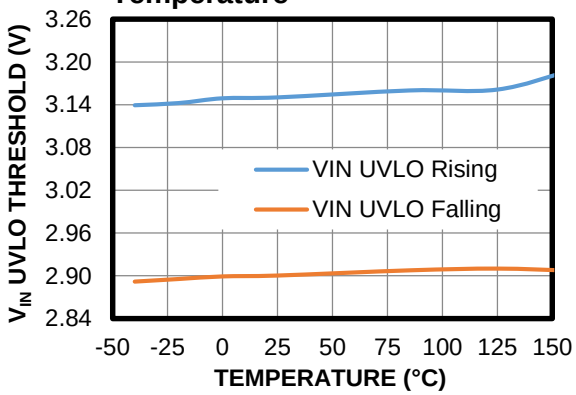
PG Rising/Falling Threshold vs. Temperature



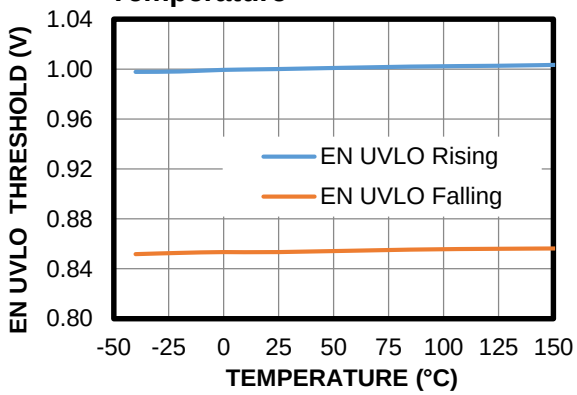
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

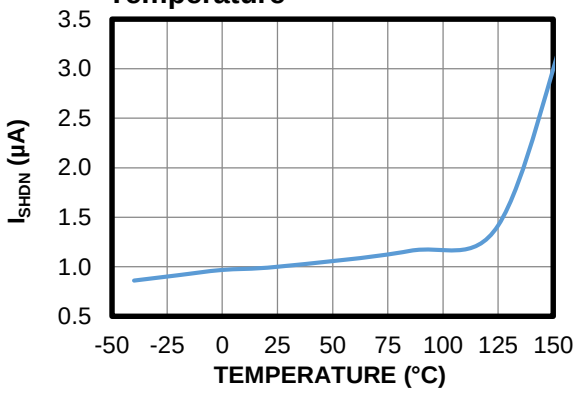
V_{IN} UVLO Threshold vs. Temperature



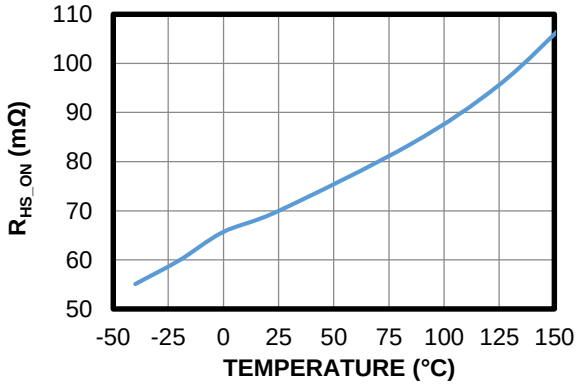
EN UVLO Threshold vs. Temperature



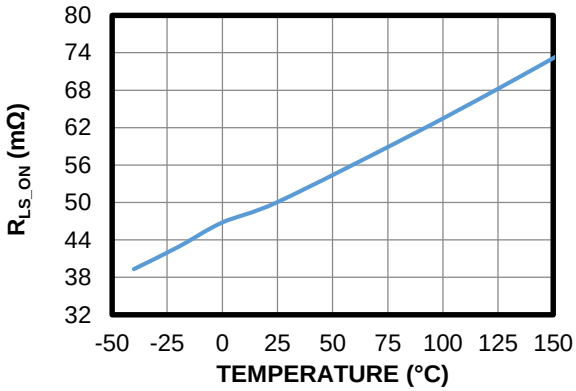
V_{IN} Shutdown Current vs. Temperature



R_{HS_ON} vs. Temperature

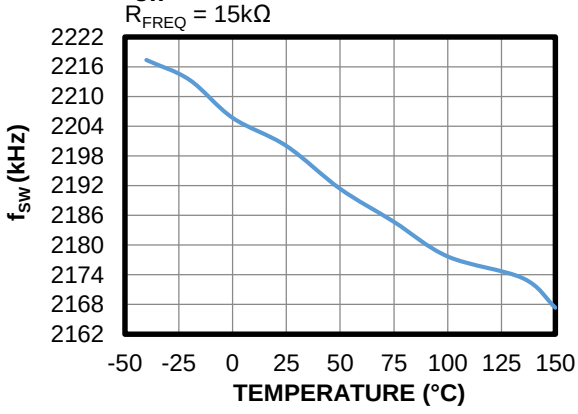


R_{LS_ON} vs. Temperature



f_{SW} vs. Temperature

R_{FREQ} = 15kΩ

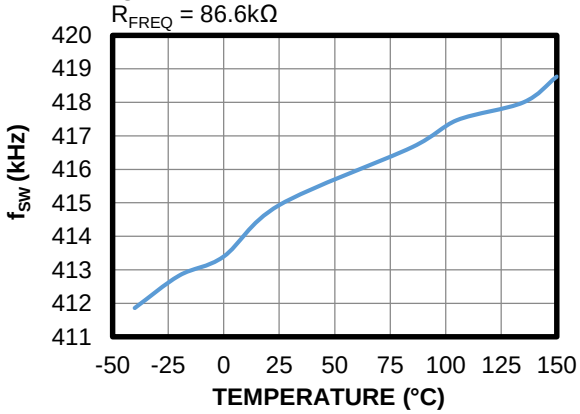


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, unless otherwise noted.

f_{SW} vs. Temperature

R_{FREQ} = 86.6kΩ

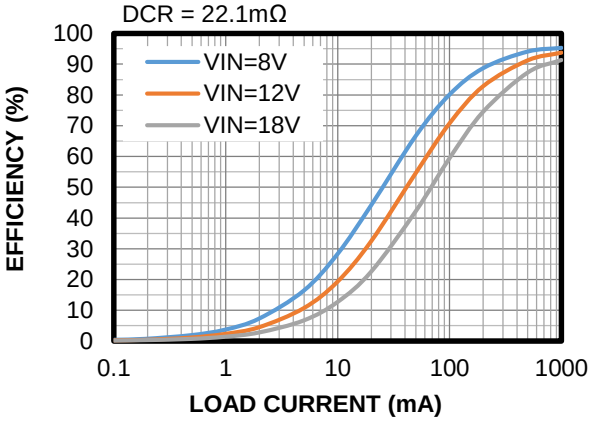


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

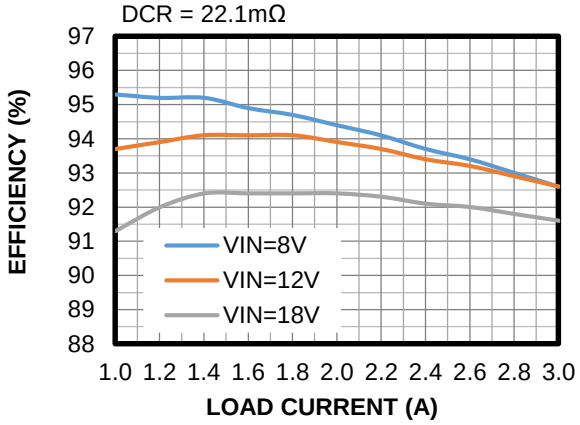
Efficiency vs. Load Current

DCR = 22.1mΩ



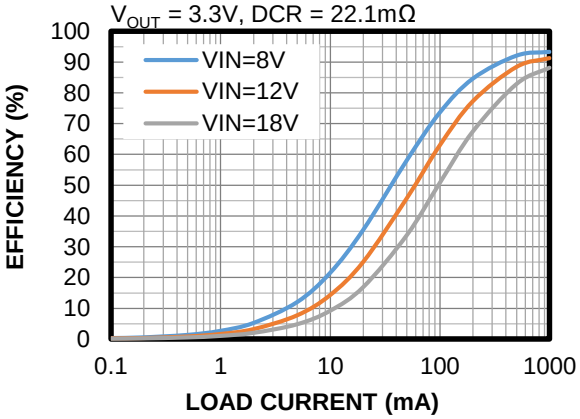
Efficiency vs. Load Current

DCR = 22.1mΩ



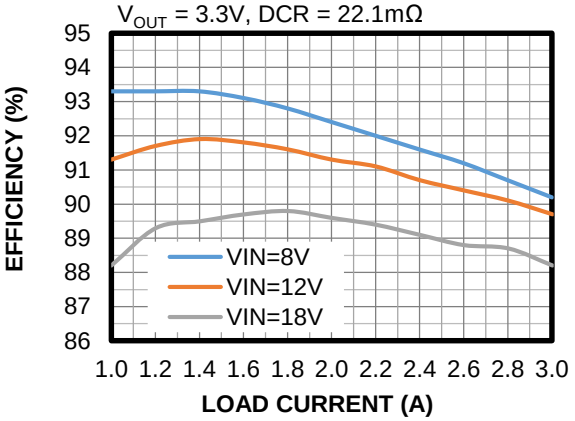
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 22.1mΩ



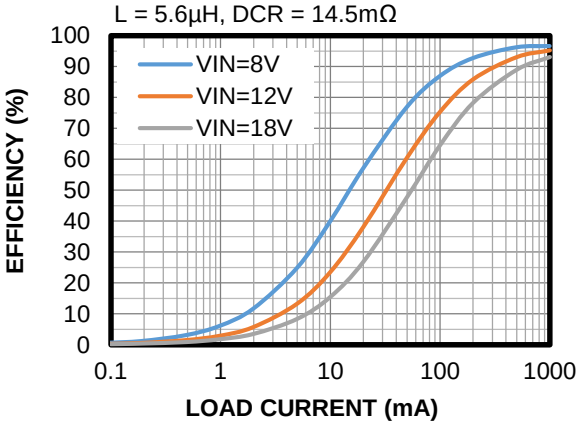
Efficiency vs. Load Current

V_{OUT} = 3.3V, DCR = 22.1mΩ



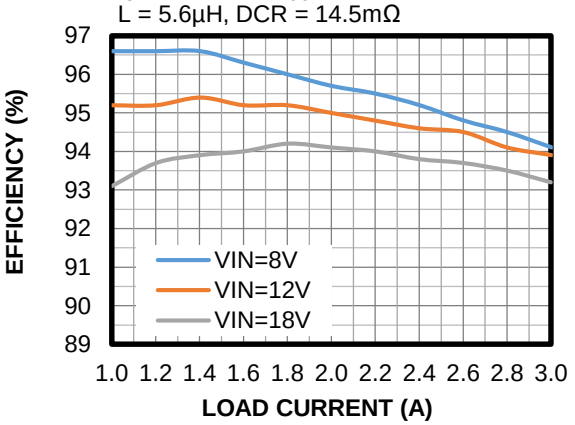
Efficiency vs. Load Current

f_{SW} = 415kHz, C_{OUT} = 47µFx2,
L = 5.6µH, DCR = 14.5mΩ



Efficiency vs. Load Current

f_{SW} = 415kHz, C_{OUT} = 47µFx2,
L = 5.6µH, DCR = 14.5mΩ

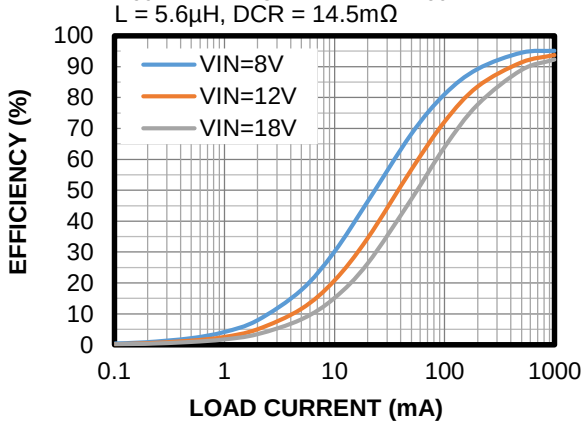


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

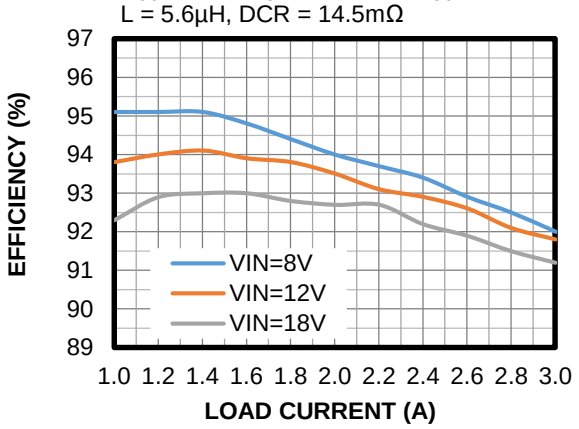
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 47µFx2, L = 5.6µH, DCR = 14.5mΩ



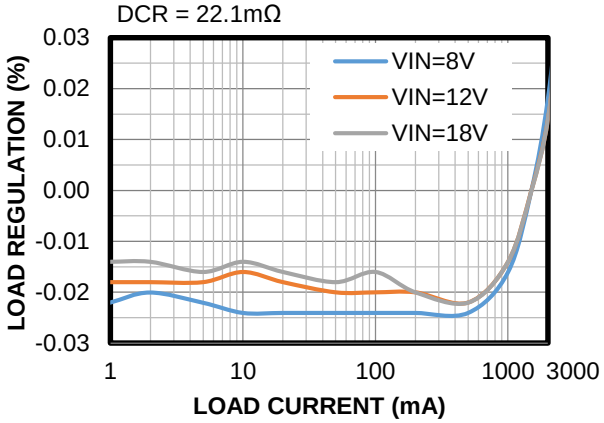
Efficiency vs. Load Current

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 47µFx2, L = 5.6µH, DCR = 14.5mΩ



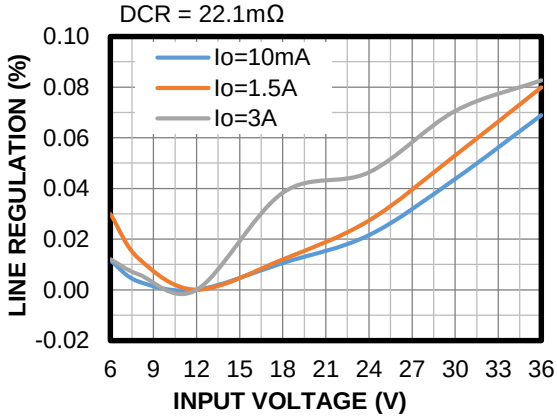
Load Regulation

DCR = 22.1mΩ



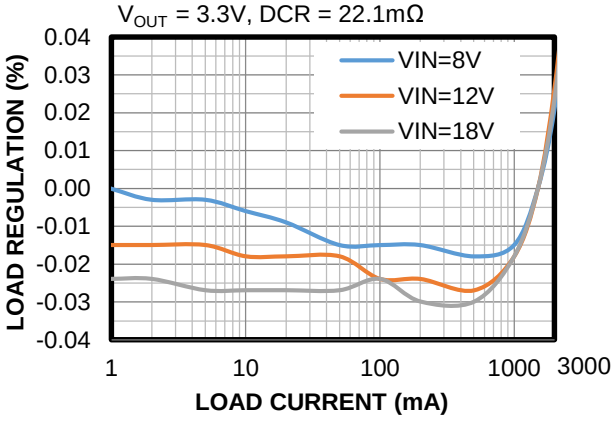
Line Regulation

DCR = 22.1mΩ



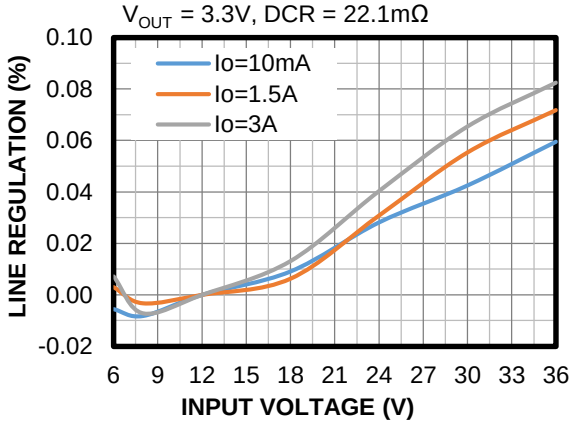
Load Regulation

V_{OUT} = 3.3V, DCR = 22.1mΩ



Line Regulation

V_{OUT} = 3.3V, DCR = 22.1mΩ

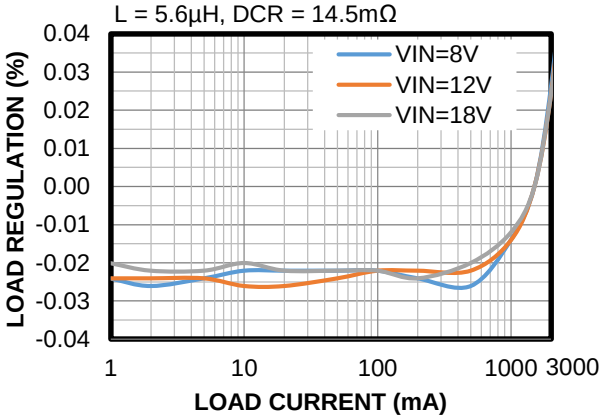


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

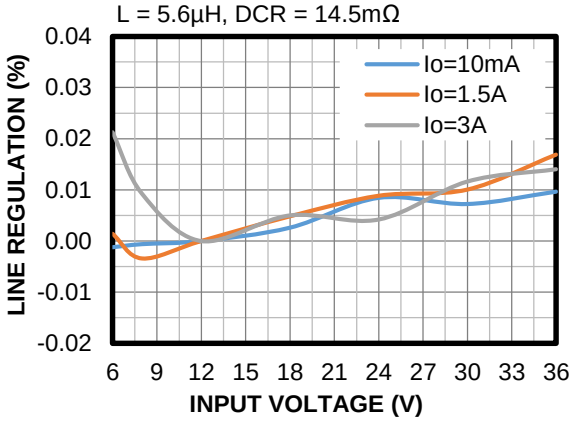
Load Regulation

f_{SW} = 415kHz, C_{OUT} = 47µFx2, L = 5.6µH, DCR = 14.5mΩ



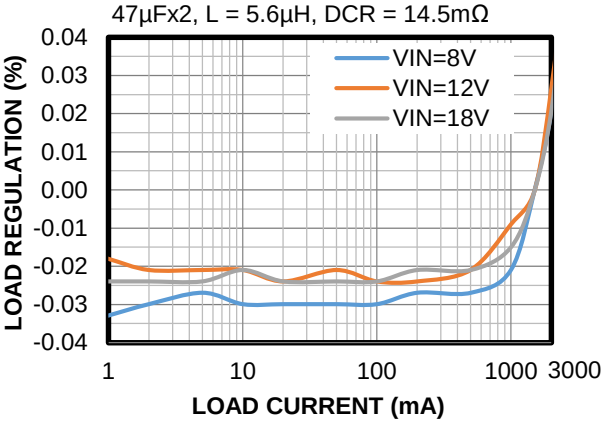
Line Regulation

f_{SW} = 415kHz, C_{OUT} = 47µFx2, L = 5.6µH, DCR = 14.5mΩ



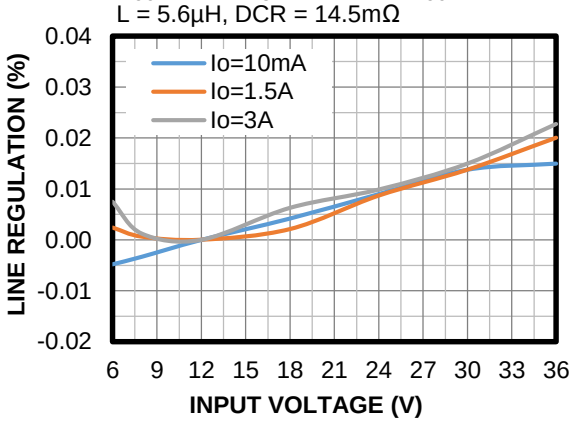
Load Regulation

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 47µFx2, L = 5.6µH, DCR = 14.5mΩ



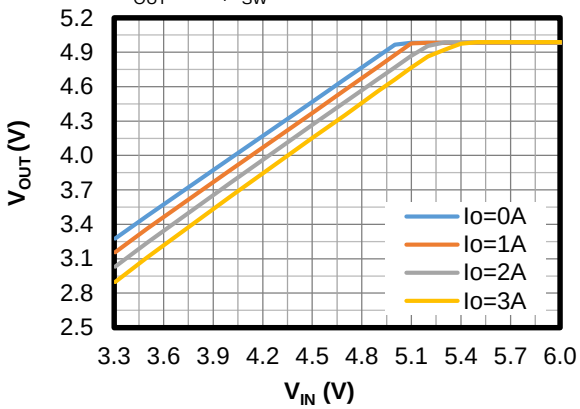
Line Regulation

V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 47µFx2, L = 5.6µH, DCR = 14.5mΩ



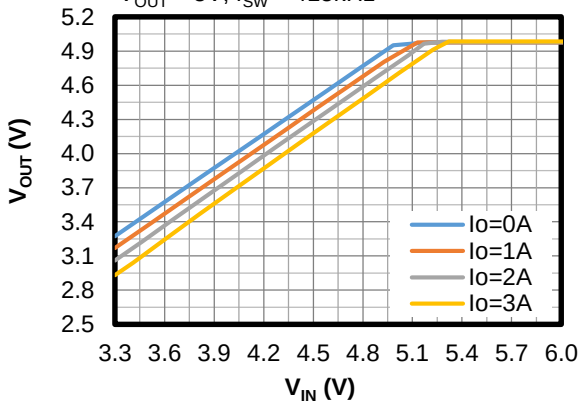
Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 2.2MHz



Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 415kHz

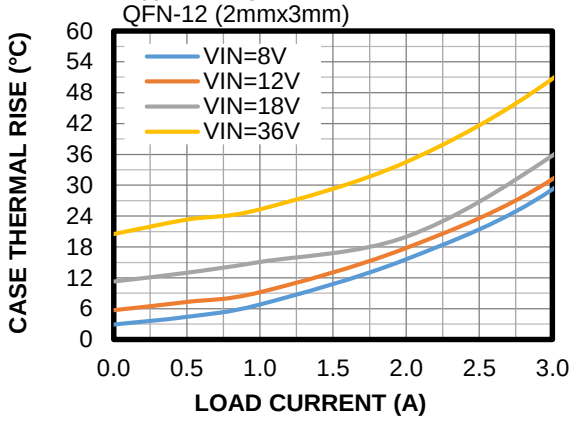


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

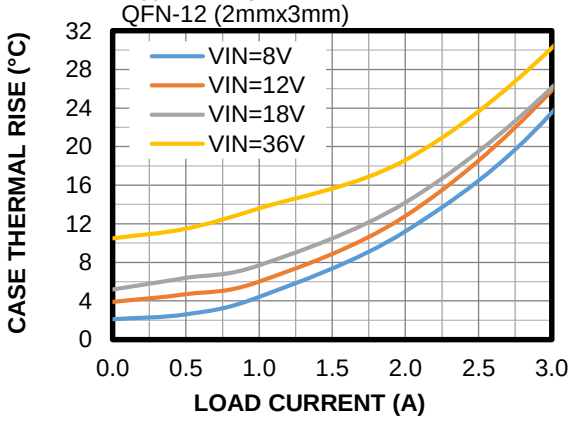
Case Thermal Rise

V_{OUT} = 5V, f_{SW} = 2.2MHz,
QFN-12 (2mmx3mm)



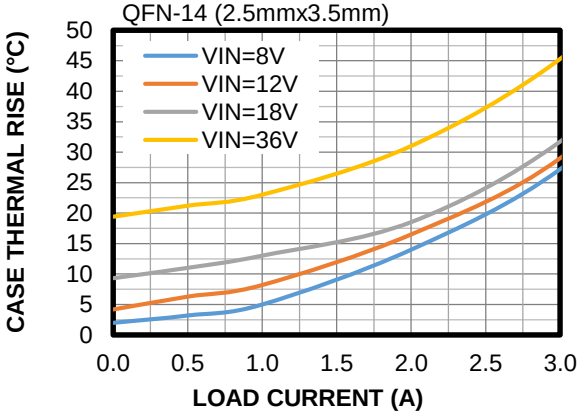
Case Thermal Rise

V_{OUT} = 5V, f_{SW} = 415kHz,
QFN-12 (2mmx3mm)



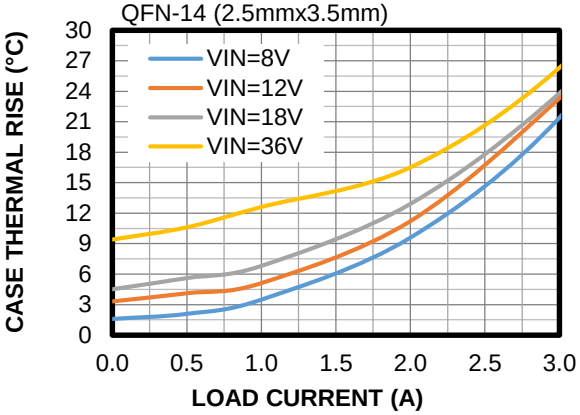
Case Thermal Rise

V_{OUT} = 5V, f_{SW} = 2.2MHz,
QFN-14 (2.5mmx3.5mm)



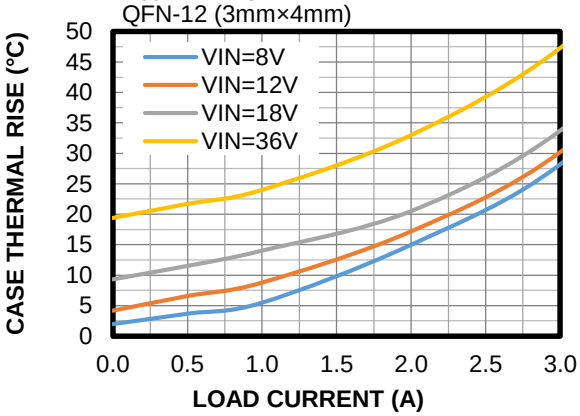
Case Thermal Rise

V_{OUT} = 5V, f_{SW} = 415kHz,
QFN-14 (2.5mmx3.5mm)



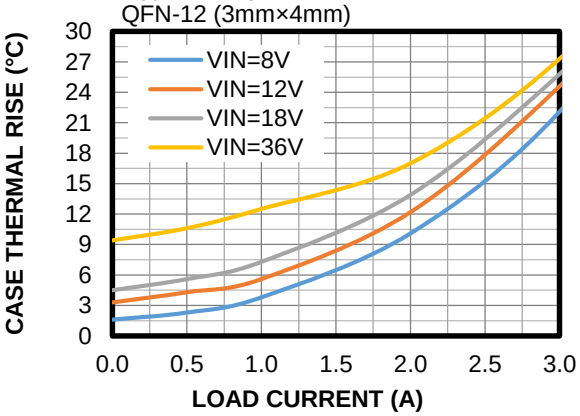
Case Thermal Rise

V_{OUT} = 5V, f_{SW} = 2.2MHz
QFN-12 (3mm×4mm)



Case Thermal Rise

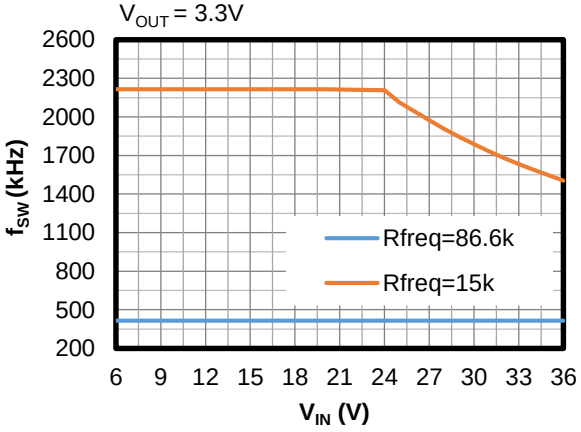
V_{OUT} = 5V, f_{SW} = 415kHz
QFN-12 (3mm×4mm)



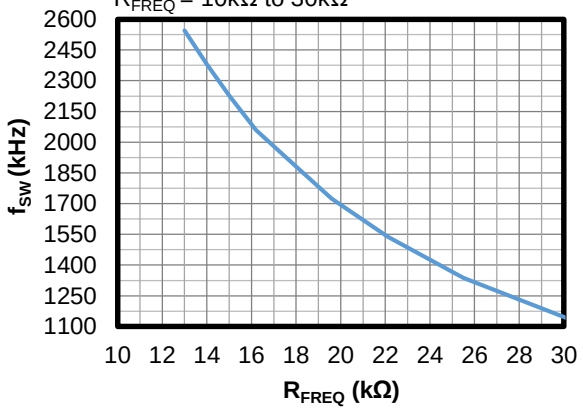
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

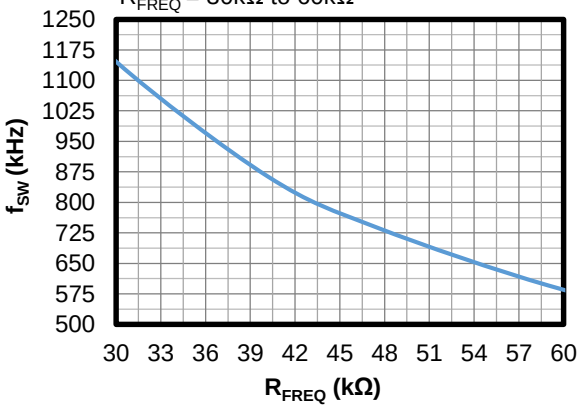
f_{SW} vs. V_{IN}
V_{OUT} = 3.3V



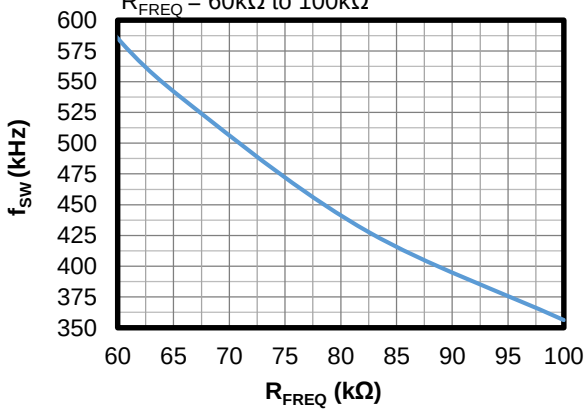
f_{SW} vs. R_{FREQ}
R_{FREQ} = 10kΩ to 30kΩ



f_{SW} vs. R_{FREQ}
R_{FREQ} = 30kΩ to 60kΩ



f_{SW} vs. R_{FREQ}
R_{FREQ} = 60kΩ to 100kΩ

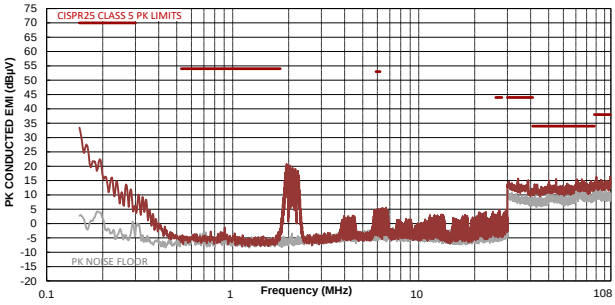


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.(12)

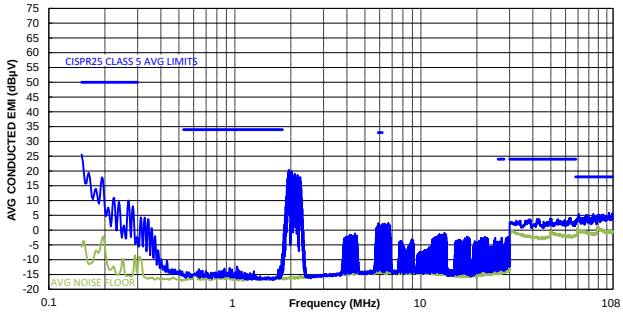
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



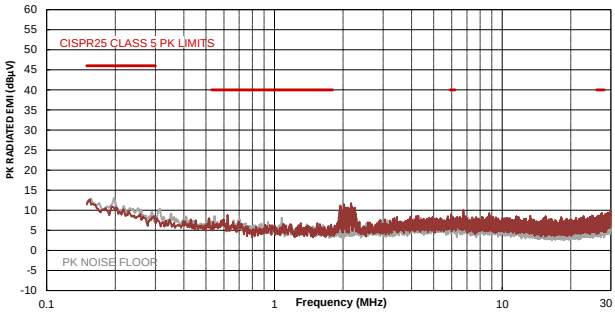
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



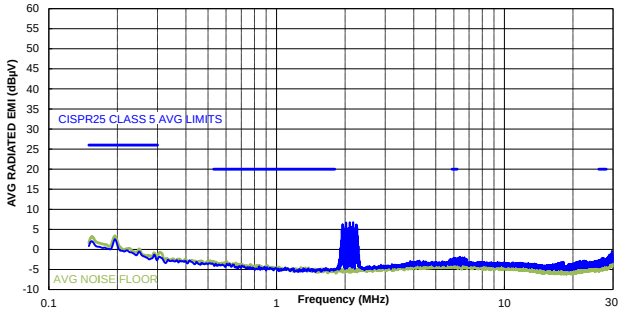
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



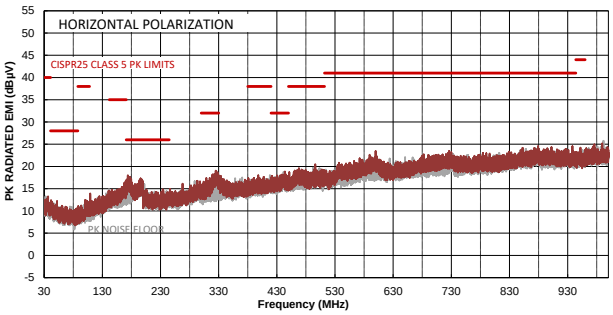
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



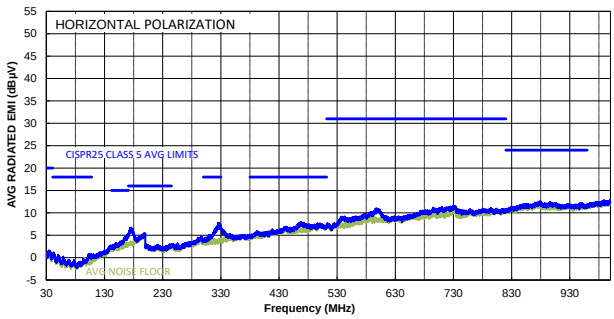
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

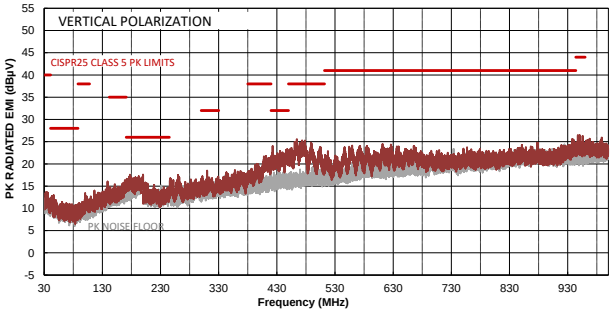


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.(12)

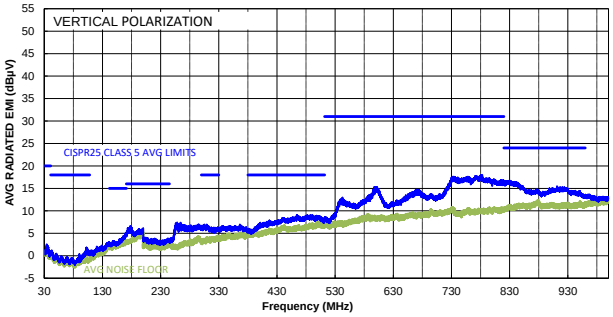
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

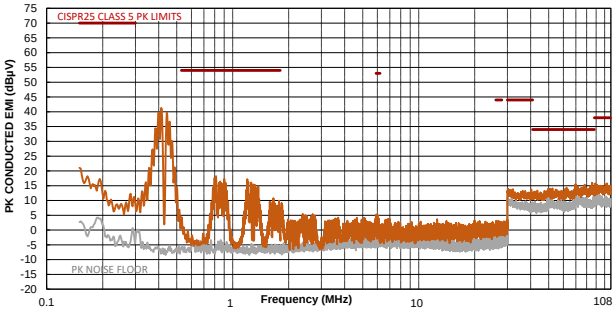
12) The EMC test results are based on the application circuit with EMI filters (see Figure 15 on page 38).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 5.6µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted.(13)

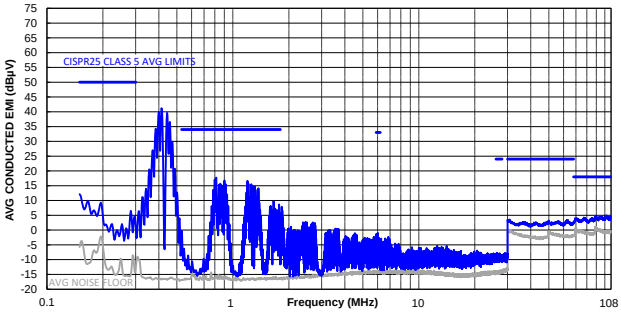
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



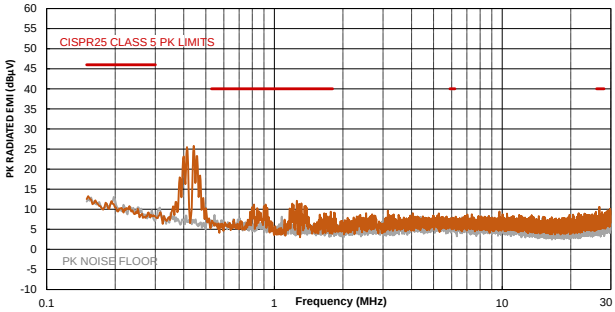
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



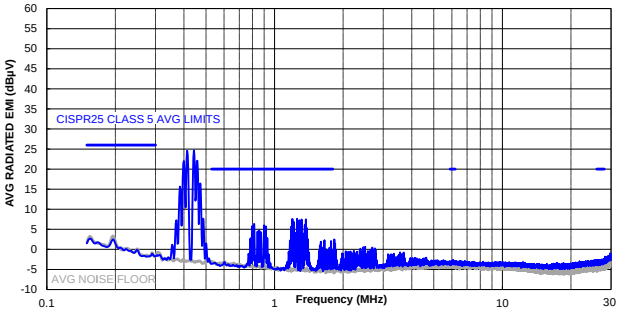
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



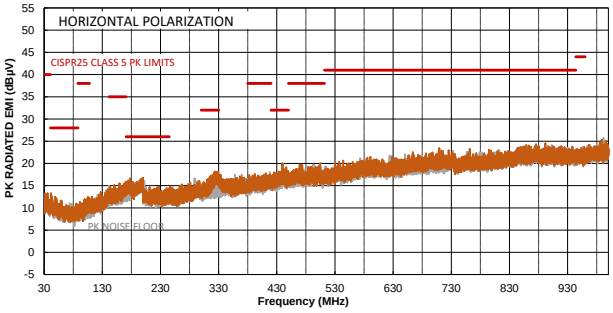
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



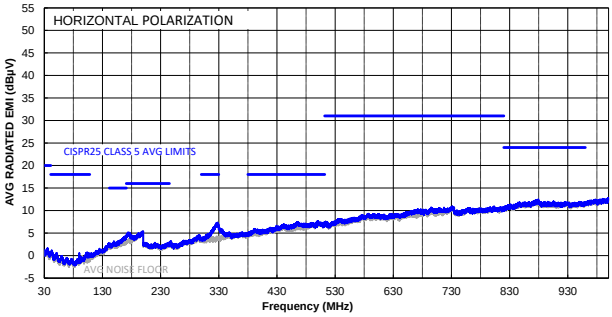
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

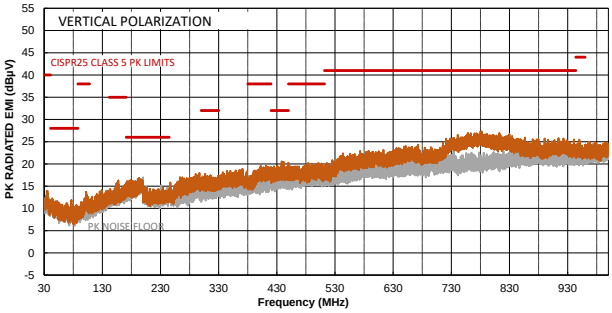


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 415kHz, L = 5.6µH, C_{OUT} = 47µF x 2, T_A = 25°C, unless otherwise noted.(13)

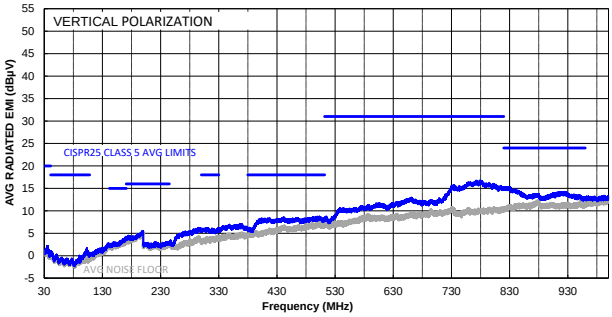
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



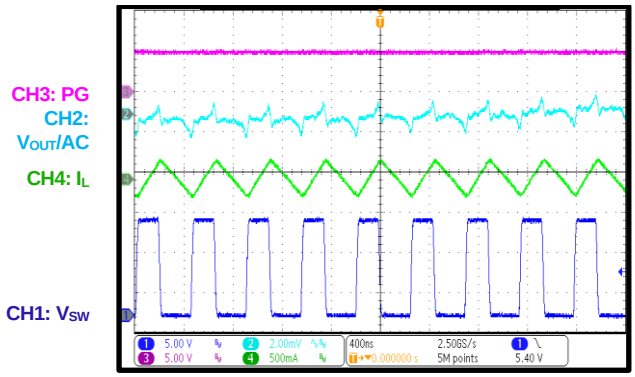
Note:

13) The EMC test results are based on the application circuit with EMI filters (see Figure 16 on page 39).

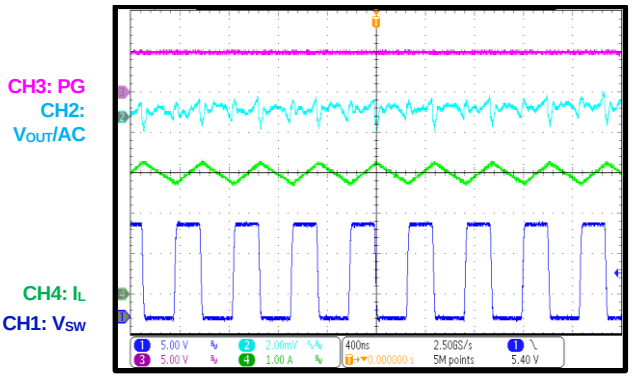
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

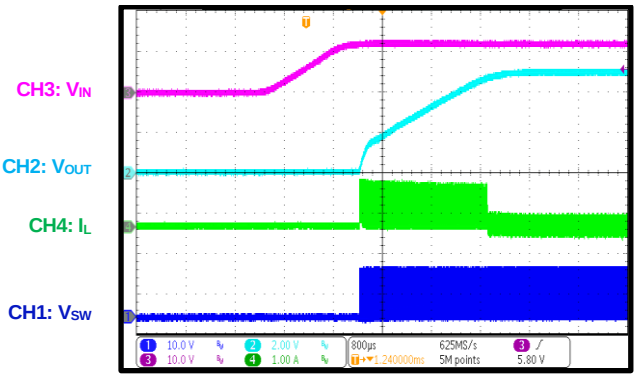
Steady State
I_{OUT} = 0A



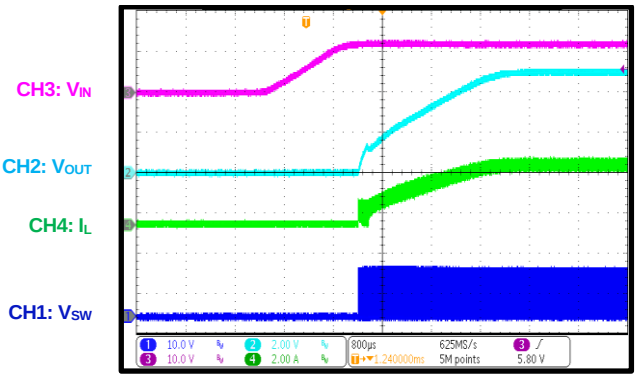
Steady State
I_{OUT} = 3A



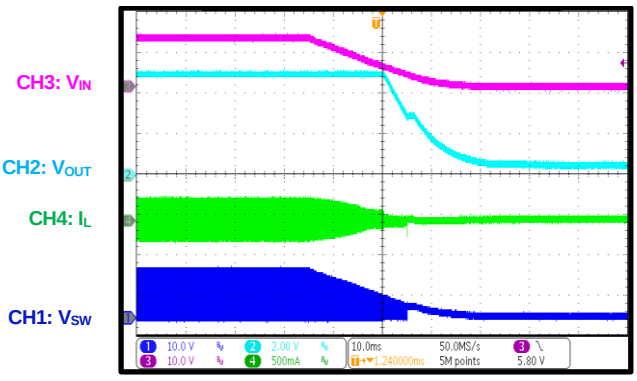
Start-Up through VIN
I_{OUT} = 0A



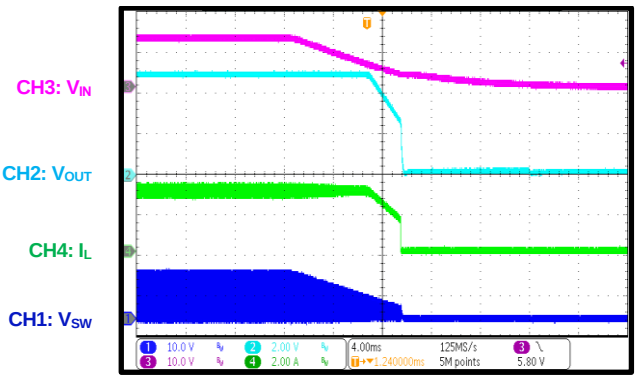
Start-Up through VIN
I_{OUT} = 3A



Shutdown through VIN
I_{OUT} = 0A



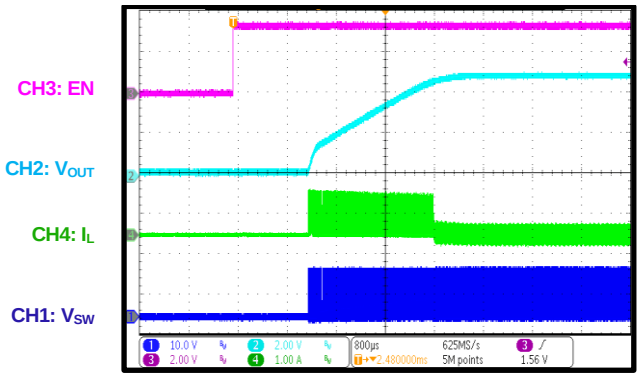
Shutdown through VIN
I_{OUT} = 3A



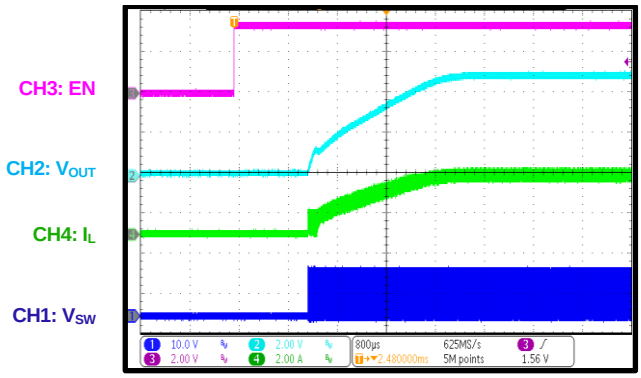
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

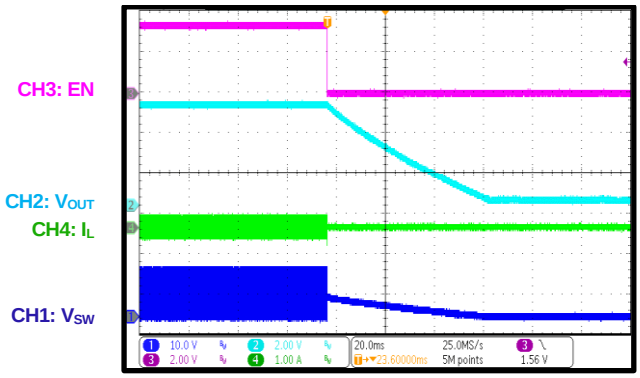
Start-Up through EN
I_{OUT} = 0A



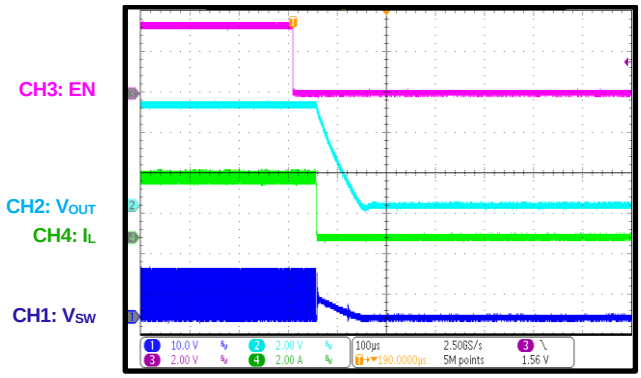
Start-Up through EN
I_{OUT} = 3A



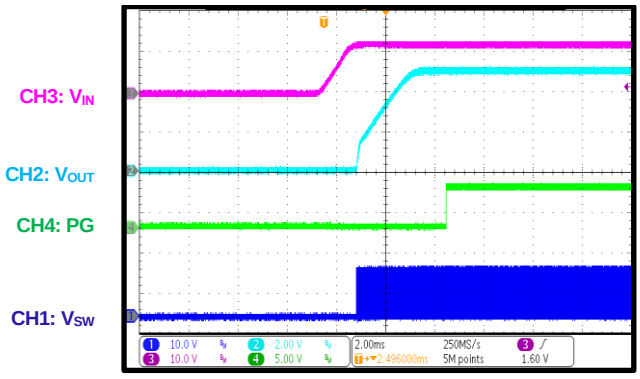
Shutdown through EN
I_{OUT} = 0A



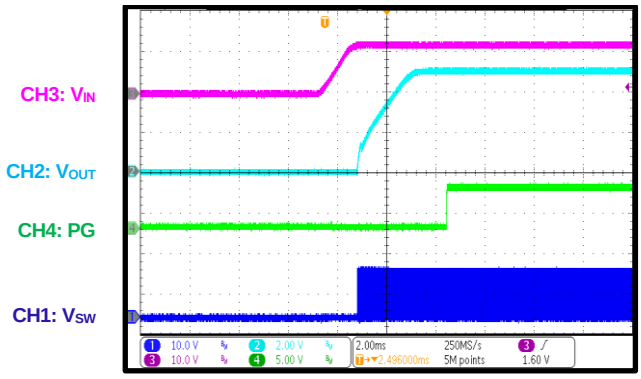
Shutdown through EN
I_{OUT} = 3A



PG during Start-Up through VIN
I_{OUT} = 0A



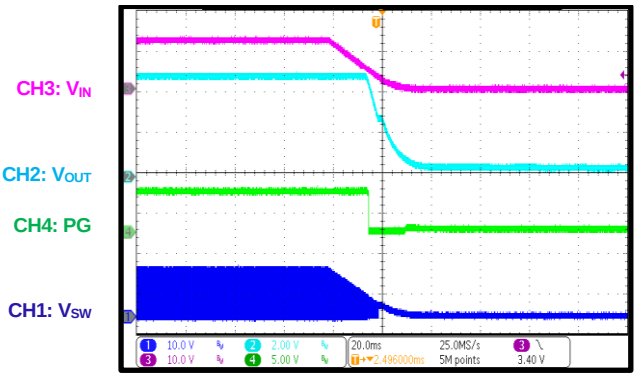
PG during Start-Up through VIN
I_{OUT} = 3A



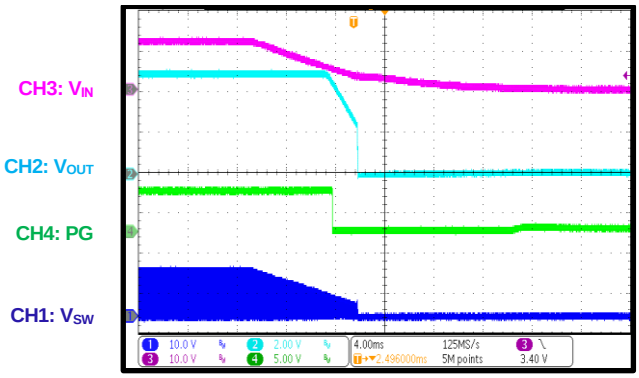
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

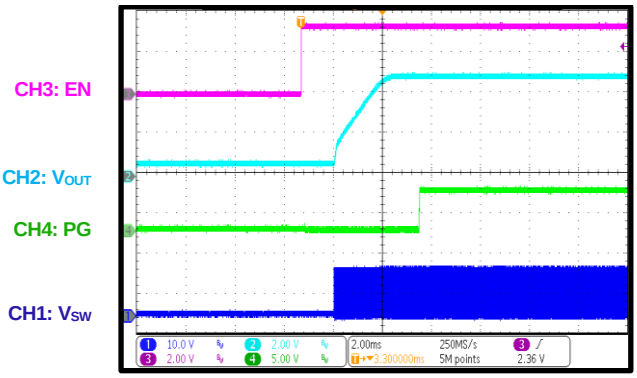
PG during Shutdown through VIN
I_{OUT} = 0A



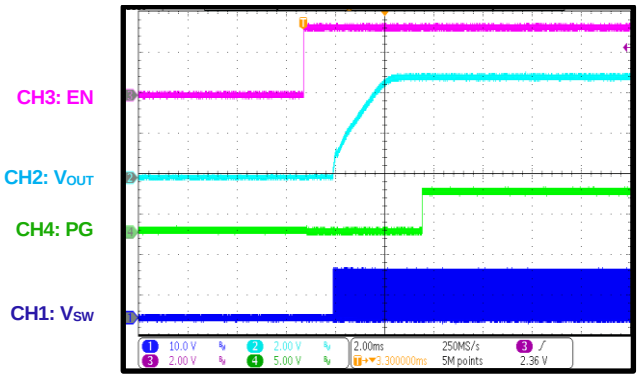
PG during Shutdown through VIN
I_{OUT} = 3A



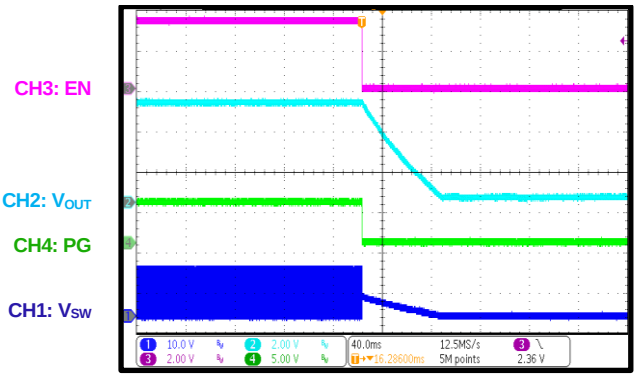
PG during Start-Up through EN
I_{OUT} = 0A



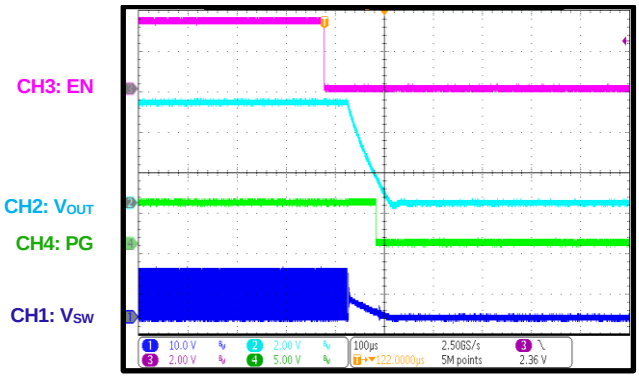
PG during Start-Up through EN
I_{OUT} = 3A



PG during Shutdown through EN
I_{OUT} = 0A



PG during Shutdown through EN
I_{OUT} = 3A

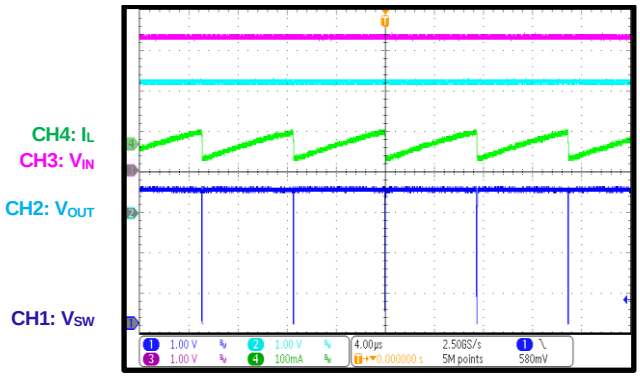


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

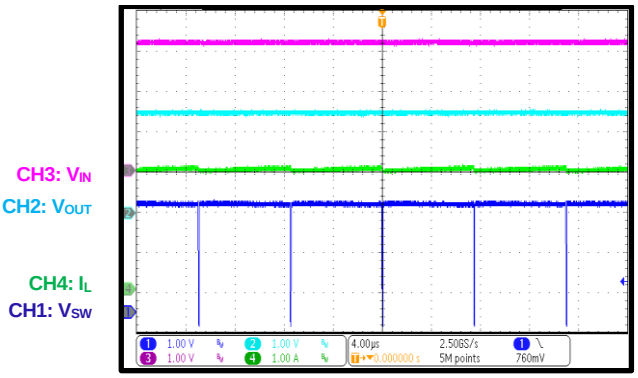
Low-Dropout Mode

I_{OUT} = 0A, V_{IN} = 3.3V



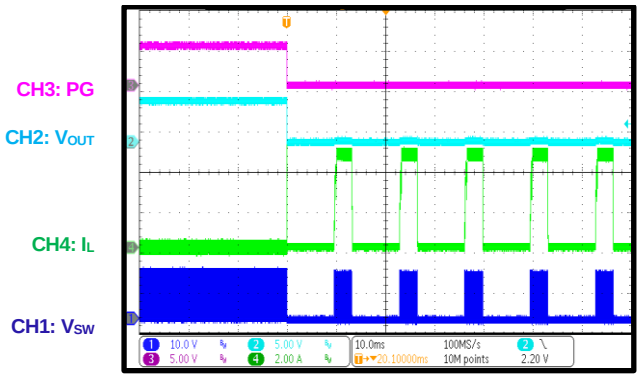
Low-Dropout Mode

I_{OUT} = 3A, V_{IN} = 3.3V



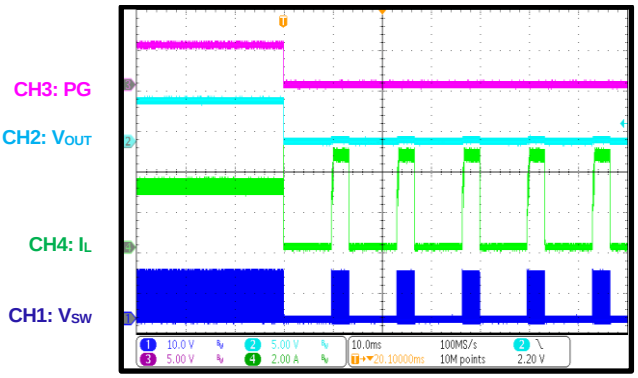
SCP Entry

I_{OUT} = 0A



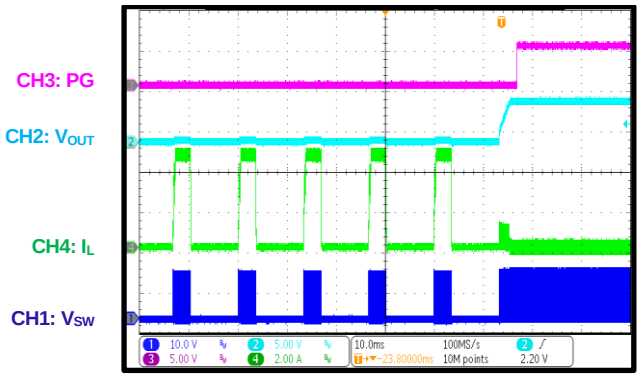
SCP Entry

I_{OUT} = 3A



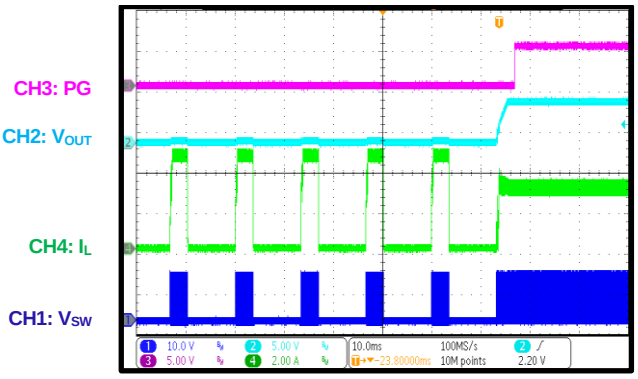
SCP Recovery

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 3A

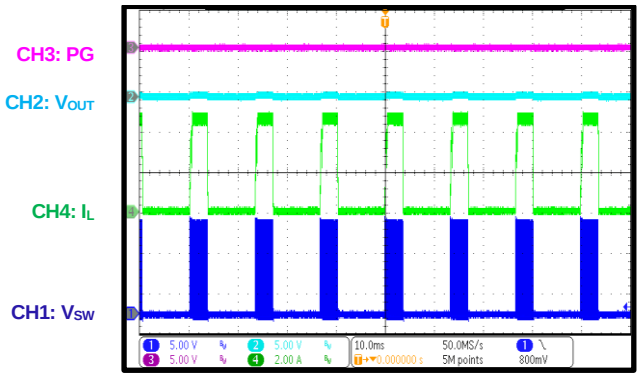


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

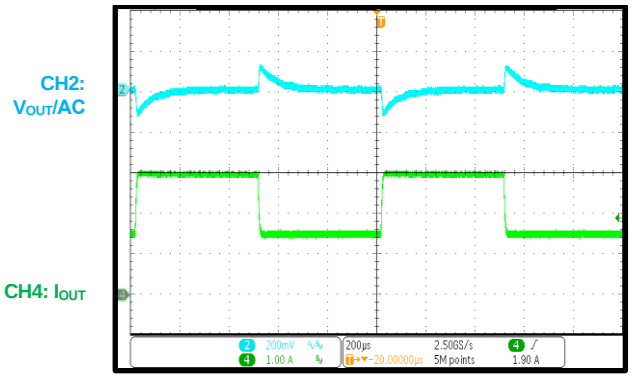
SCP Steady State

I_{OUT} = 0A



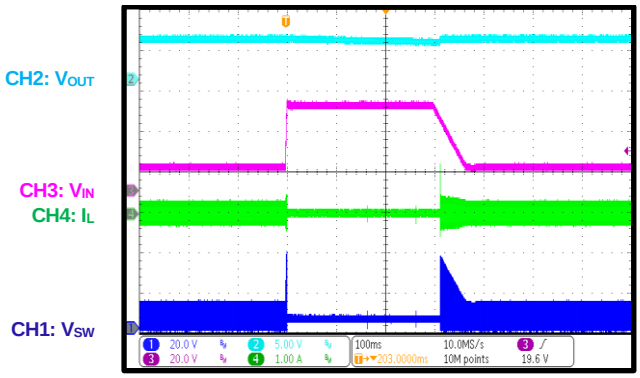
Load Transient

I_{OUT} = 1.5A to 3A, 1.6A/µs



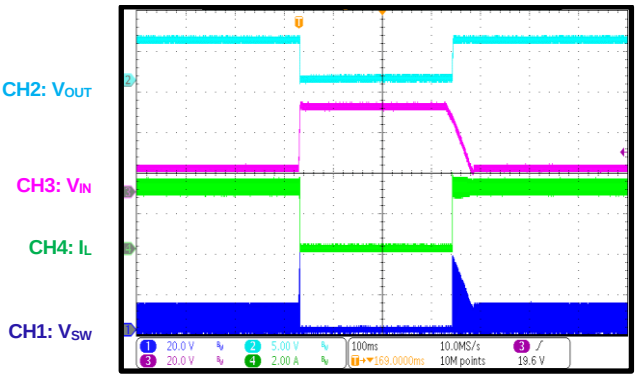
Load Dump

V_{IN}= 12V to 42V, I_{OUT} = 0A



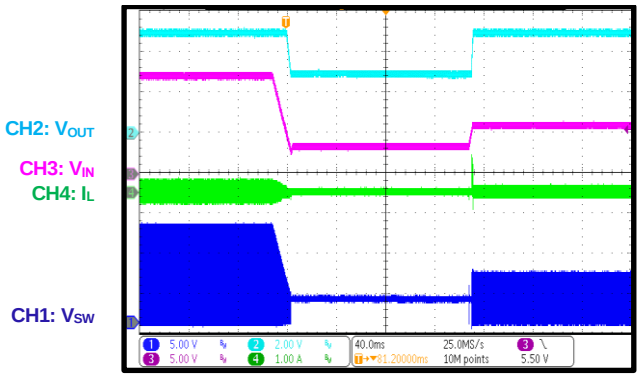
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 3A



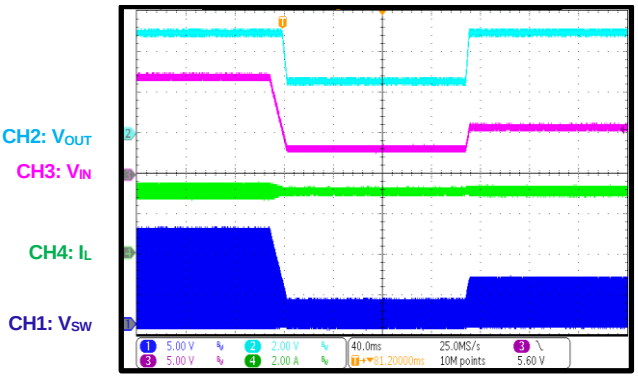
Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 0A



Cold Crank

V_{IN} = 12V to 3.3V to 6V, I_{OUT} = 3A

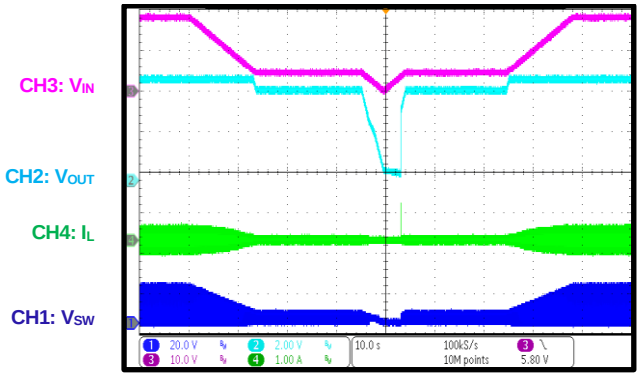


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH, C_{OUT} = 22µF x 2, T_A = 25°C, unless otherwise noted.

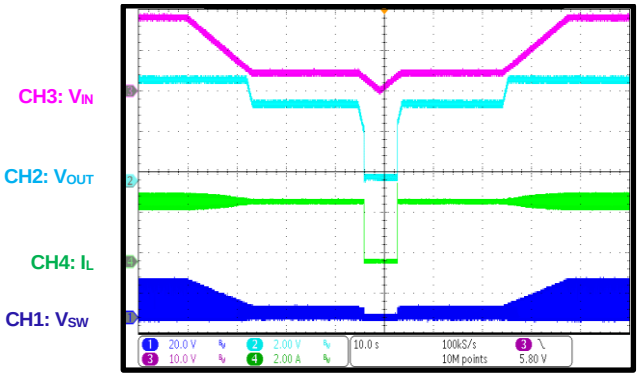
V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 0A



V_{IN} Ramping Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V,
I_{OUT} = 3A



FUNCTIONAL BLOCK DIAGRAM

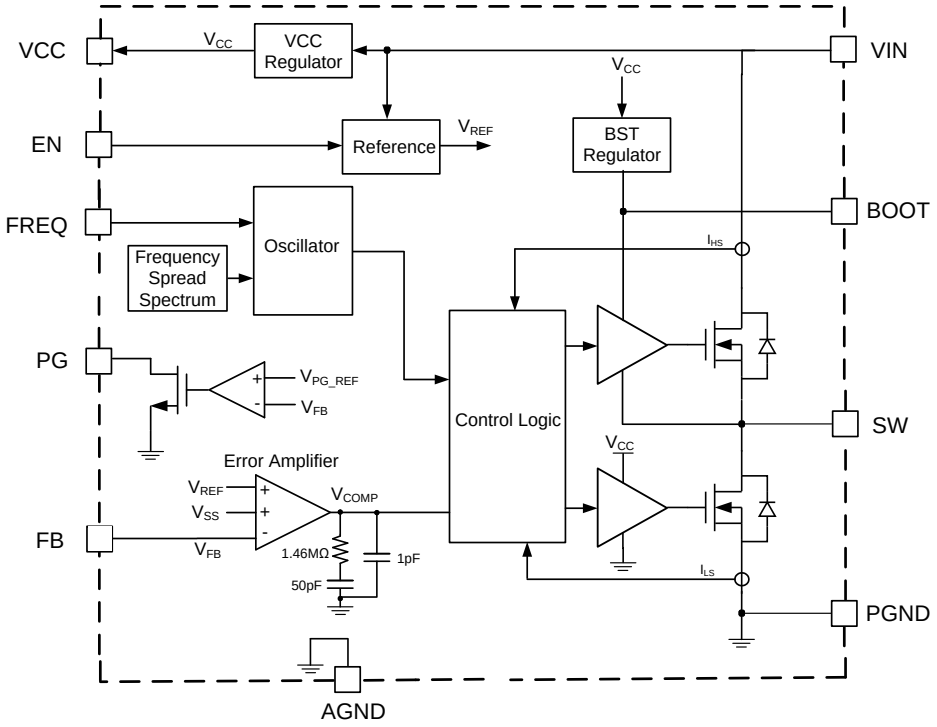


Figure 3: Functional Block Diagram (Adjustable Output)

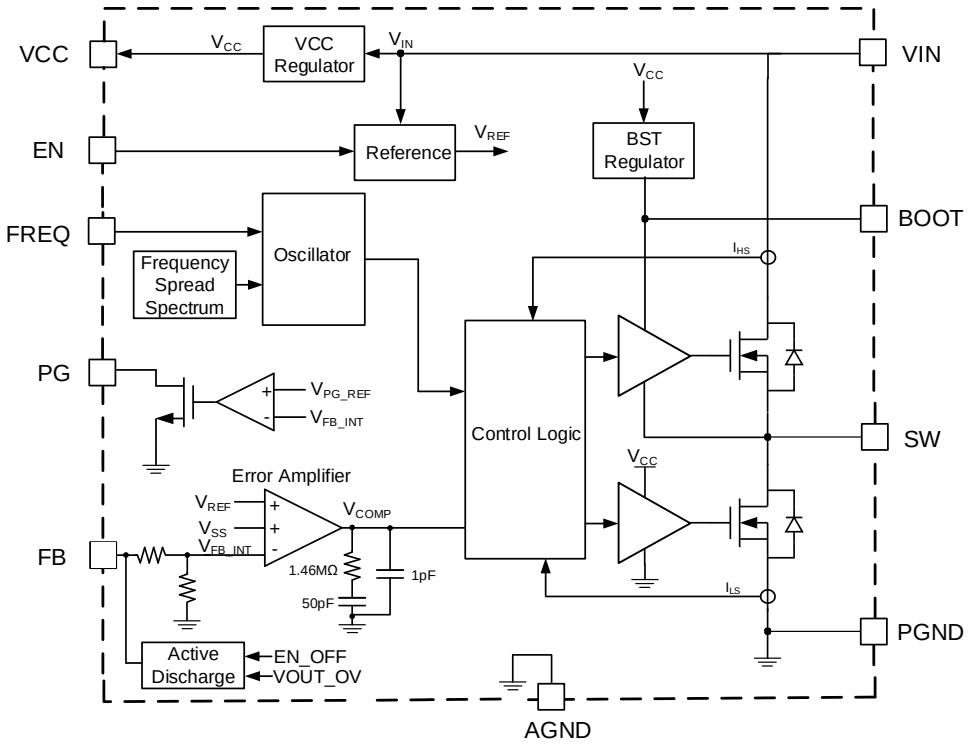


Figure 4: Functional Block Diagram (Fixed Output)

OPERATION

The MPQ4323C is a synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs. It provides 3A of highly efficient output current (I_{OUT}) with peak current mode control.

The devices features a wide input voltage (V_{IN}) range, configurable 350kHz to 2.5MHz switching frequency (f_{SW}), internal soft start, and precision current limit. The MPQ4323C's very low operational quiescent current makes it well-suited for battery-powered applications.

PWM Control

At moderate to high output currents, the MPQ4323C operates with fixed-frequency, peak current mode control to regulate the output voltage (V_{OUT}). A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}).

When the HS-FET is off, the low-side power MOSFET (LS-FET) turns on immediately and stays on until the next cycle starts, or until the inductor current (I_L) falls below the reverse current limit. The LS-FET remains off for at least the minimum off time before the next cycle starts.

If the current in the HS-FET cannot reach the value set by COMP within one PWM period, the HS-FET remains on and skips a turn-off operation. The HS-FET is forced on until it reaches the value set by COMP, or its 7µs maximum on time is reached. This operation mode extends the duty cycle, which achieves a low dropout when V_{IN} is almost equal to V_{OUT}.

Light-Load Operation

Under light-load conditions, the MPQ4323C can work in forced continuous conduction mode (FCCM). In this mode, the device works with a fixed frequency from the no-load to full-load range. The advantages of FCCM are its controllable frequency and lower output voltage ripple under light loads.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin's voltage (V_{FB}) with the internal reference (0.8V) and outputs a current proportional to the difference between the two values. This output current is then used to charge the compensation network to form V_{COMP}, which is the error used to control the power MOSFET's duty cycle.

During operation, the minimum V_{COMP} is clamped to 0.5V and its maximum is clamped to 2.5V. COMP is internally pulled down to GND in shutdown mode.

Frequency Spread Spectrum (FSS)

The MPQ4323C uses a 15kHz modulation frequency with a maximum 128-step triangular profile to spread the internal oscillator frequency across a 20% (±10%) window. The steps vary with the set oscillator frequency to ensure that the exact f_{SW} steps cycle by cycle (see Figure 5).

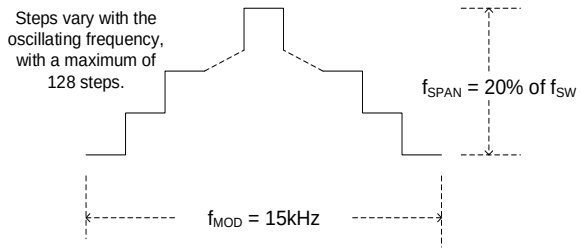


Figure 5: Frequency Spread Spectrum

Side bands are created by modulating the switching frequency with the triangle modulation waveform. The emission power of the fundamental switching frequency and its harmonics is reduced. This significantly reduces the peak EMI noise.

Soft Start (SS)

Soft start is implemented to prevent the converter output voltage from overshooting during start-up. The soft-start time is fixed internally.

When the soft-start period starts, the soft-start voltage (V_{SS}) rises from 0V to 1.2V with a specific slew rate. When V_{SS} is below the internal 0.8V reference voltage (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

When the chip is enabled by EN, the first pulse is sent after about 830µs. During this period, VCC is regulated, and the internal bias is complete, the compensator network finishes charging After another 2.9ms, V_{OUT} ramps up

and reaches the set value. Then soft start completes after 1.5ms, and PG pulls high after a 70µs delay.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} at start-up, the output has a pre-biased voltage. In this scenario, neither the HS-FET nor LS-FET turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature rises above its upper threshold (about 175°C), the device shuts down the power MOSFETs. If the temperature drops below its lower threshold (about 155°C), the thermal shutdown condition is removed, and the chip is enabled again.

Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. When the inductor current (I_L) reaches the high-side peak current limit (typically 5.8A) while the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side valley current limit (typically 4.4A). Then I_L can drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Reverse Current Limit

The direction of the reverse current flows from the output voltage to the SW node. The MPQ4323C has a 1.8A reverse current limit. Once I_L reaches the current limit, the LS-FET immediately turns off, and the HS-FET turns on. The current limit prevents the negative current from dropping too low and damaging the components.

Short-Circuit Protection (SCP)

If the output is shorted to ground, and the output voltage drops below 70% of its nominal output, the MPQ4323C shuts down and begins discharging V_{SS}. The device restarts with a full soft start when V_{SS} is fully discharged. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

The MPQ4323C stops switching if V_{OUT} exceeds 130% of its nominal regulation value. An internal, 75Ω discharge path from FB to GND is activated to discharge V_{OUT}. This discharge path only can be activated if the output is fixed. The device resumes switching when V_{OUT} drops back to 125% of its nominal value, and then the discharge path is disabled.

For a fixed output, the V_{OUT} discharge path is also activated if an EN shutdown occurs while V_{CC} exceeds its under-voltage lockout (UVLO) threshold. When V_{CC} drops to its UVLO threshold, this path is deactivated.

Start-Up and Shutdown

If both V_{IN} and EN exceeds their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

When the internal supply rail is up, the internal circuits start to work. If BOOT does not reach its refresh rising threshold (about 2.5V), the LS-FET turns on to charge BOOT. The HS-FET stays off during this time. When the soft-start block is enabled, V_{OUT} starts to ramp up slowly. V_{OUT} smoothly reaches its target within 5ms.

Three events shut down the chip: EN going low, V_{IN} falling below its UVLO threshold, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then the COMP voltage is pulled down, and the floating driver works to disable the HS-FET.

APPLICATION INFORMATION

Figure 6 shows the MPQ4323C's typical application circuit.

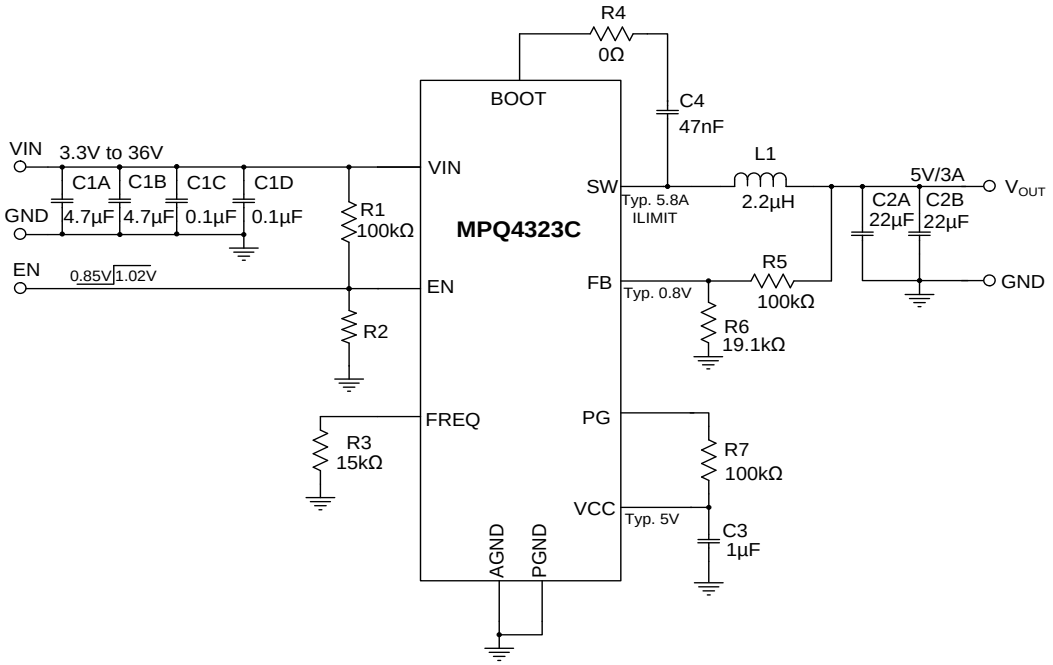


Figure 6: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

QFN-12 Pin #	QFN-12 Pin #	Pin Name	Component	Design Guide Index
1, 11	1, 13	PGND	-	Connection GND (GND and PGND)
2, 10	3, 11	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN)
3	4	BOOT	R4, C4	The Floating Driver and Bootstrap Charging (BOOT)
4	5	FREQ	R3	Setting the Switching Frequency (FREQ)
5	6	VCC	C3	The Internal VCC (VCC)
6	7	AGND		Connection GND (GND and PGND)
7	8	FB	R5, R6	Feedback (FB)
8	9	PG	R7	Power Good Indication (PG)
9	10	EN	R1, R2	Enable Control (EN) and Under-Voltage Lockout (UVLO)
12	14	SW	L1, C2A, C2B	Selecting the Inductor and Output Capacitors (SW)
-	2, 12	NC	-	No Connection (NC)

Selecting the Input Capacitors (VIN)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (1)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

V_{IN} Over-Voltage Protection (OVP)

The MPQ4323C stops switching when V_{IN} rises above its over-voltage (OV) rising threshold (typically 37.5V). The device resumes normal regulation and switching when V_{IN} drops to the OV falling threshold (typically 36.5V).

The Floating Driver and Bootstrap Charging (BOOT)

The BOOT capacitor (C4, also called C_{BOOT}) is recommended to be between 22nF and 100nF.

It is not recommended to place a resistor (R_{BOOT}) in series with the BOOT capacitor, unless there is a strict EMI requirement. R_{BOOT} helps enhance EMI performance and reduce voltage stress at high input voltages, but it also generates additional power consumption and reduces efficiency. When R_{BOOT} is necessary, it should be below 4Ω.

The voltage between BOOT and SW ($V_{BOOT-SW}$) is regulated to about 5V by the dedicated internal bootstrap regulator. When $V_{BOOT-SW}$ is below this value, an N-channel MOSFET pass transistor connected from VCC to BOOT turns on to charge the bootstrap capacitor (C_{BOOT}). The external circuit should provide enough voltage headroom to facilitate the charging. When the HS-FET is on, the BOOT voltage exceeds V_{CC}, so the bootstrap capacitor cannot be charged.

Under conditions with higher duty cycles, the time available for bootstrap charging is shorter, so the bootstrap capacitor may not be charged sufficiently. In this case, the external circuit has insufficient voltage and time to charge the bootstrap capacitor. External circuitry can be used to ensure that the bootstrap voltage remains in the normal operation region.

If the bootstrap voltage reaches its under-voltage lockout (UVLO) threshold, the HS-FET turns off, and the LS-FET turns on with a minimum off time to refresh the bootstrap voltage with the set f_{SW}.

Setting the Switching Frequency (FREQ)

A resistor (R3) can set the switching frequency (see Table 2 on page 32 and the f_{SW} vs. R_{FREQ} curves on page 16).

The MPQ4323C switching frequency can be configured by an external resistor (R_{FREQ}) connected from the FREQ pin to ground. The frequency resistor should be located between the FREQ pin and GND, placed as close as possible to the device. Table 2 on page 32 shows the relationship between the switching frequency and R_{FREQ}.

Table 2: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)	R_{FREQ} (kΩ)	f_{SW} (kHz)
100	355	30.1	1150
93.1	385	26.1	1300
86.6	415	22.6	1450
80.6	450	20.5	1600
75	480	19.6	1750
68.1	520	17.8	1900
59	600	16.2	2050
51.1	700	15	2200
40.2	850	14.3	2350
34.8	1000	13.3	2500

It is not possible to have both a high switching frequency and input voltage due to the HS-FET's limited minimum on time. The MPQ4323C control loop automatically sets the maximum possible f_{SW} to the set frequency, which also reduces excessive power loss. V_{OUT} is regulated by varying the duration of the HS-FET's switch-off time, which automatically reduces f_{SW}.

The device is guaranteed to comply with the HS-FET's minimum on time. An advantage of this method is that the device works at the target f_{SW} for as long as possible, and f_{SW} only changes when the device operates at high input voltages. For more details, see the f_{SW} vs. V_{IN} curve on page 16. In this scenario, R_{FREQ} = 15kΩ, and V_{OUT} = 3.3V.

The Internal VCC (VCC)

The VCC capacitor (C3) is recommended to be 1µF.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses VIN as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation. When V_{IN} drops below 5V, the VCC output degrades.

Feedback (FB)

The feedback voltage is typically 0.8V, and its output can be adjusted. The external resistor divider connected to FB sets the output voltage (see Figure 7).

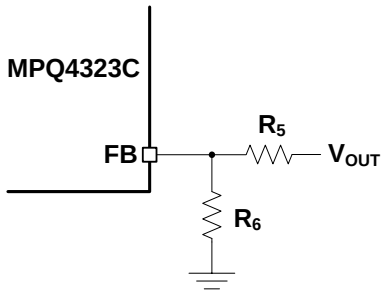


Figure 7: Feedback Divider Network (Adjustable Output Version)

Calculate R_6 with Equation (4):

$$R_6 = \frac{R_5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

For a fixed output, the FB resistor divider is integrated internally. This means that FB should be directly connected to the output to set the output voltage. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3.0V, 3.3V, 3.8V, and 5V (see Figure 8).

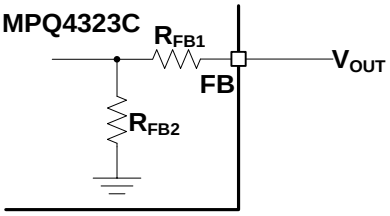


Figure 8: Feedback Divider Network of Fixed Output Version

Table 3 shows the relationship between the internal R_{FB} and V_{OUT}.

Table 3: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3	704	256
3.3	800	256
3.8	960	256
5	1344	256

Power Good (PG) Indication

The PG resistor (R7) should have a resistance of about 100kΩ.

The MPQ4323C includes an open-drain power good output that indicates whether the regulator output is within its nominal value window.

If using the PG pin, connect it to a logic high power source (e.g. 3.3V) via a pull-up resistor. PG goes high if the output voltage is within 94.5% to 105.5% of the nominal voltage; PG goes low if the output voltage is above 107% or below 93% of the nominal voltage. Float PG if it is not used.

Enable Control (EN) and Under-Voltage Lockout (UVLO)

EN is a digital control pin that turns the regulator on and off.

Enabled by External Logic High/Low Signal

When the EN voltage reaches 0.7V, BG does not turn on until V_{IN} exceeds 2.7V. BG then provides an accurate reference voltage for the EN threshold. Forcing EN above its rising threshold (about 1.02V) turns the device on. Turn the device off by driving EN below 0.85V. There is no internal pull-up or pull-down resistor connected to the EN pin, so do not float EN. An external pull-up or pull-down resistor is required if the control signal cannot give an accurate high or low logic.

Configurable V_{IN} Under-Voltage Lockout (UVLO)

The MPQ4323C has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.65V, while the falling threshold is about 2.9V. For applications that require a higher UVLO point, an external resistor divider can be placed between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 9).

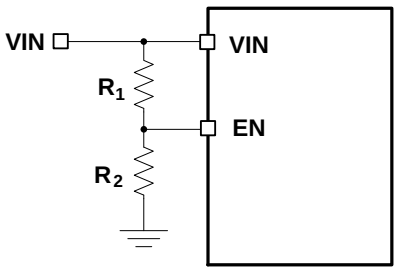


Figure 9: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (5) and Equation (6), respectively:

$$INUV_{RISING} = (1+\frac{R_1}{R_2}) \times V_{EN\_RISING} \quad (5)$$

$$INUV_{FALLING} = (1+\frac{R_1}{R_2}) \times V_{EN\_FALLING} \quad (6)$$

Where V_{EN_RISING} is 1.02V, and $V_{EN\_FALLING}$ is 0.85V.

If EN is not used to control when the device turns on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor and Output Capacitors (SW)

The inductor (L_1) value can be estimated with Equation (7):

$$L_1 = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current (I_{LP}) can be estimated with Equation (8):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Choose an inductor that does not saturate under the peak inductor current.

The output voltage ripple can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1-\frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductor value, and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

The output capacitor (C_{OUT}) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low.

For ceramic capacitors**,** the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting an output capacitor, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, the output capacitance can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^{2} \times L}{V_{OUT}^{2} \times ((V_{OUTMAX} / V_{OUT})^{2} - 1)} \quad (12)$$

Where V_{OUTMAX}/V_{OUT} is the allowable maximum overshoot. After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance value.

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4323C can be optimized for a wide range of capacitance and ESR values.

GND Connection (GND and PGND)

See the PCB Layout Guidelines on page 35 for more details.

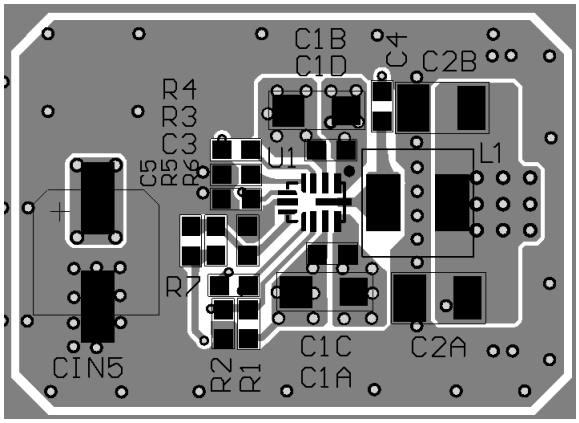
PCB Layout Guidelines [14]

An efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 10 and follow the guidelines below:

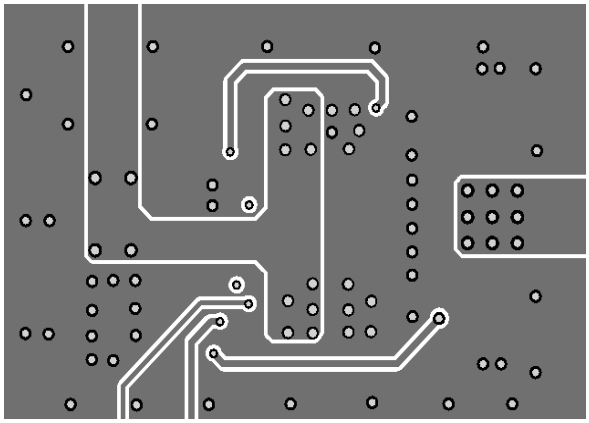
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BOOT away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

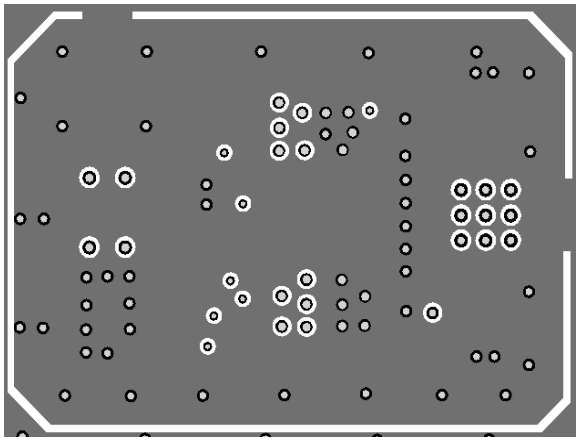
14) The recommended PCB layout is based on Figure 6 on page 30.



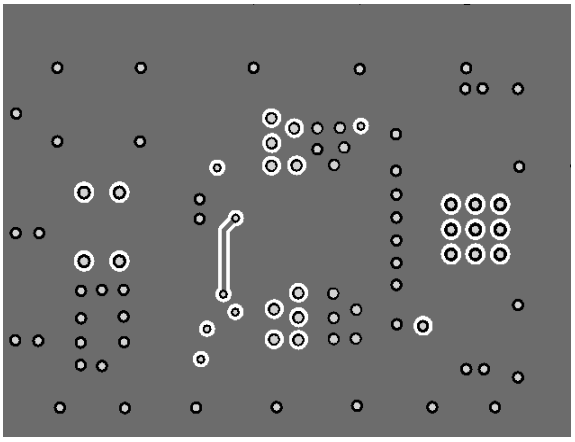
Top Silk and Top Layer



Mid-Layer 2



Mid-Layer 1



Bottom Layer and Bottom Silk

Figure 10: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

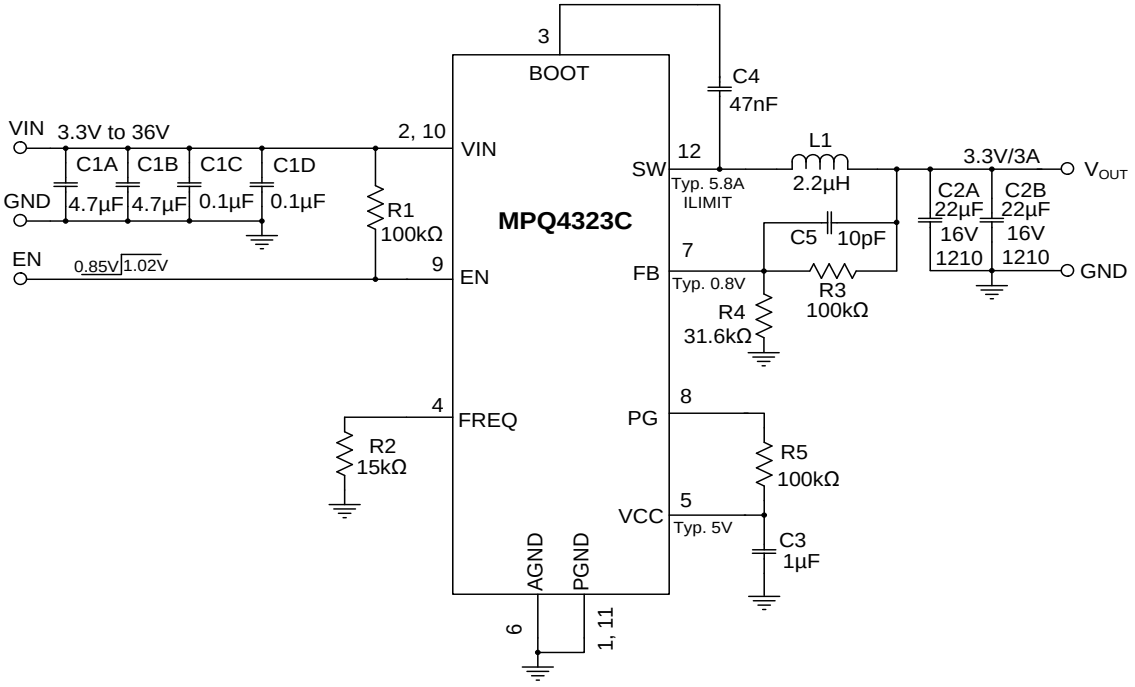


Figure 11: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz) with the QFN-12 Package

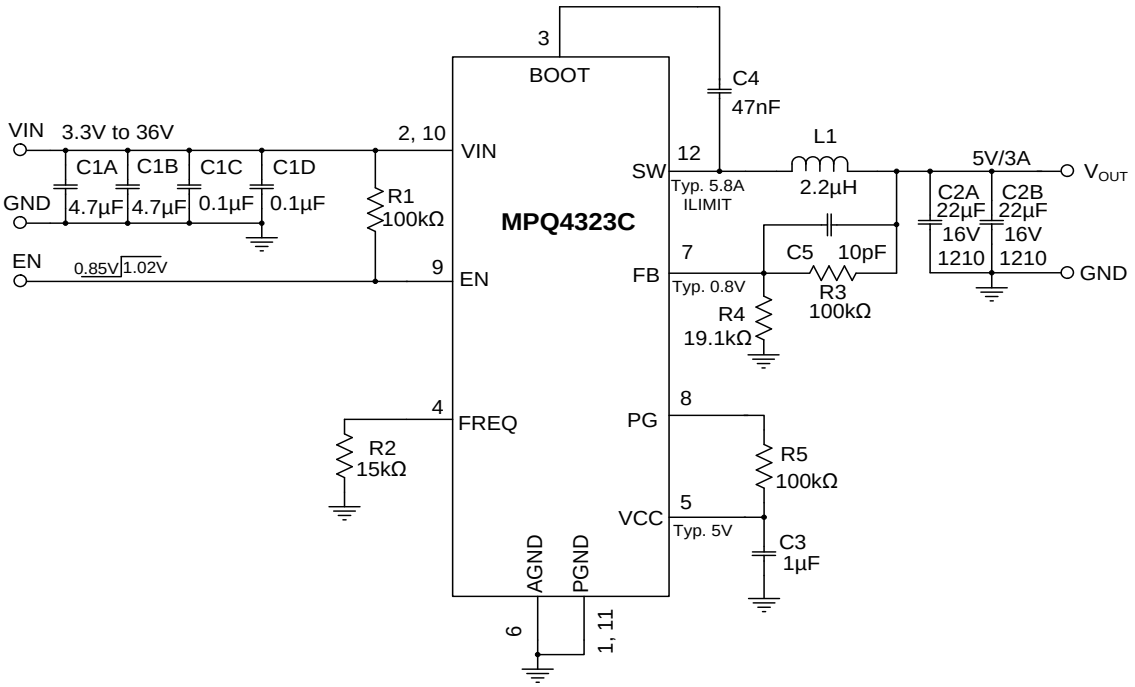


Figure 12: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz) with the QFN-12 Package

TYPICAL APPLICATION CIRCUITS *(continued)*

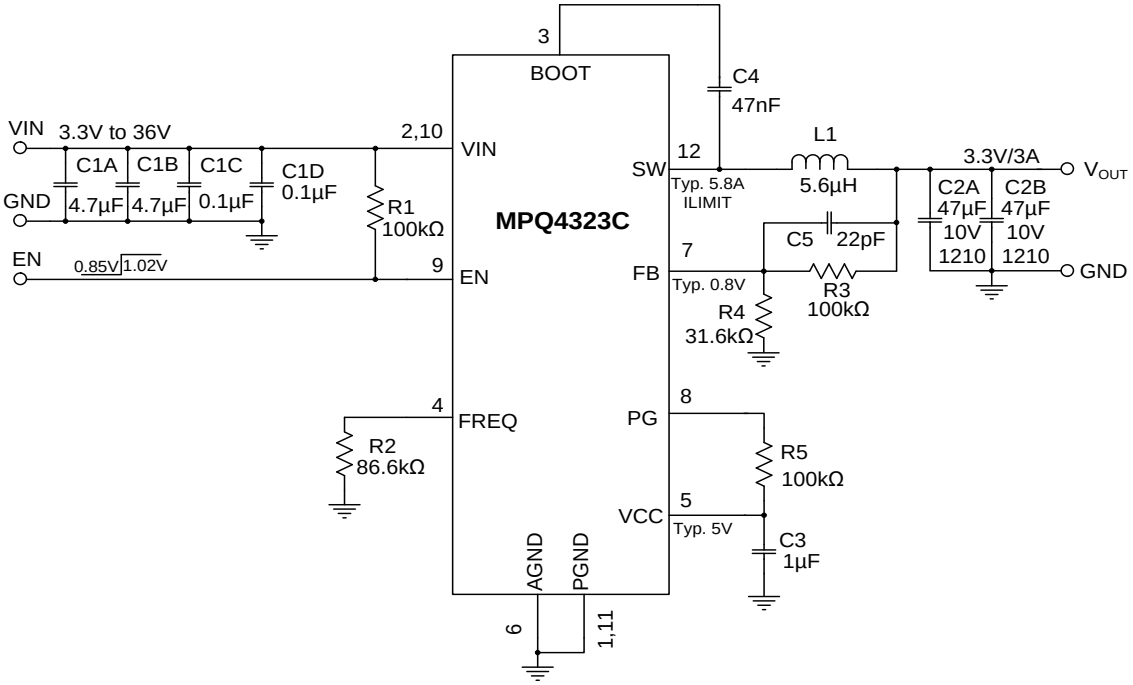


Figure 13: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 415kHz) with the QFN-12 Package

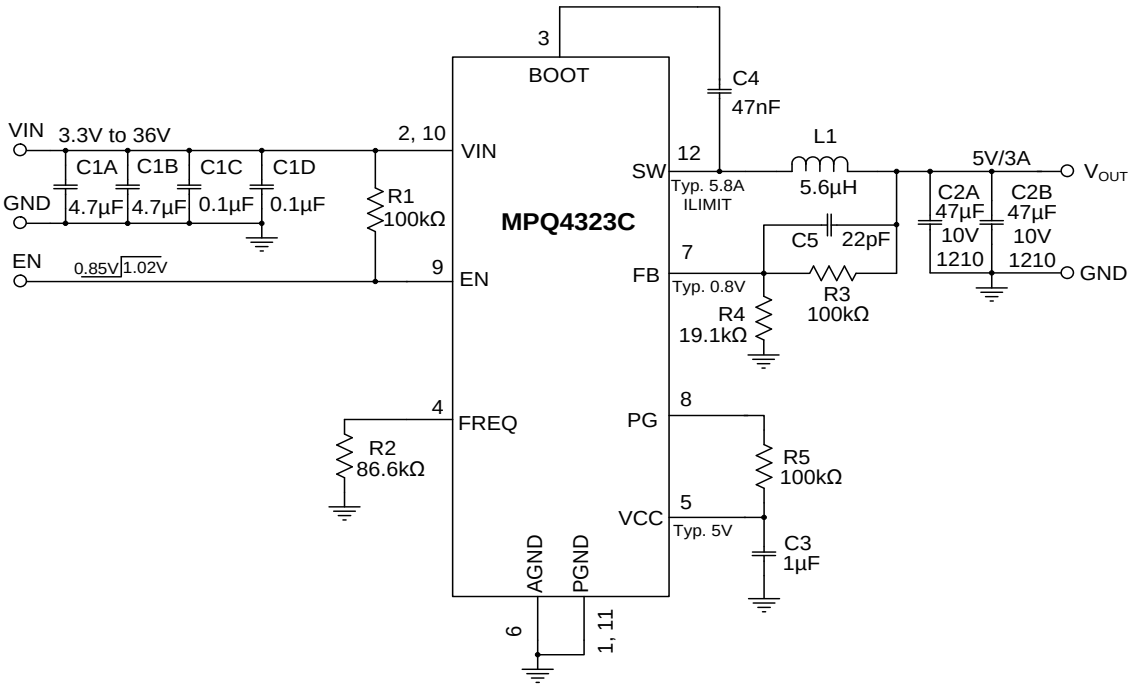


Figure 14: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz) with the QFN-12 Package

TYPICAL APPLICATION CIRCUITS *(continued)*

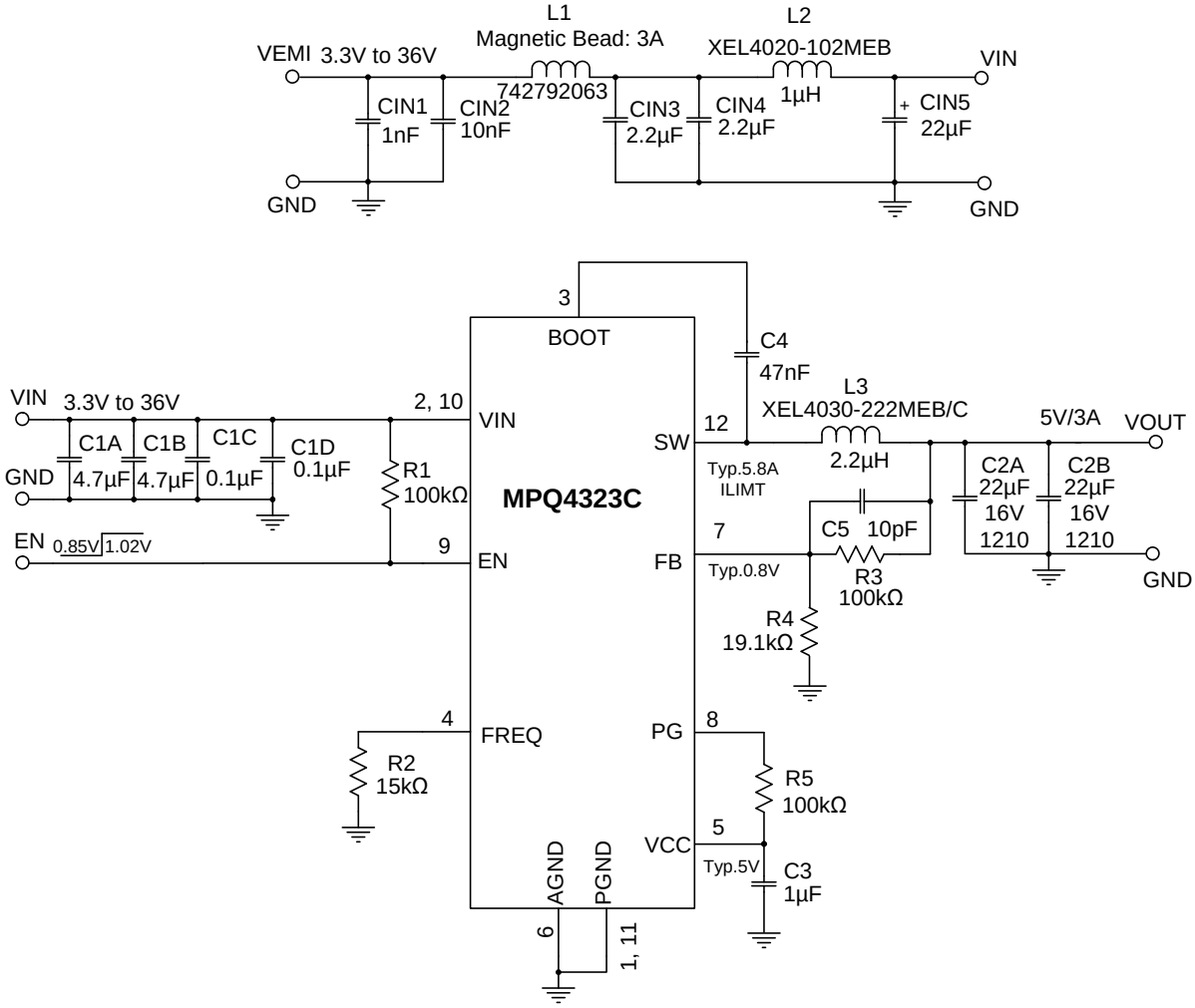


Figure 15: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters) with the QFN-12 (2mmx3mm) Package

TYPICAL APPLICATION CIRCUITS *(continued)*

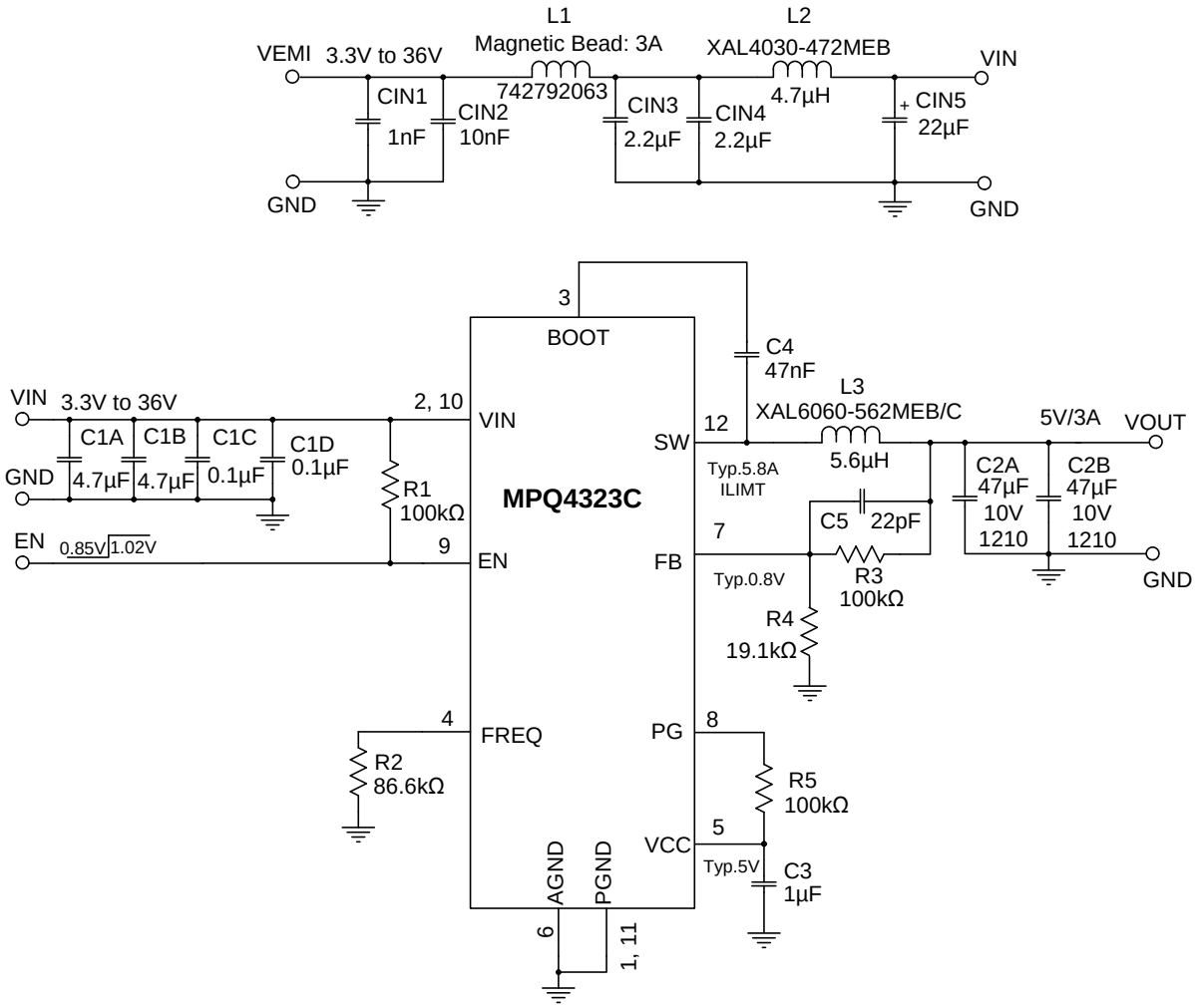
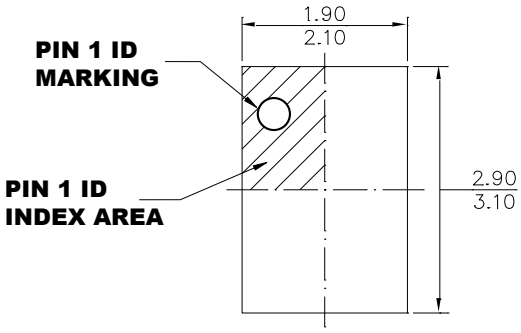


Figure 16: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 415kHz with EMI Filters) with the QFN-12 Package

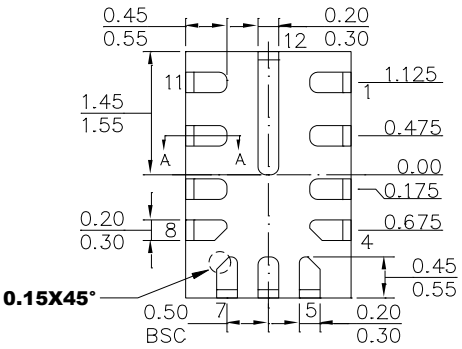
PACKAGE INFORMATION

QFN-12 (2mmx3mm)

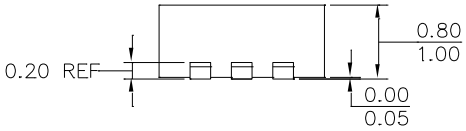
Wettable Flank



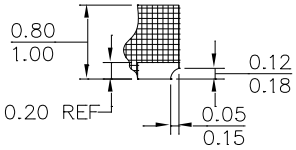
TOP VIEW



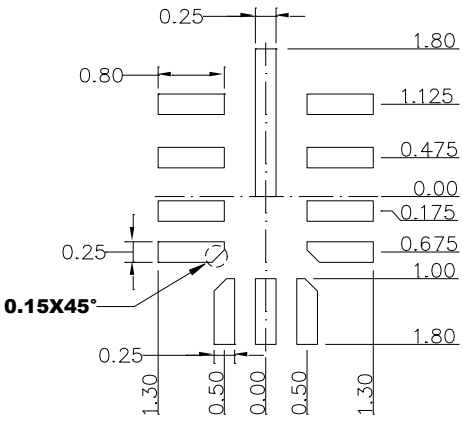
BOTTOM VIEW



SIDE VIEW



SECTION A-A



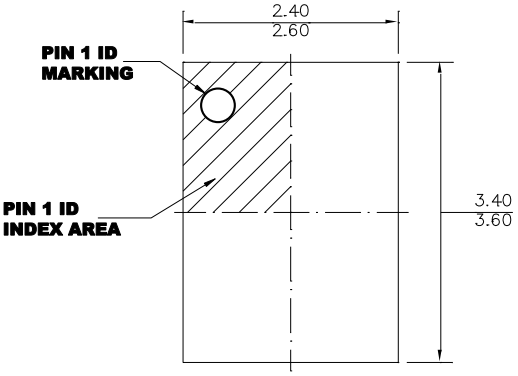
RECOMMENDED LAND PATTERN

NOTE:

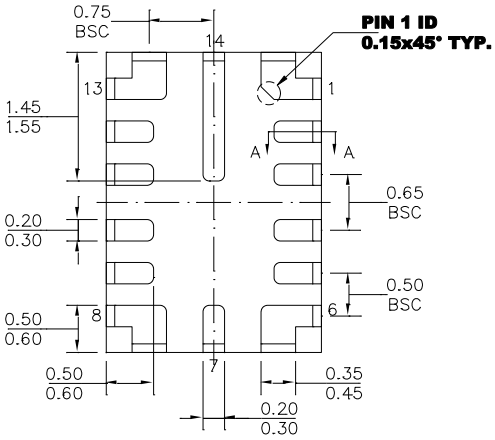
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

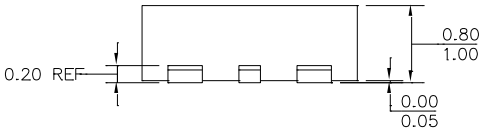
QFN-14 (2.5mmx3.5mm)
Wettable Flank



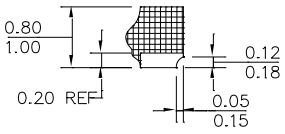
TOP VIEW



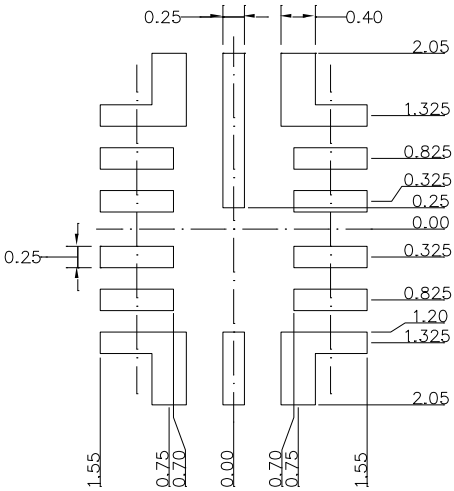
BOTTOM VIEW



SIDE VIEW



SECTION A-A



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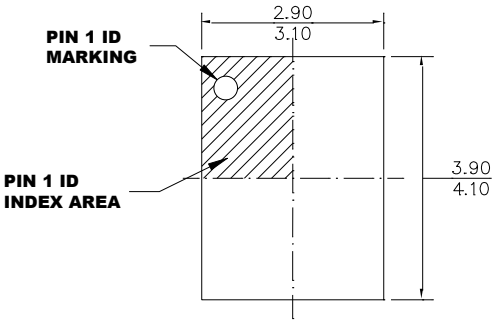
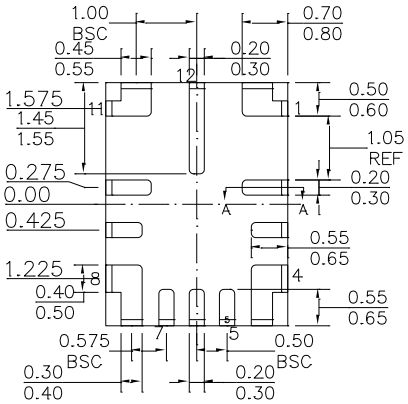
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

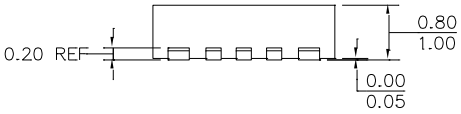
QFN-12 (3mmx4mm)
Wettable Flank



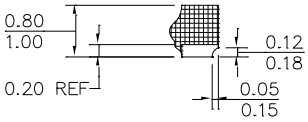
TOP VIEW



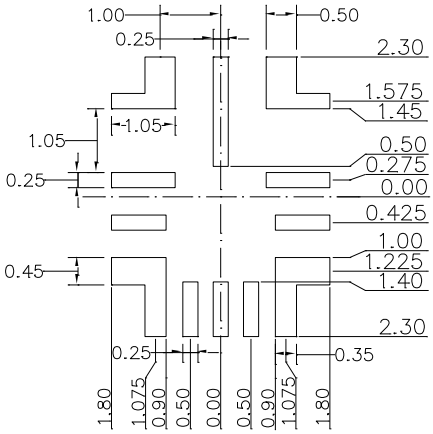
BOTTOM VIEW



SIDE VIEW



SECTION A-A



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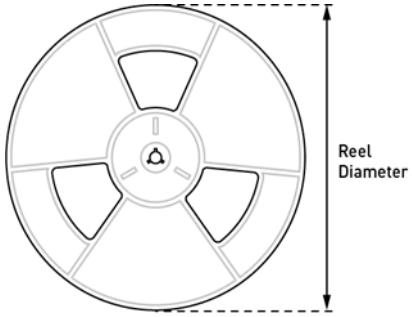
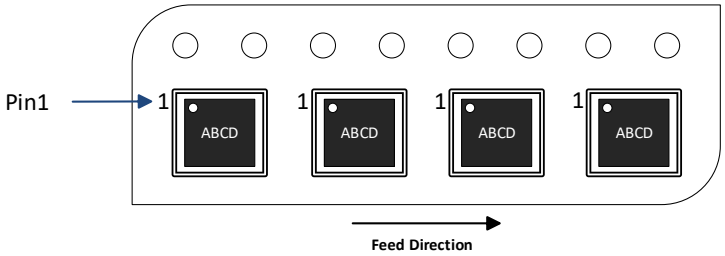
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4323CGDE-AEC1-Z	QFN-12 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4323CGRHE-AEC1-Z	QFN-14 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4323CGLE-AEC1-Z	QFN-12 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/27/2022	Initial Release	-
1.1	5/15/2023	Removed “(Absolute maximum)” in Features section; added QFN-12 (3mmx4mm) package	1
		Removed the MPQ4323CGRHE-5-AEC1 and MPQ4323CGRHE-33-AEC1 SKUs from Ordering Information and Top Marking sections; added new MPQ4323CGLE-AEC1 SKU to Ordering Information and Top Marking sections; added QFN-12 (3mmx4mm) package	3–4
		Updated the minimum start-up V_{IN} from “3.8V” to “3.9V”, making it the same as the UVLO rising max value; added detail description about θ_{JC} in note 7, note 8, note 9, and note 10; minor formatting updates; added QFN-12 (3mmx4mm) package and its thermal information	6
		Updated note numbers	6–35
		Updated “PG rising/falling delay” to “PG rising/falling deglitch time”	8
		Added two Case Thermal Rise curves for QFN-12 (3mmx4mm) package	15
		Updated figure number and page number references for note 12 and note 13	18, 20
		Updated C4 from “100nF” to “47nF” and updated titles for Figure 6, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, Figure 19, and Figure 20	30, 36–41
		Updated recommended C_{BOOT} to “22nF to 100nF”; updated “P-channel MOSFET” to “N-channel MOSFET”	31
		Updated page number references in Setting the Switching Frequency (FREQ) section	31–32
		Minor formatting updates	35
		Removed typical application circuits for fixed-output version (previously Figure 13, Figure 14, Figure 17, and Figure 18)	37–41
		Added QFN-12 (3mmx4mm) package and POD	44
		Removed the MPQ4323CGRHE-5-AEC1 and MPQ4323CGRHE-33-AEC1 SKUs from Carrier Information section; added new MPQ4323CGLE-AEC1 SKU to Carrier Information section	45
1.2	7/10/2024	• Changed the recommended operating condition V_{OUT} max to 6V • Add note 7: “Higher voltages are possible. Contact MPS for application recommendations.”	6
		Updated note numbers	6–8, 17–20, 35

1.3	9/16/2024	• Removed note 7 • Updated Recommended Operating Conditions section: updated V_{OUT} max to “0.95 x V_{IN}”	6
		• Updated the typical value of LS reverse current limit to 1.8A in the Electrical Characteristics table and the Reverse Current Limit section	8, 29
		Updated note numbers	6–8, 17–20, 35