MPM3612-33

3V to 22V Input, 1A, Ultra-Low 5µA I_Q, Power Module in an LGA-10 (3mmx3mmx2mm) Package

DESCRIPTION

The MPM3612-33 is a synchronous, rectified, step-down switch-mode converter with built-in internal power MOSFETs and high light-load efficiency. The MPM3612-33 has an ultra-low 5µA quiescent current (I_Q). The MPM3612-33 offers a very compact solution that achieves 1A of continuous output current (I_{OUT}) with excellent load and line regulation across a wide input supply range.

The MPM3612-33's switching edge is optimized to reduce electromagnetic interference (EMI). Constant-on-time (COT) control provides seamless mode transitions and a fast load transient response.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown.

The MPM3612-33 requires a minimal number of readily available, standard external components, and is available in a space-saving LGA-10 (3mmx3mmx2mm) package.

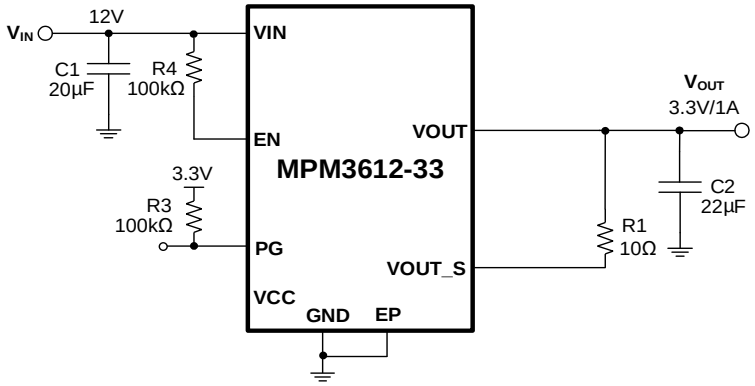
FEATURES

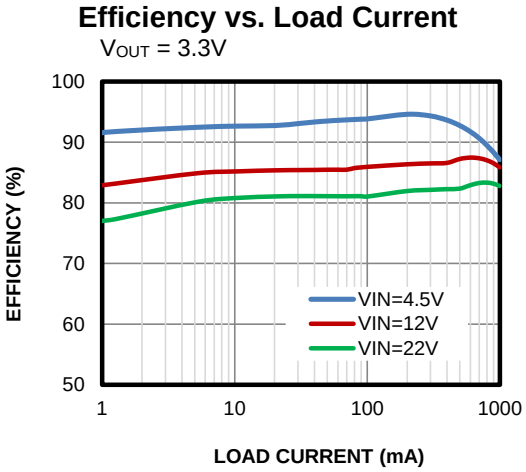
- Wide 3V to 22V Operating Input Voltage (V_{IN}) Range
- 5µA Low Quiescent Current (I_Q)
- 1A Load Current
- High Efficiency from 100µA to 1A Load when V_{IN} is 4V to 22V
- Power-Save Mode (PSM)
- 1.25MHz Fixed Switching Frequency (f_{SW}) during Continuous Conduction Mode (CCM)
- On Time (t_{ON}) Extension to Support Large Duty Cycles
- Power Good (PG) Indication
- EN Shutdown Output Discharge
- Over-Current Protection (OCP) and Over-Voltage Protection (OVP) with Hiccup Mode
- Fixed 3.3V Output Voltage (V_{OUT})
- Available in an LGA-10 (3mmx3mmx2mm) Package

APPLICATIONS

- Internet-of-Things (IoT) Devices
- Home Automation, Home Security
- Single-Cell or Multi-Cell Li-Ion Battery Systems
- Multi-Cell Dry Battery Systems
- Sever Power

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3612GLQ-33	LGA-10 (3mmx3mmx2mm)	*See Below*	3

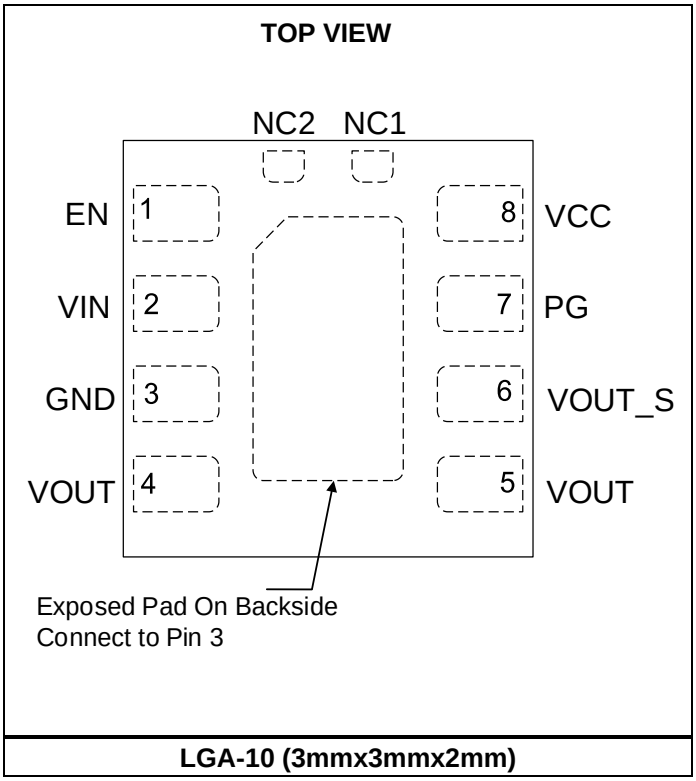
* For Tape & Reel, add suffix -Z (e.g. MPM3612GLQ-33-Z).

TOP MARKING

BNTY
LLLL

BNT: Product code of MPM3612GLQ-33
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



LGA-10 (3mmx3mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable control pin.** Do not float the EN pin. Apply a logic high voltage on this pin to enable the MPM3612-33; pull EN to logic low to disable the MPM3612-33.
2	VIN	**Supply voltage.** The MPM3612-33 operates from a 3V to 22V input rail. A capacitor (C1) is required to decouple the input rail. Use a wide PCB trace or multiple vias to make the VIN connection.
3	GND	**System ground.** The GND pin is the reference ground for the regulated output voltage and requires special consideration during PCB layout.
4, 5	VOUT	**Module voltage output node**
6	VOUT_S	**Output voltage sense.**
7	PG	**Power good output.** The PG pin is an open drain that can indicate over-voltage (OV) and under-voltage (UV) conditions.
8	VCC	**Internal 3.3V LDO output.** The driver and control circuits are powered from the voltage on the VCC pin.
NC1	NC1	**Not connect pin 1.** The NC1 pin cannot be connected to NC2.
NC2	NC2	**Not connect pin 2.** The NC2 pin cannot be connected to NC1.
EP	EP	**Exposed pad.** The exposed pad on backside should be connected to pin 3.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{EN}, V_{OUT} .....-0.3V to +24V
V_{SW}.....-0.3V (-5V <10ns) to +24V (+28V <10ns)
V_{BST} ..... V_{SW} + 4V
V_{PG} / V_{OUT_S} 6.5V
All other pins .....-0.3V to +4.3V
Continuous power dissipation (T_A = 25°C) (2)
..... 1.78W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM)..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN})……3V to 22V
Output voltage (V_{OUT})..... 3.3V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) (5) (6) (7)

LGA-10 (3mmx3mmx2mm)
θ_{JA}……70.3°C/W
θ_{JC_TOP}……34.9°C/W
θ_{JB}……54.9°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) -T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produces an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is the junction-to-case top thermal characterization parameter, and θ_{JB} is the junction-to-board thermal characterization parameter.
5) The thermal parameter is based on testing on the MPS evaluation board (EVM3612-LQ-00A) under no airflow cooling conditions in a standard enclosure. The board size is 6.4cmx6.4cm, 2 layers. For the top and bottom layer, the copper thickness is 2oz.
6) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on equation $T_J = \theta_{JC\_TOP} \times P_{LOSS} + T_{CASE\_TOP}$, where P_{LOSS} is the entire loss of module at real application, T_{CASE_TOP} is the case top temperature.
7) The junction-to-board thermal characterization parameter, θ_{JB}, is an estimation of the junction temperature in the real system, based on equation $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the entire loss of module at real application, and T_{BOARD} is the board temperature.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN_SD}				2	µA
Supply current (quiescent)	I_Q	V_{FB} = 0.7V		5	9	µA
High-side (HS) switch on resistance	$R_{DS(ON)\_HS}$			260	450	mΩ
Low-side (LS) switch on resistance	$R_{DS(ON)\_LS}$			120	200	mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{IN} = 22V, T_J = 25°C, V_{SW} = 0V and 22V			1	µA
LS valley current limit	I_{VALLEY}		1.15	1.4	1.65	A
LS sink current limit [9]	I_{LSSINK}	OVP or output discharge		-600		mA
Internal inductor (L) value	L			2.2		µH
Internal inductor DCR	L_{DCR}	T_J = 25°C		200		mΩ
Switching frequency	f_{SW}	V_{OUT} = 3.3V, in CCM	-10%	+1250	+10%	kHz
Minimum off time [9]	t_{OFF_MIN}			140		ns
Minimum on time [9]	t_{ON_MIN}			40		ns
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV	96	98		%
Output voltage	V_{OUT}	T_J = -40°C to +125°C	-1%	+3.3	+1%	V
Feedback current	I_{FB}	V_{FB} = 620mV		10	50	nA
Output over-voltage protection (OVP) rising	V_{OVP_R}		115%	120%	125%	V_{REF}
Output OV deglitch time [9]	t_{OVP}			8		µs
Output OVP recovery	V_{OVP_F}		105%	110%	115%	V_{REF}
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_VTH}$		2.63	2.80	2.97	V
V_{IN} UVLO threshold hysteresis	$V_{IN\_UVLO\_HYS}$			170		mV
Soft-start period	t_{SS}	10% to 90% of V_{OUT}	1	1.3	1.6	ms
VCC voltage	V_{CC}	I_{CC} = 2.5mA	3.1	3.3	3.5	V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0mA to 5mA	0.1	0.5	0.9	%
Thermal shutdown [9]	T_{STD}			150		°C
Thermal hysteresis [9]	T_{HYS}			20		°C
EN rising threshold	V_{EN_R}		1.05	1.20	1.35	V
EN hysteresis	V_{EN_F}			150		mV
EN input current	I_{EN}	V_{EN} = 2V			0.1	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good (PG) UV rising	$V_{PG\_UV\_R}$		87%	92%	97%	V_{REF}
PG UV falling	$V_{PG\_UV\_F}$		82%	87%	92%	V_{REF}
PG OV rising	$V_{PG\_OV\_R}$		108%	113%	118%	V_{REF}
PG OV falling	$V_{PG\_OV\_F}$		103%	108%	113%	V_{REF}
PG rise delay	$t_{PG\_R\_DLY}$			120		µs
PG falling delay	$t_{PG\_F\_DLY}$			50		µs
Power good sink current capability	V_{PG_SINK}	Sink 1mA			0.4	V

Notes:

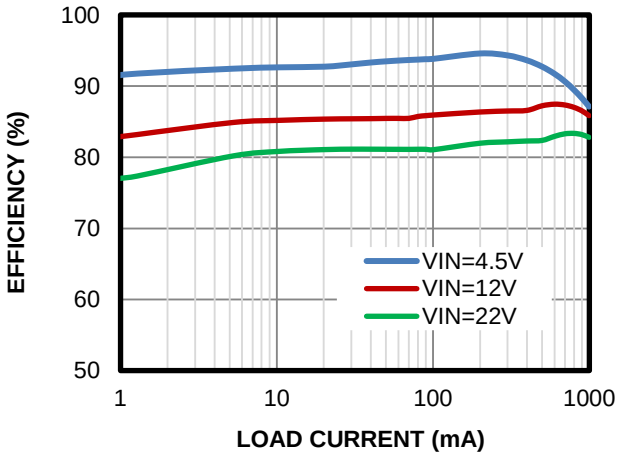
8) Not tested in production. Guaranteed by over-temperature correlation.
9) Guaranteed by design and engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

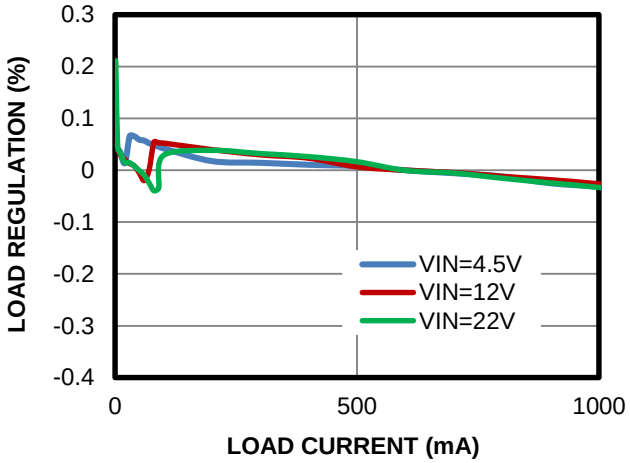
Efficiency vs. Load Current

V_{OUT} = 3.3V



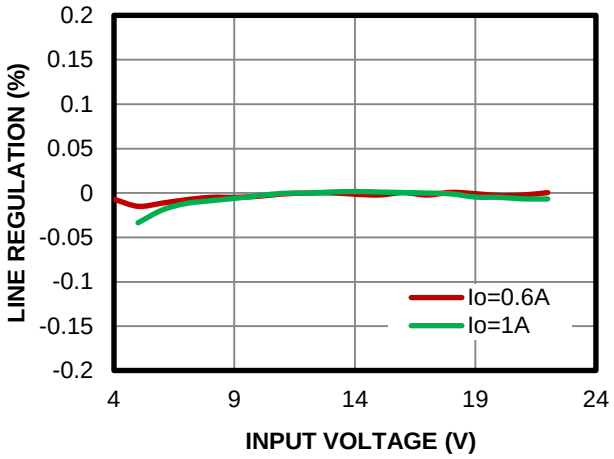
Load Regulation vs. Load Current

V_{OUT} = 3.3V



Line Regulation vs. Input Voltage

V_{OUT} = 3.3V

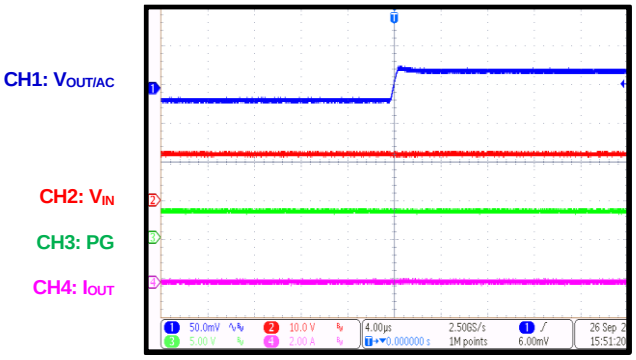


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

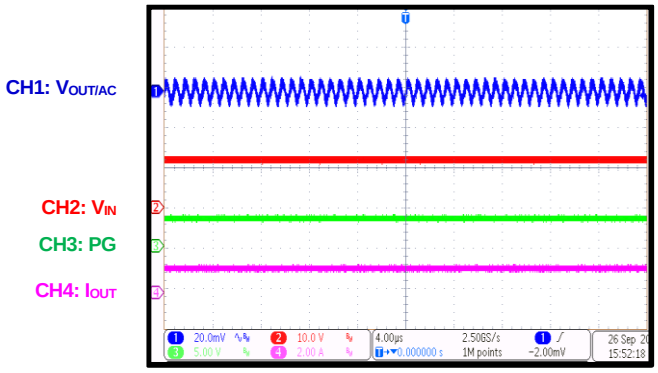
Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



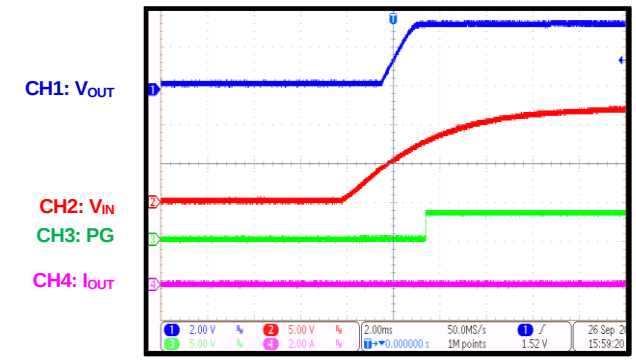
Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



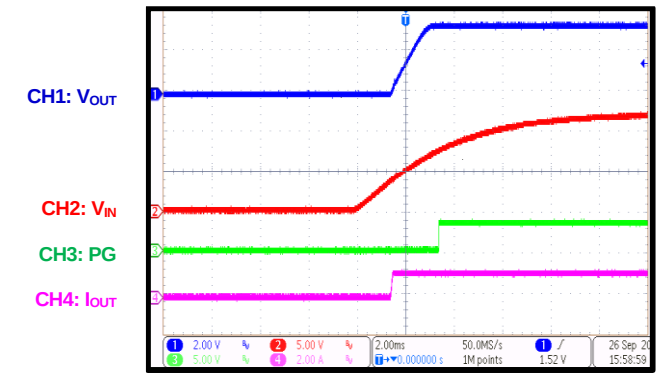
Start-Up through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



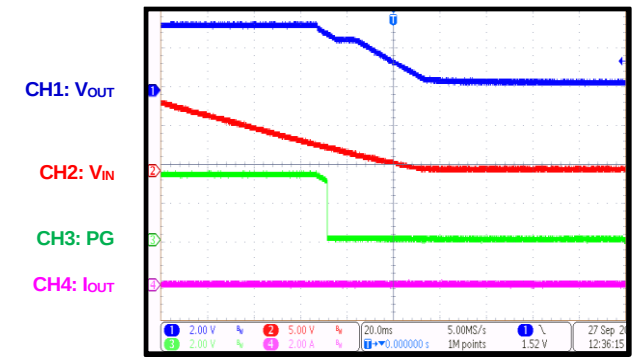
Start-Up through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



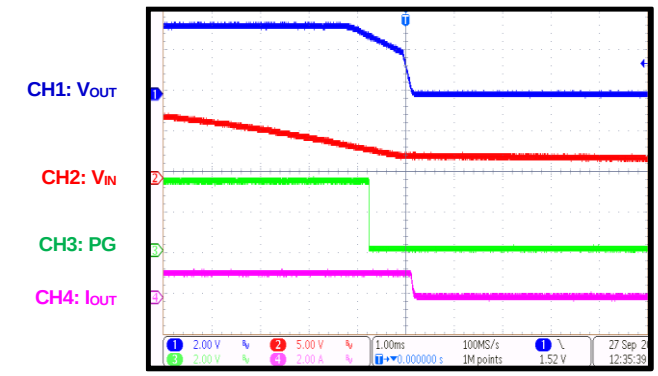
Shutdown through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



Shutdown through VIN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A

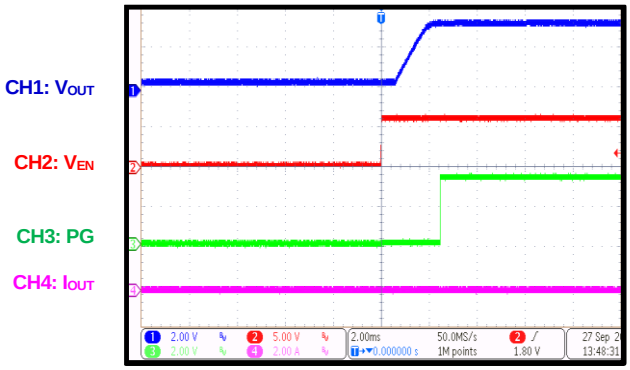


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

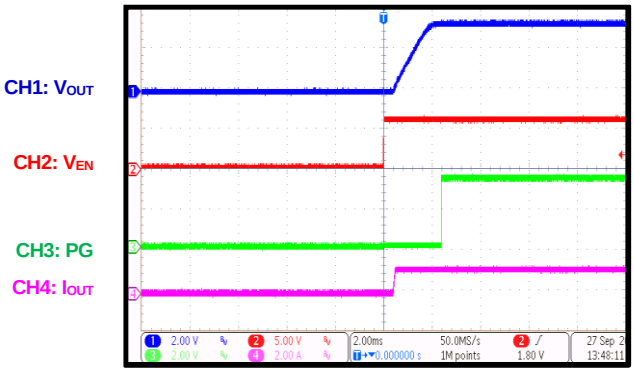
Start-Up through EN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



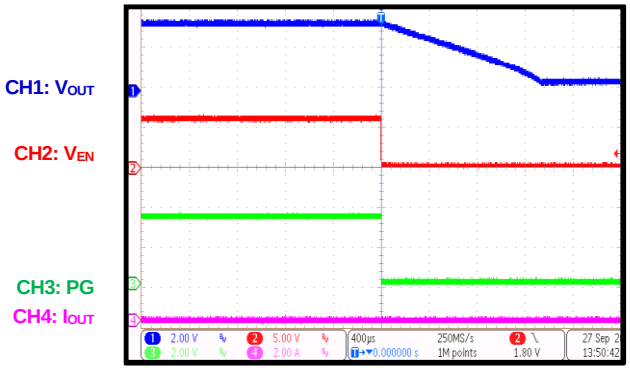
Start-Up through EN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



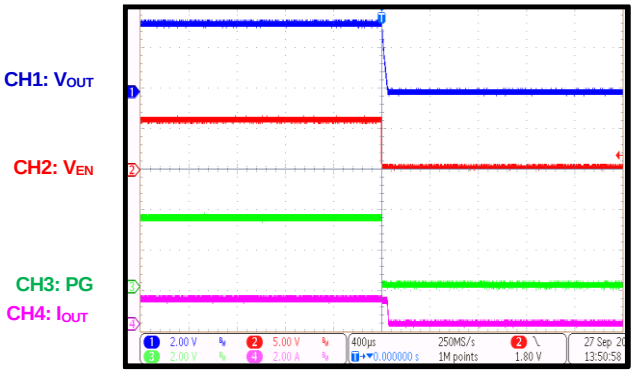
Shutdown through EN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



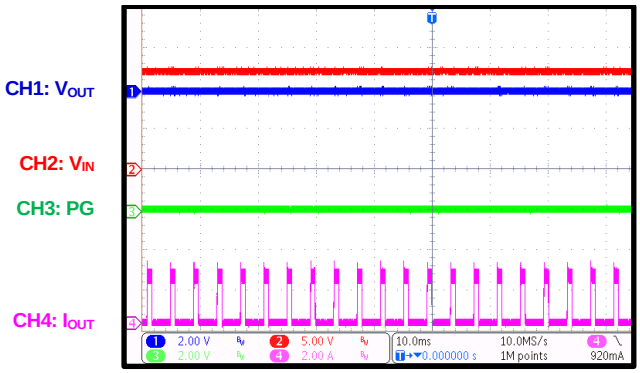
Shutdown through EN

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



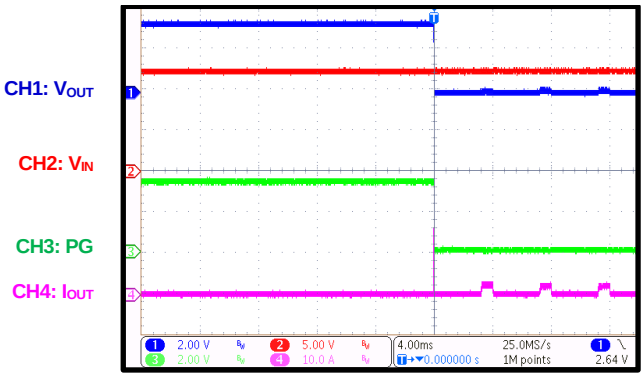
SCP Steady State

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



SCP Entry

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

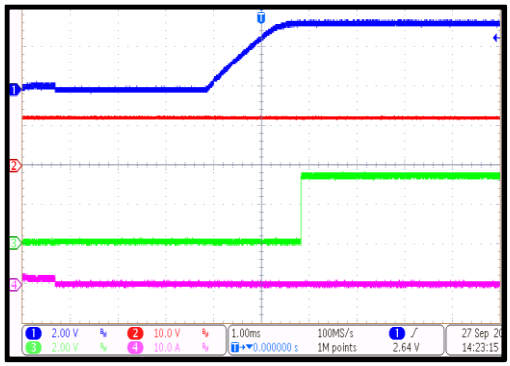


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

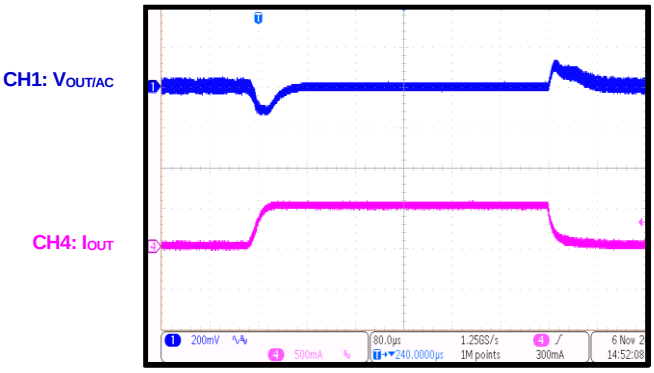
SCP Recovery

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



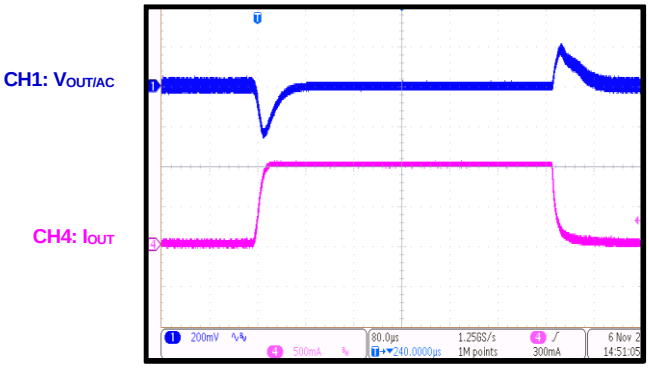
Load Transient Response

0.8A/µs, 0A to 0.5A, V_{IN} = 12V, V_{OUT} = 3.3V



Load Transient Response

0.8A/µs, 0A to 1A, V_{IN} = 12V, V_{OUT} = 3.3V

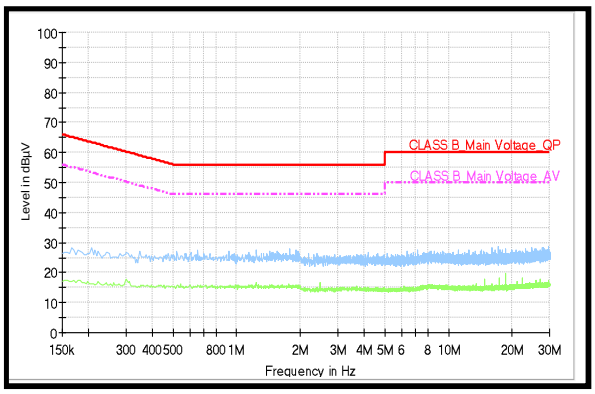


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

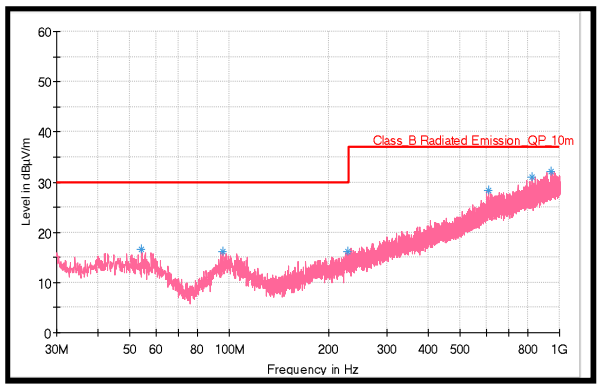
Conducted Emission, EN55022 Class B

MPM3612-33, V_{OUT} = 3.3V,
input PI filter: 8.8μF, 2.2μF, 8.8μF, 2.2μH

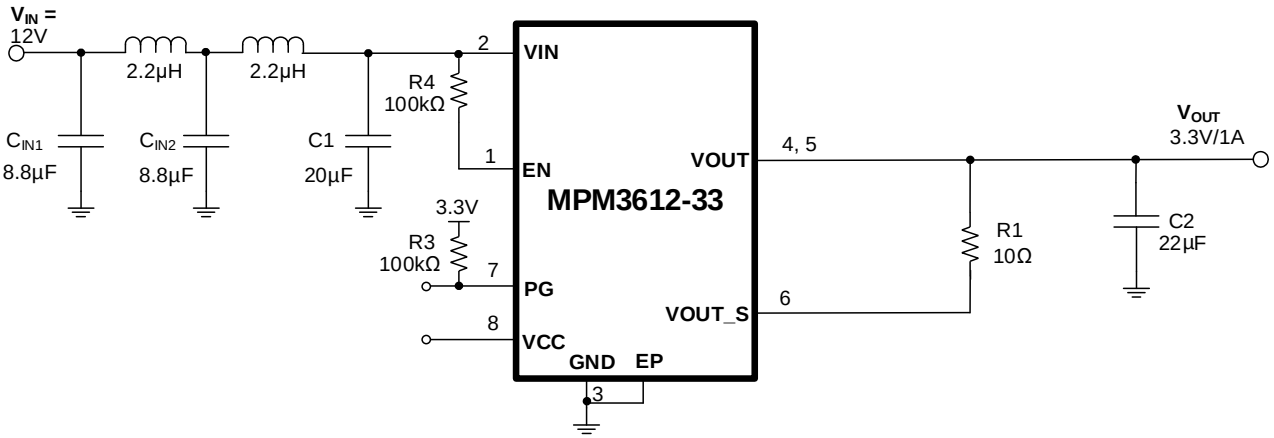


Radiated Emission, EN55022 Class B

MPM3612-33, V_{OUT} = 3.3V,
input PI filter: 8.8μF, 2.2μF, 8.8μF, 2.2μH



EMI TEST CIRCUIT



FUNCTIONAL BLOCK DIAGRAM

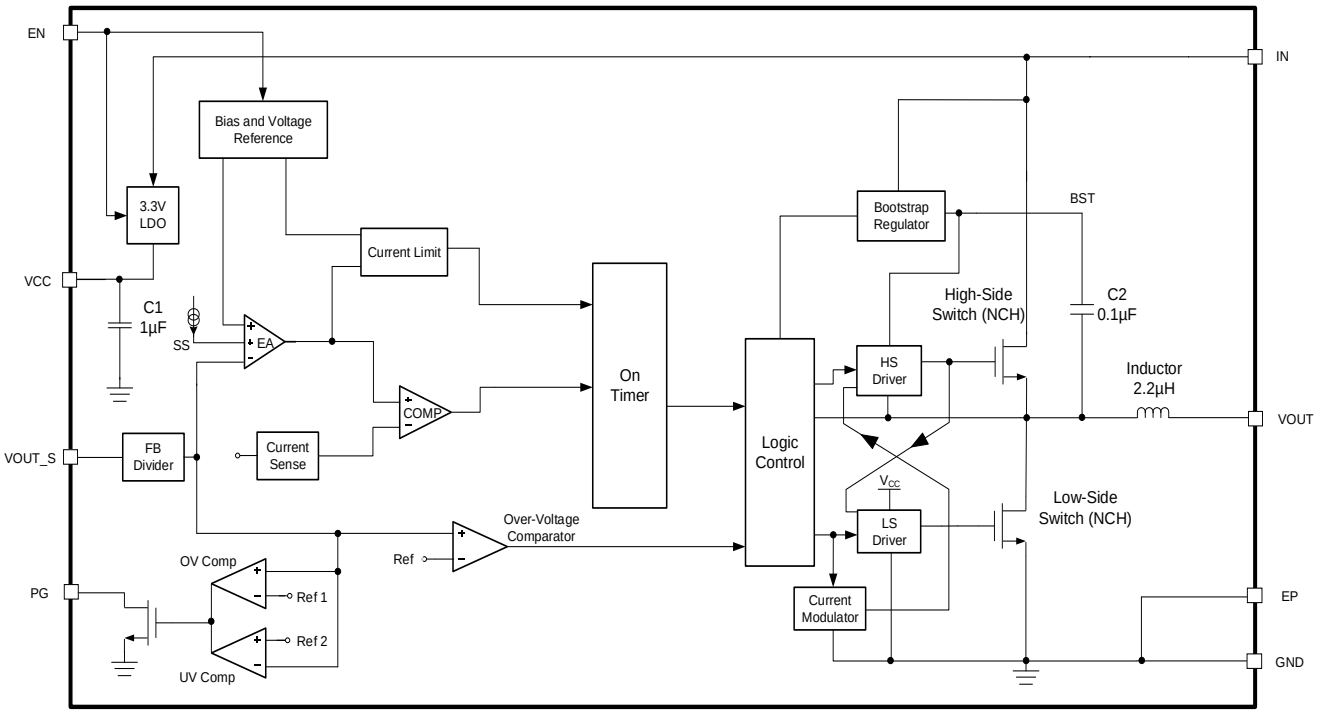


Figure 1: Functional Block Diagram

OPERATION

The MPM3612-33 is a low quiescent current (I_Q), fully integrated, synchronous, rectified step-down module. It offers a very compact solution to achieve 1A of output current (I_{OUT}) across a wide input supply range with excellent efficiency.

Pulse-Width Modulation (PWM) Operation

The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. Figure 2 shows the MPM3612-33's simplified ramp compensation block.

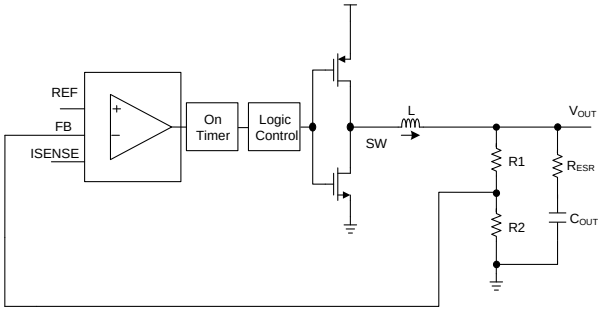


Figure 2: Simplified Control Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ISENSE ramp (V_{ISENSE}) is below the error amplifier's output voltage (V_{EAO}), which indicates insufficient output voltage (V_{OUT}).

After the on period elapses, the HS-FET turns off. By cycling HS-FET between its on and off states, the device regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET turn on at the same time, causing a dead short between the input and GND. Shoot-through dramatically reduces efficiency, and the MPM3612-33 avoids this by internally generating a dead time (DT) between when the HS-FET is off and the LS-FET is on, and vice versa. The device enters either heavy-load operation or light-load operation depending on I_{OUT}.

Light-Load Operation

When the MPM3612-33 works under light-load conditions, the MPM3612-33 automatically reduces the switching frequency (f_{SW}) to maintain high efficiency, and the inductor current (I_L) drops to almost zero. Once I_L reaches zero, the LS-FET driver goes into tri-state (Hi-Z). The current modulator controls the LS-FET and limits I_L to around 0A (see Figure 3). The output capacitors discharge slowly to GND through the LS-FET and feedback resistors (R1 and R2). This operation greatly improves efficiency when I_{OUT} is low.

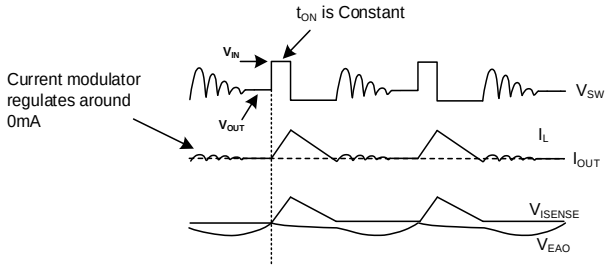


Figure 3: Light-Load Operation

Light-load operation is also called pulse-skip mode because the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of I_{OUT}; as I_{OUT} increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. This also increases f_{SW}.

I_{OUT} reaches its critical level when the current modulator time changes to zero, calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The MPM3612-33 reverts to PWM mode once I_{OUT} exceeds the critical level. Then f_{SW} stays constant across the I_{OUT} range.

VCC Regulator

An internal 3.3V regulator powers most of the internal circuitries. This regulator takes the VIN input and operates across the full V_{IN} range. When V_{IN} exceeds 3.3V, the regulator's output is in full regulation. When V_{IN} is below 3.3V, V_{OUT} decreases and follows V_{IN}.

Soft Start (SS)

The MPM3612-33 employs a soft start (SS) mechanism to ensure smooth output during start-up. When the MPM3612-33 is enabled and the BST voltage reaches its rising threshold, and an internal current source starts to charge up the internal SS capacitor.

The SS capacitor voltage takes over the reference voltage (V_{REF}) to the PWM comparator. V_{OUT} smoothly ramps up with the SS voltage (V_{SS}). Once V_{SS} exceeds V_{REF}, V_{SS} continues to ramp up while the PWM comparator only compares V_{REF} and the FB voltage (V_{FB}). At this point, SS finishes, and the device enters steady state operation.

The internal soft-start time is set at a fixed 1.3ms (for V_{OUT} to rise from 10% to 90%). The output capacitance should not exceed 470μF to avoid triggering the current limit during start-up.

Pre-Biased Start-Up

The MPM3612-33 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the internal soft-start capacitor should also be charged. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed V_{OUT} at the VOUT_S pin, the MPM3612-33 starts to operate normally.

Power Good (PG)

The MPM3612-33 has a power good (PG) output to indicate whether V_{OUT} is ready. The PG pin is an open-drain output. Connect PG to VCC or another voltage source via a pull-up resistor (e.g. 100kΩ). When V_{IN} is applied, the PG pin pulls down to GND before V_{SS} reaches 1V. Once V_{SS} reaches 1V and V_{FB} exceeds 92% of V_{REF}, there is a 120μs delay and PG pulls high. During normal operation, PG pulls low if V_{FB} drops below 87% of V_{REF} (after a 50μs delay).

If under-voltage lockout (UVLO) or over-temperature protection (OTP) occurs, or EN goes low, the PG pin pulls low immediately. If over-current protection (OCP) occurs and V_{FB} drops below 87% of V_{REF}, there is a 50μs delay and PG pulls low.

PG also indicates whether an output over-voltage (OV) condition has occurred. If V_{OUT} exceeds 113% of the V_{REF} rising threshold, PG pulls low. If V_{OUT} falls below 108% of the V_{REF} falling threshold, PG pulls high again. The PG deglitch timer is 120μs and 50μs for the rising and falling thresholds, respectively. This threshold is below the OVP discharge threshold.

Low-Dropout Mode

To improve dropout, the MPM3612-33 is designed to extend the on time (t_{ON}) when the minimum off time is triggered. The HS-FET on time is extended and f_{SW} drops. The typical minimum frequency is 240kHz. When the frequency drops to 240kHz, the duty cycle reaches its maximum (D_{MAX}) because the on time is at its maximum value. If V_{IN} continues to drop, the MPM3612-33 operates at 240kHz and V_{OUT} drops.

D_{MAX} can be estimated with Equation (2):

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW\_MIN} \quad (2)$$

Where t_{OFF_MIN} = 140ns, and f_{SW_MIN} = 240kHz.

Output Over-Voltage Protection (OVP)

The MPM3612-33 monitors V_{OUT} and enters OVP discharge mode if V_{OUT} exceeds 120% of the regulation voltage for longer than 8μs. In OVP discharge mode, the LS-FET turns on and stays on until the LS-FET current reaches its negative current limit. Then the output discharges to keep V_{OUT} within a normal range. If the V_{OUT} OV conditions remains, the LS-FET turns on again after a fixed delay to repeat the discharge behavior.

The MPM3612-33 exits this discharge mode when V_{FB} drops below 110% of V_{REF}.

If V_{IN} exceeds 24V (the input OVP threshold) during OVP discharge mode, the MPM3612-33 shuts down until V_{IN} drops below 22V, then restarts again. This input OVP function is only active during output OV conditions.

Output Discharge

The MPM3612-33 provides a discharge function that provides an active discharge path for the external output capacitor. This function is active when the part is disabled via EN (EN is pulled low). When EN is disabled, the HS-FET turns off and the LS-FET turns on to discharge V_{OUT}. When the LS-FET current reaches the negative current limit, the LS-FET turns off. After a fixed time delay, the LS-FET turns on again. This behavior repeats until FB goes low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM3612-33 has valley current limit control. While the LS-FET is on, I_L is monitored. When the sensed I_L exceeds the valley current limit threshold, the device enters over-current protection (OCP). The HS-FET cannot turn on until I_L falls below the valley current limit. Meanwhile, V_{OUT} drops until it falls below the under-voltage (UV) threshold (typically 60% below V_{REF}).

Once the UV and OC conditions are both triggered, the MPM3612-33 enters hiccup mode to periodically restart the part. The hiccup duty cycle is very small to reduce power dissipation during the short-circuit condition.

During OCP, the device tries to recover from the OC fault with hiccup mode. This means that the device disables the output power stage, discharges the soft-start capacitor, and then automatically tries to initiate a soft start again. If the OC condition still exists when soft start finishes, the device repeats this operation. OCP is non-latch protection.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn the regulator off. Do not float the EN pin. The EN pin can survive with a 22V V_{IN}, which means the EN and VIN pins can be connected for automatic start-up.

Under-Voltage Lockout (UVLO)

The MPM3612-33 has UVLO. When V_{IN} exceeds the UVLO rising threshold voltage, the MPM3612-33 starts up. The device shuts down when V_{IN} falls below the UVLO falling threshold.

Thermal Shutdown

The MPM3612-33 employs thermal shutdown by internally monitoring its junction temperature (T_J). If T_J exceeds the 150°C threshold, the device shuts off. This is non-latch protection. There is a 20°C hysteresis. Once T_J drops about 130°C, the device initiates a soft start.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current can be calculated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, estimated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Under the worst-case conditions, V_{IN} = 2 x V_{OUT}, estimated with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The output voltage ripple caused by the equivalent series resistance (ESR) is very small. When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency.

In addition to considering the output ripple, choosing a larger-value output capacitor can improve load transient response, but the maximum output capacitor limit should also be considered in design application. If the output capacitance is too high, V_{OUT} cannot reach the design value during the soft-start time, and then the MPM3612-33 fails to regulate. The maximum output capacitor value (C_{O_MAX}) can be calculated with Equation (9):

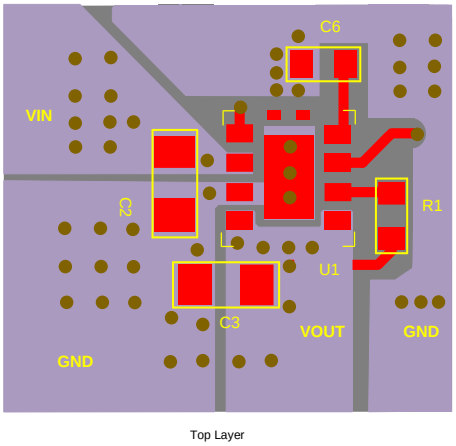
$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (9)$$

Where I_{LIM_AVG} is the average start-up current during soft-start period, and t_{SS} is the soft-start time.

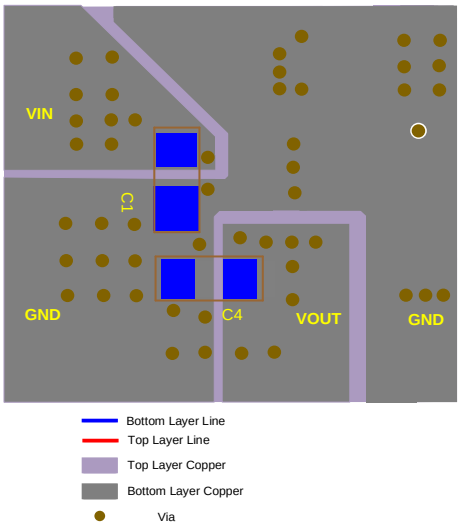
PCB Layout Guidelines (10)

An optimized PCB layout is critical for reliable operation. For the best results, refer to Figure 4 and follow the below guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
3. Ensure that the high-current paths (PGND, VIN, and VOUT) have short and wide traces.
4. Place as many PGND vias as possible close to the pin to minimize parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to VCC and GND pin.



Top Layer



Bottom Layer

Figure 4: Recommended PCB Layout

Note:

10) This layout covers a full range of specifications. A much smaller layout size can be achieved for specific cases (e.g. higher switching frequency, lower input voltage, lower output current) by selecting smaller packages for the inductors and capacitors.

TYPICAL APPLICATION CIRCUIT

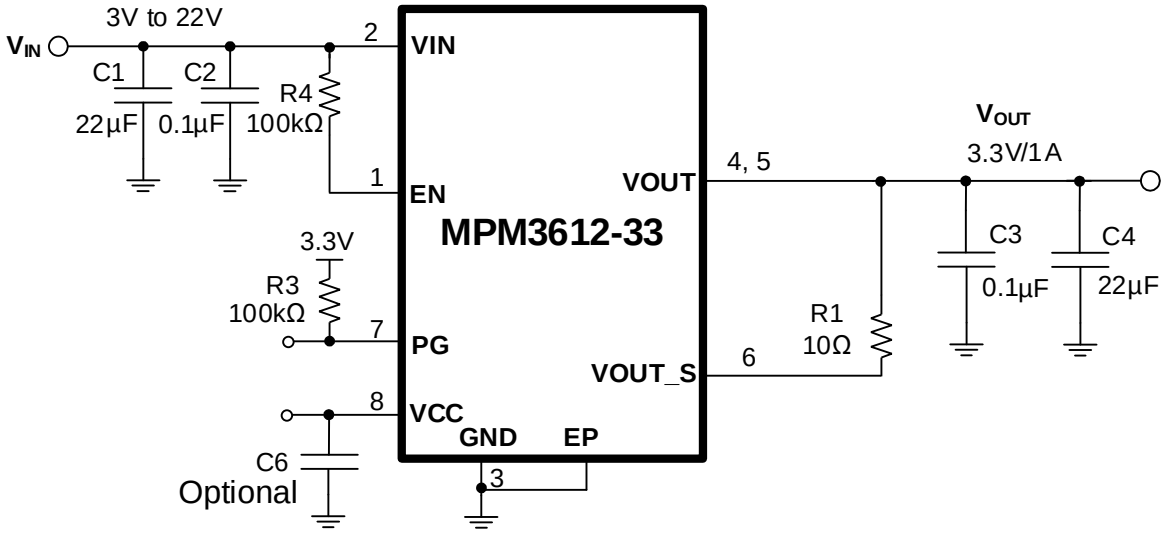
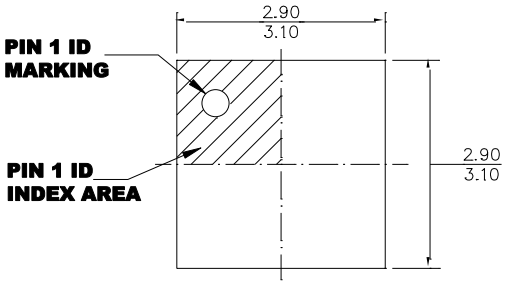


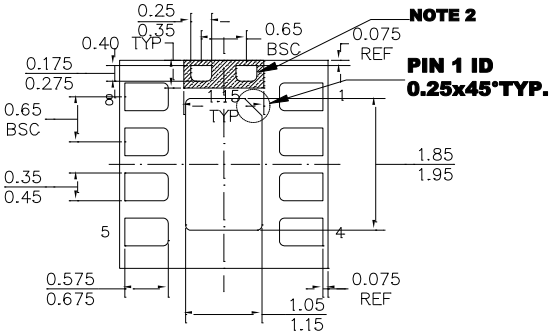
Figure 5: MPM3612-33 Typical Application Circuit

PACKAGE INFORMATION

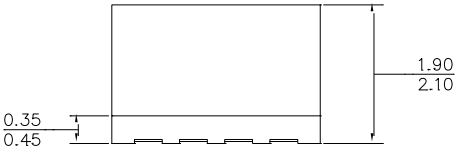
LGA-10 (3mmx3mmx2mm)



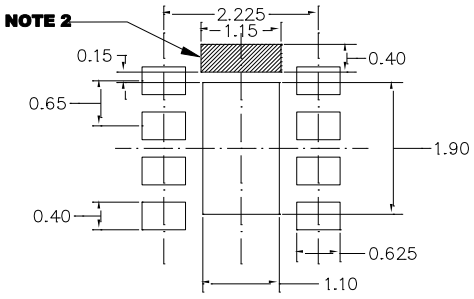
TOP VIEW



BOTTOM VIEW



SIDE VIEW

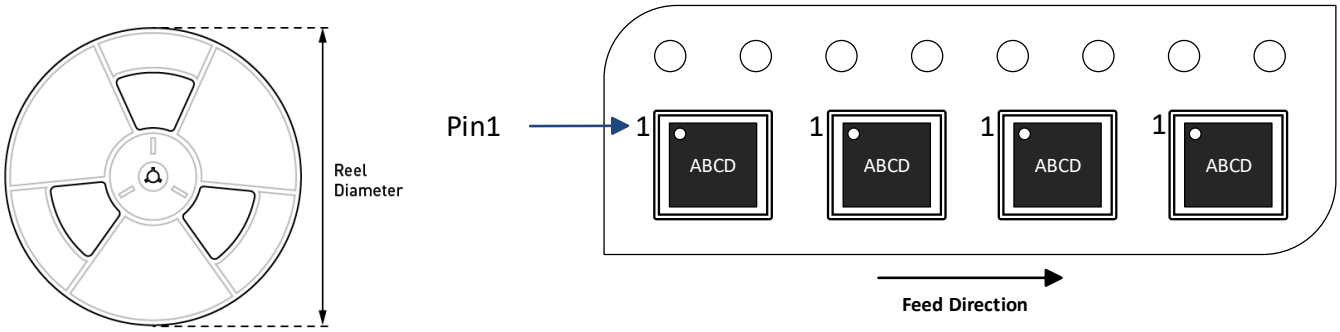


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2)SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-303.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3612GLQ-33-Z	LGA-10 (3mmx3mmx2mm)	2500	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/15/2023	Initial Release	-