PIN Diode Driver (Positive Voltage)

MPD3T28125-701 Datasheet

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Features

- High output voltage and high output current PIN diode driver in surface mount package
- Usable with MSW3100 series T-R and symmetrical high power SP3T switches
- Operates from positive voltage: +5 V and +28 V to +125 V
- High output current (200 mA) for Low switch loss and high isolation
- Separate TTL input controls, 3 pairs of complementary outputs
- RoHS complaint

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Description

The MPD3T28125-701 Surface Mount PIN Diode Driver is designed to provide high voltage and high current bias signals to high power PIN diode single pole three throw (SP3T) switches. This PIN diode driver is intended to operate with Aeroflex/Metelics MSW3100 series of surface mount, high power SP3T transmit-receive and symmetrical switches, as well as with switch designs employing discrete PIN diodes. The driver operates with positive supply voltages only.

This driver can supply voltages from 28 V to 125 V for reverse biasing switching PIN diodes to enable PIN diode switches, such as those described above, to handle up to 100 W CW RF signals. The MPD3T28125-701 driver can source current up to 200 mA to enable PIN diode switches to produce low insertion loss and high isolation. The driver can be controlled via three TTL-compatible control ports. Three complementary outputs are available which can drive the six bias ports which are required for a typical SP3T PIN diode switch which employs the series-shunt topology, or for asymmetrical switch designs. Switching time is approximately 1.5 µs.

The PIN driver is available in a 1.3 (W) x 1.3 (L) x 0.33 (H) inches (33 x 33 x 8.4 mm) surface mount package. The device is available in tube and tape-reel packaging for high volume pick and place automated assembly.

MPD3T28125-701 Surface Mount PIN Diode Driver is RoHS compliant.

Applications

The MPD3T28125-701 switch driver is designed to provide high voltage and high current bias to high power PIN diode SP3T switches. This driver is compatible with high volume, surface mount, solder reflow manufacturing. The product is durable, reliable, and capable of operating reliably in military, commercial and industrial environments.

Environmental Capabilities

The MPD3T28125-701 switch driver is capable of meeting the environmental requirements of MIL-STD-202 and MIL-STD-750.

ESD and Moisture Sensitivity Level Rating

All semiconductor devices are susceptible to damage from ESD events. Proper precautions must be taken to protect this product from such events. The ESD rating for this device is Class 1A, HBM. The moisture sensitivity level rating for this device is MSL 1.

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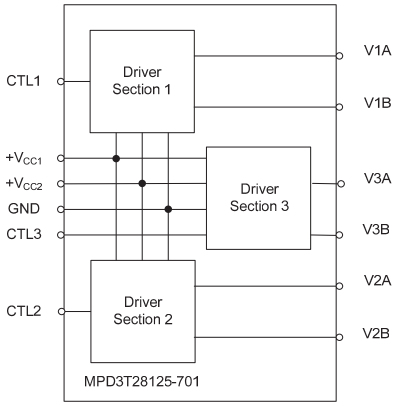
Block Diagram:



MPD3T28125-701 Electrical Specifications

T_A = +25 °C (Unless Otherwise Defined)

Parameter	Symbol	Test Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Operating Frequency	PRF	$+V_{CC1}$ = 5 V, $+V_{CC2}$ = 28 V to 125 V	0	100	500	kHz
Supply Voltage 1	$+V_{CC1}$		4.5	5	5.5	V
Supply Voltage 2	$+V_{CC2}$		10	28	125	V
Quiescent Current, $+V_{CC1}$	I_{Q1}	$+V_{CC1}$ = 5 V, $+V_{CC2}$ = 28 V to 125 V, no load connected to Output A and Output B	5	10	20	mA
Quiescent Current, $+V_{CC2}$	I_{Q2}	$+V_{CC1}$ = 5 V, $+V_{CC2}$ = 28 V to 125 V, no load connected to Output A and Output B	30	40	50	mA
TTL Input Voltage	V_{TTL}	Logic 0: sink current = 20 µA Logic 1: source current = 500 µA	0 2.0	- - -	0.8 5.0	V
Low Level Output Voltage, Output 1 or Output 2 or Output 3	V_{OUTL}	$+V_{CC1}$ = 5 V, $+V_{CC2}$ = 28 V to 125 V, sink current = 200 mA	0.05	0.1	0.2	V
High Level Output Voltage, Output 1 or Output 2 or Output 3	V_{OUTH}	$+V_{CC1}$ = 5 V, $+V_{CC2}$ = 28 V to 125 V, source current = 20 mA	$+V_{CC2}$-1	$+V_{CC2}$ - 0.3	$+V_{CC2}$ - 0.1	V
Switching Time (Note 1)	T_{ON} T_{OFF}	$+V_{CC1}$ = 5 V, $+V_{CC2}$ = 28 V to 125 V, f = 10 kHz, 50% TTL to 10% or 90% RF output voltage	- - -	1.5	2	µs

Notes:
1. Switching time is measured using the Aeroflex/Metelics MSW2031-203 Symmetrical SP3T switch, f_{RF} = 500 MHz, $+V_{CC1}$ = 5 V and $+V_{CC2}$ = 50 V in the commutating switching mode.

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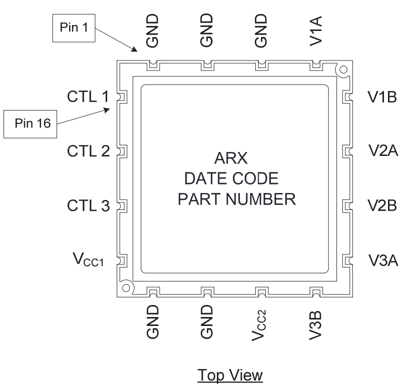
Absolute Maximum Ratings

T_A = +25 °C (Unless Otherwise Defined)

Parameter	Conditions	Absolute Maximum Value
Input Voltage, $+V_{CC1}$		-0.5 V to 6.0 V
Input Voltage, $+V_{CC2}$		-0.5 V to 130 V
Control Port Input Voltage		-0.5 V to 5.5 V
Output Sink Current	$V_{OUT} = 0$ V	200 mA
Output Source Current	$V_{OUT} \approx +V_{CC2}$ V	25 mA
Operating Temperature		- 65 °C to 125 °C
Storage Temperature		- 65 °C to 150 °C
Assembly Temperature	t ≤ 10 s	260 °C
Total Dissipated Power	$T_{CASE} = 85$ °C	2.0 W

Pinout & Pin Description



Pin	Pin Name	Input/ Output (I/O)	Description
1	GND		$+V_{CC1}$ & $+V_{CC2}$ ground return
2	GND		$+V_{CC1}$ & $+V_{CC2}$ ground return
3	GND		$+V_{CC1}$ & $+V_{CC2}$ ground return
4	V1A	O	Bias voltage/current output from driver section 1 (V1A, Inverted output W.R.T. CTL1 control)
5	V1B	O	Bias voltage/current output from driver section 1 (V1B, Non-Inverted output W.R.T. CTL1 control)
6	V2A	O	Bias voltage/current output from driver section 2 (V2A, Inverted output W.R.T. CTL2 control)
7	V2B	O	Bias voltage/current output from driver section 2 (V2B, Non-Inverted output W.R.T. CTL2 control)
8	V3A	O	Bias voltage/current output from driver section 3 (V3A , Inverted output W.R.T. CTL3 control)
9	V3B	O	Bias voltage/current output from driver section 3 (V3B , Non-Inverted output W.R.T. CTL3 control)
10	$+V_{CC2}$	I	High voltage (+28 V to +125 V) input
11	GND		$+V_{CC1}$ & $+V_{CC2}$ ground return
12	GND		$+V_{CC1}$ & $+V_{CC2}$ ground return
13	$+V_{CC1}$	I	V_{CC1} (+5V Input)
14	CTL 3	I	TTL control input to driver section 3
15	CTL 2	I	TTL control input to driver section 2
16	CTL 1	I	TTL control input to driver section 1

Truth Table

CTL1 (notes 1,2)	CTL2 (notes 1,2)	CTL3 (notes 1,2)	Driver Output Section 1	Driver Output Section 2	Driver Output Section 3
V_{HIGH}	V_{LOW}	V_{LOW}	V1A Low, 0 V, current sinking mode. V1B High, ≈ +VCC2, current sourcing mode.	V2A, High, ≈ +VCC2, current sourcing mode. V2B, Low, 0 V, current sinking mode.	V3A High , ≈ +VCC2, current sourcing mode V3B Low, 0 V , current sinking mode
V_{LOW}	V_{HIGH}	V_{HIGH}	V1A High, ≈ +VCC2, current sourcing mode. V1B Low, 0 V, current sinking mode.	V2A, Low, 0 V, current sinking mode. V2B, High, ≈ +VCC2, current sourcing mode.	V3A, Low, 0 V, current sinking mode. V3B, High, ≈ +VCC2, current sourcing mode.
VHIGH	V_{LOW}	V_{HIGH}	V1A Low, 0 V, current sinking mode. V1B High, ≈ +VCC2, current sourcing mode.	V2A, High, ≈ +VCC2, current sourcing mode. V2B, Low, 0 V, current sinking mode.	V3A Low, 0 V, current sinking mode. V3B High, ≈ +VCC2, current sourcing mode.
V_{LOW}	V_{HIGH}	V_{LOW}	V1A High, ≈ +VCC2, current sourcing mode. V1B Low, 0 V, current sinking mode.	V2A, Low, 0 V, current sinking mode. V2B, High, ≈ +VCC2, current sourcing mode.	V3A High, ≈ +VCC2, current sourcing mode. V3B Low, 0 V, current sinking mode.
V_{HIGH}	V_{HIGH}	V_{LOW}	V1A Low, 0 V, current sinking mode. V1B High, ≈ +VCC2, current sourcing mode.	V2A Low, 0 V, current sinking mode. V2B High, ≈ +VCC2, current sourcing mode.	V3A High, ≈ +VCC2, current sourcing mode. V3B Low, 0 V, current sinking mode.
V_{LOW}	V_{LOW}	V_{HIGH}	V1A High, ≈ +VCC2, current sourcing mode. V1B Low, 0 V, current sinking mode.	V2A High, ≈ +VCC2, current sourcing mode. V2B Low, 0 V, current sinking mode.	V3A, Low, 0 V, current sinking mode. V3B, High, ≈ +VCC2, current sourcing mode.
V_{LOW}	V_{LOW}	V_{LOW}	Not recommended (note 3)		
V_{HIGH}	V_{HIGH}	V_{HIGH}	Not recommended (note 3)		

Notes:

1. $2\text{ V} \le V_{HIGH} \le 5\text{ V}$
2. $0\text{ V} \le V_{LOW} \le 0.8\text{ V}$
3. Operation in these modes may not be compatible with the design of the PIN switch being controlled.

Applications

The MPD3T28125-701 surface mount PIN diode driver is optimized for use with Aeroflex Metelics families of SP3T switches. It can also be used to control other PIN diode SP3T switches. The driver comprises three driver sections, each of which is capable of providing either a forward-bias current or a reverse-bias, high voltage to a PIN diode, depending upon the TTL-compatible control voltage applied to its control port. Each section of the driver has a dedicated control port, so these sections are controlled and may be operated independently. In typical applications only one of the control inputs is driven HIGH at a time, and the other two inputs are driven LOW.

The driver evaluation board includes a parallel R-C network on the output of each driver section (R1-C3 on the driver output V1A, R2–C4 on the driver output V1B, R3-C5 on the driver output V2A, R4-C6 on the driver output V2B, R5-C7 on the driver output V3A and R6-C8 on the driver output V3B). Each network produces a current spike on the transitions of the driver state, which rapidly extracts stored charge from PIN diodes which are being forced from the conduction to the non-conduction state, as well as to rapidly inject charge into PIN diodes which are being forced from the non-conduction to the conduction state. These current spikes accelerate the transition of the switch from one state to the other.

Control of Symmetrical SP3T Switch

The MPD3T28125-701 is fully capable of controlling a SP3T switch comprising a series-shunt topology. Each driver section is connected to bias a series diode and a shunt diode of a switch arm. For example, in the configuration described below for the control of a symmetrical SP3T switch, driver output V1A biases the series diode connected between switch ports J0 and J1, the driver output V1B biases the shunt diode connected between switch ports J1 and B1. Similarly driver output V2A biases the series diode connected between switch ports J0 and J2, output V2B biases the shunt diode connected between switch ports J2 and B2 and output V3A biases the series diode connected between switch ports J0 and J3, the driver output V3B biases the shunt diode connected between switch ports J3 and B3.

A typical symmetric switch/driver application circuit is shown below. In this circuit, the MPD3T28125-701 driver is used to control the Aeroflex Metelics MSW3100-310 symmetrical SP3T switch. The switch is controlled to operate in one of three operational states, which are called State 1, State 2 and State 3. In the descriptions of States 1, 2 and 3 (below), it is assumed that $+V_{CC1} = 5$ V and $+V_{CC2} = 28$ V.

Truth Table for Control of Symmetrical SP3T Switch, MSW310X-310

$+V_{CC1} = 5$ V and $+V_{CC2} = 28$ V (Unless otherwise noted)

CTL1 (note 1)	CTL 2 (note 1)	CTL 3 (note 1)	RF State	Path J0 – J1	Path J0 – J2	Path J0 – J3	J1 Bias V1A	J2 Bias V2A	J3 Bias V3A	B1 Bias V1B	B2 Bias V2B	B3 Bias V3B
V_{HIGH}	V_{LOW}	V_{LOW}	State 1	Low Loss	High Isolation	High Isolation	0 V -100 mA	27 V 0 mA	27 V 0 mA	27 V 0 mA	0 V -25 mA	0 V -25 mA
V_{LOW}	V_{HIGH}	V_{LOW}	State 2	High Isolation	Low Loss	High Isolation	27 V 0 mA	0 V -100 mA	27 V 0 mA	0 V -25 mA	27 V 0 mA	0 V -25 mA
V_{LOW}	V_{LOW}	V_{HIGH}	State 3	High Isolation	High Isolation	Low Loss	27 V 0 mA	27 V 0 mA	0 V -100 mA	0 V -25 mA	0 V -25 mA	27 V 0 mA

Note 1 : All other conditions are not recommended.

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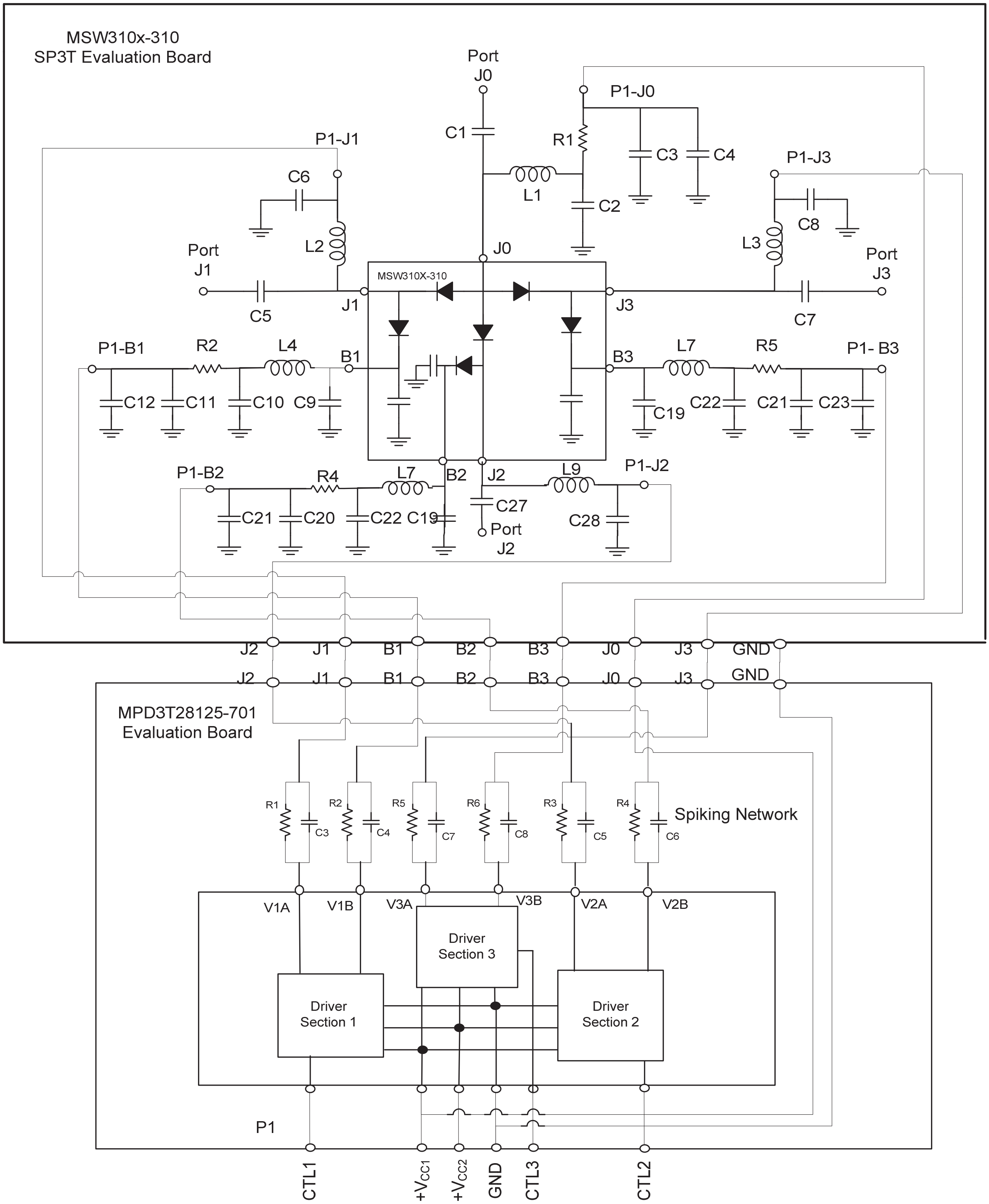
Interfacing MSW310x-310 switch module evaluation board with MPD3T28125-701 driver module evaluation board



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State 1

In State 1, the path from port J0 to J1 is in its low insertion loss condition. The path from port J0 to port J2, and the path from port J0 to port J3, are in their high isolation states.

In State 1, the control voltage applied to CTL 1 is TTL-logic high, and the control voltages applied to CTL 2 and CTL 3 are TTL-logic low, which forward biases the series PIN diode between the J0 and J1 ports by applying 0 V to the J1 bias input port (P1-J1), while reverse-biasing the series diodes connected from port J0 to port J2, and from port J0 to port J3. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J0 bias port (P1-J0), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA.

At the same time, the shunt PIN diodes connected between port J2 and B2 and between port J3 and B3 are also forward biased by applying a high bias voltage, nominally 28 V, to the J2 and J3 bias ports (P1-J2, P1-J3) and 0 V to the B2 and B3 bias ports (P1-B2, P1-B3). The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J2 and J3 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resistances of R4 and R5. These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J2 ports, between the J0 and J3 ports and the shunt diode between J1 and B1 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non-conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0-to-J1 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J2 bias port or J3 bias port and the DC forward voltage of the forward-biased J0-to-J1 series PIN diode.

The minimum voltage required to maintain the series diode between ports J0 and J2 and the series diode between ports J0 and J3 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the series diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. The minimum reverse bias voltage may be calculated as described in the "Minimum Reverse Bias Voltage" section (below).

State 2

In State 2, the path from port J0 to J2 is in its low insertion loss condition. The path from port J0 to port J1, and the path from port J0 to port J3, are in their high isolation states.

In State 2, the control voltage applied to CTL 2 is TTL-logic high, and the control voltages applied to CTL 1 and CTL 3 are TTL-logic low, which forward biases the series PIN diode between the J0 and J2 ports by applying 0 V to the J2 bias input port (P1-J2), while reverse-biasing the series diodes connected from port J0 to port J1, and from port J0 to port J3. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J0 bias port (P1-J0), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA.

At the same time, the shunt PIN diodes connected between port J1 and B1 and between port J3 and B3 are also forward biased by applying a high bias voltage, nominally 28 V, to the J1 and J3 bias ports (P1-J1, P1-J3) and 0 V to the B1 and B3 bias ports (P1-B2, P1-B3). The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J1 and J3 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resistances of R2 and R5. These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J1 ports, between the J0 and J3 ports and the shunt diode between J2 and B2 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non-conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0-to-J2 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J1 bias port or J3 bias port and the DC forward voltage of the forward-biased J0-to-J2 series PIN diode.

State 3

In State 3, the path from port J0 to J3 is in its low insertion loss condition. The path from port J0 to port J1, and the path from port J0 to port J2, are in their high isolation states.

In State 3, the control voltage applied to CTL 3 is TTL-logic high, and the control voltages applied to CTL 1 and CTL 2 are TTL-logic low, which forward biases the series PIN

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diode between the J0 and J3 ports by applying 0 V to the J3 bias input port (P1-J3), while reverse-biasing the series diodes connected from port J0 to port J1, and from port J0 to port J2. The magnitude of the resultant bias current through the forward-biased diode is primarily determined by the voltage applied to the J0 bias port (P1-J0), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA.

At the same time, the shunt PIN diodes connected between port J1 and B1 and between port J3 and B2 are also forward biased by applying a high bias voltage, nominally 28 V, to the J1 and J2 bias ports (P1-J1, P1-J2) and 0 V to the B1 and B2 bias ports (P1-B2, P1-B2). The magnitudes of the bias currents through these diodes are primarily determined by the voltage applied to the J1 and J2 bias ports, the magnitudes of the forward voltage across each of the PIN diodes and the resistances of R2 and R4. These currents are nominally 25 mA each. Under this condition, the series PIN diodes connected between the J0 and J1 ports, between the J0 and J2 ports and the shunt diode between J3 and B3 are each reverse biased.

The reverse bias voltage applied to non-conducting diodes must be sufficiently large to maintain each diode in its non-conducting, high impedance state when a large RF signal voltage may be present. For example, assume a large RF signal is present in the J0-to-J3 path. The reverse bias voltage across each of the series diodes in the other paths is the arithmetic difference of the bias voltage applied to the J1 bias port or J2 bias port and the DC forward voltage of the forward-biased J0-to-J3 series PIN diode.

Calculation of Resistor Values

The magnitude of the forward bias current applied to the series diode is set by the magnitude of the supply voltage $+V_{CC1}$, which is nominally 5 V, the value of resistor R1 and the forward voltage of the series diode, V_{DIODE}, among other factors. Given the desired current value, the resistance is given by the formula:

$$R_1 = \frac{(+V_{CC1} - V_{DIODE})}{I_{BIAS}}$$

The magnitude of the current through the shunt diode is set by the magnitude of the supply voltage $+V_{CC2}$, the value of resistor in series with the shunt diode (R2 or R4 or R5)and the forward voltage of the shunt diode, V_{DIODE}, among other factors. Given the desired current value, this resistance is given by the formula:

$$R_{SHUNT} = \frac{(+V_{CC2} - 0.3 - V_{DIODE})}{I_{BIAS}}$$

It is important to note that the switch module evaluation board, as supplied from the factory, is not capable of handling RF input signals larger than 45 dBm. If performance of the switch under larger input signals is to be evaluated, an adequate heat sink must be properly attached to the evaluation board, and several of the passive components on the board must be changed in order to safely handle the dissipated power as well as the high bias voltage necessary for proper performance. Contact the factory for recommended components and heat sink.

Minimum Reverse Bias Voltage

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal is given by:

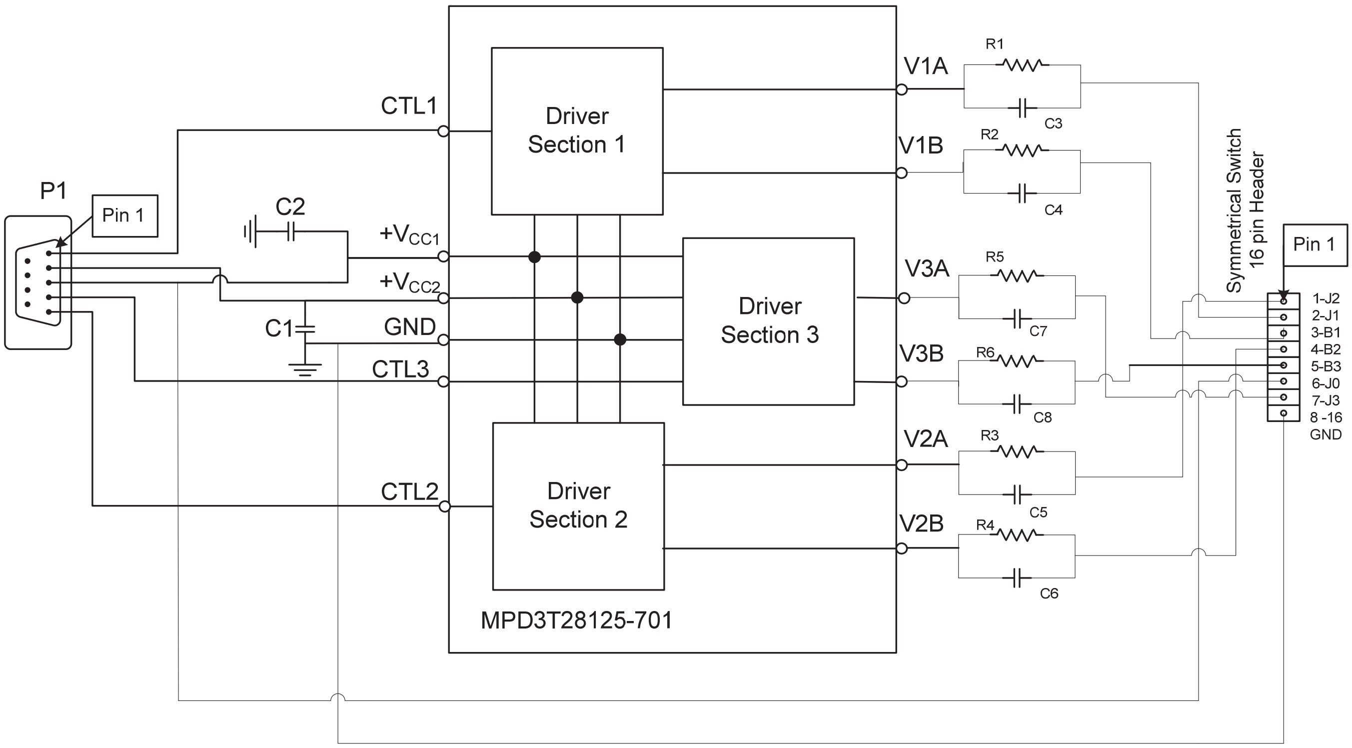
$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1 + \left[\left(\frac{0.0142 \times f_{MHz} \times W_{mils}^2}{V_{RF} \times \sqrt{D}}\right) \times \left(1 + \sqrt{1 + \left(\frac{0.056 \times V_{RF} \times \sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2}}$$

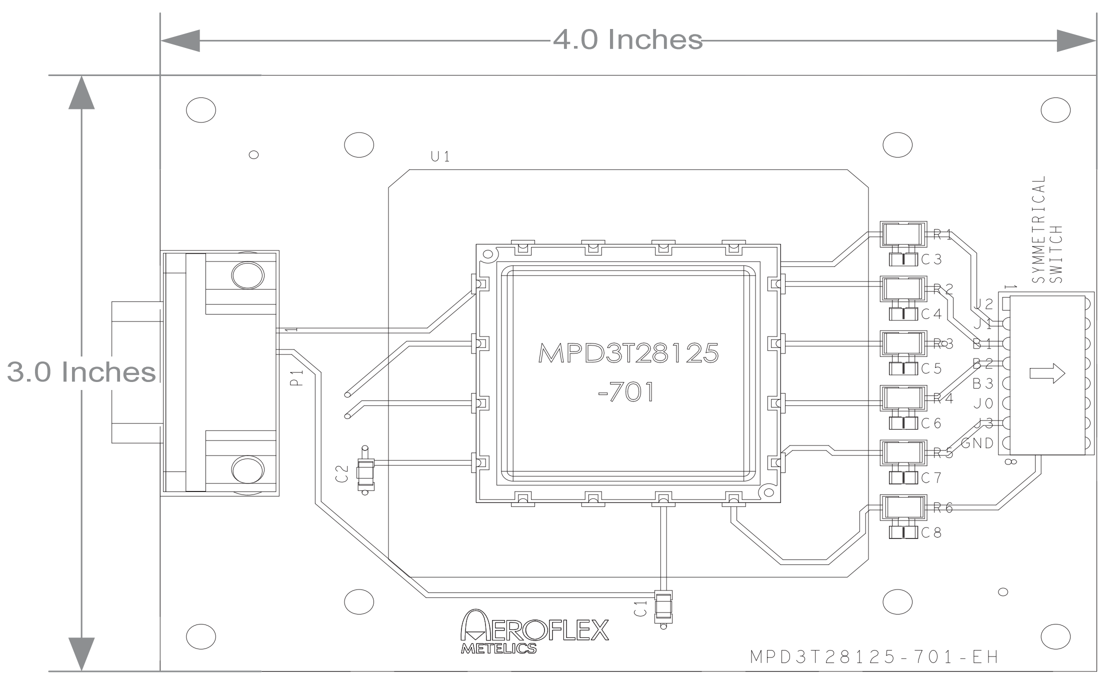
where

$\|V_{DC}\|$	=	magnitude of the minimum DC reverse bias voltage
$\|V_{RF}\|$	=	magnitude of the peak RF voltage (including the effects of VSWR)
f_{MHz}	=	lowest RF signal frequency expressed in MHz
D	=	duty factor of the RF signal
W_{mils}	=	thickness of the diode I layer, expressed in mils (thousandths of an inch)

(Caverly, R. H. & Hiller, G., “Establishing the Minimum Reverse Bias for a p-i-n Diode in a High-Power Switch”, IEEE Transactions on Microwave Theory and Techniques, Vol. 38, No. 12, December 1990)

MPD3T28125-701 3CH Driver Evaluation Board Block Diagram





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Driver Evaluation Board

The evaluation board for the MPD3T28125-701 allows for full exercise of the driver, as well as to utilize the driver to control symmetrical or asymmetrical Aeroflex Metelics SP3T switch evaluation circuits.

In addition to the MPD3T28125-701 driver, the evaluation board contains several passive components. C1 and C2 are bypass capacitors for the $+V_{CC2}$ and $+V_{CC1}$ supply voltages, respectively. R1 and C3 form a parallel RC network which can be used to decrease switching time for the diodes which are driven by the driver output V1A similarly R2 C4 , R3 C5 , R4 C6 , R5 C7 and R6 C8 spiking networks are driven by the V1B , V2A , V2B , V3A and V3B driver outputs respectively. These are the 3 complimentary pair outputs of the MPD3T28125-701 driver. There are two multi-pin connectors on the board. P1 is a DB-9 male connector which facilitates connection of the TTL control signal(s), supply voltages and ground to the evaluation board, symmetrical switch a 16-pin female header which can be used to connect directly to the male header on Aeroflex Metelics SP3T symmetrical switch evaluation boards. The pinouts for these connectors are shown in the tables below. Please note that the MPD3T28125-701 evaluation board is intended to operate only one high power PIN diode switch at a time.

Pinout – P1 Connector - MPD3T28125-701 Eval Board

DB-9 Connector Pin Number	Connects to MPD3T28125-701 Pin Number	MPD3T28125-701 Pin Name	Function
1	16	CTL1	TTL logic input for driver section 1
2	10	$+V_{CC2}$	High voltage bias supply (28 V ≤ $+V_{CC2}$ ≤ 125 V)
3	13	$+V_{CC1}$	Logic supply voltage (5 V)
4	14	CTL3	TTL logic input for driver section 3
5	15	CTL2	TTL logic input for driver section 2
6, 7, 8	1, 2, 3, 11, 12	GND	Supply return for $+V_{CC1}$ and $+V_{CC2}$
9	No Connection	N/A	N/A

Pinout – 16 Pin Header (Symmetrical Switch Connector) - MPD3T28125-701 Eval Board (SP3T Symmetric Switches Modules)

16 Pin Header Connector Pin Number	Connects to Symmetric Switch Pin Name	Function
1	J2	Bias signal to bias RF port J2 , V2A
2	J1	Bias signal to bias RF port J1 , V1A
3	B1	Bias signal to bias port B1 , V1B
4	B2	Bias signal to bias port B1 , V2B
5	B3	Bias signal to bias port B3 , V3B
6	J0	$+V_{CC1}$ (5 V typical) supply voltage to bias RF port J0
7	J3	Bias signal to bias RF port J3 , V3A
8	GND	Supply return for $+V_{CC1}$ and $+V_{CC2}$
9 to 16	GND	Supply return for $+V_{CC1}$ and $+V_{CC2}$

PIN Diode Driver

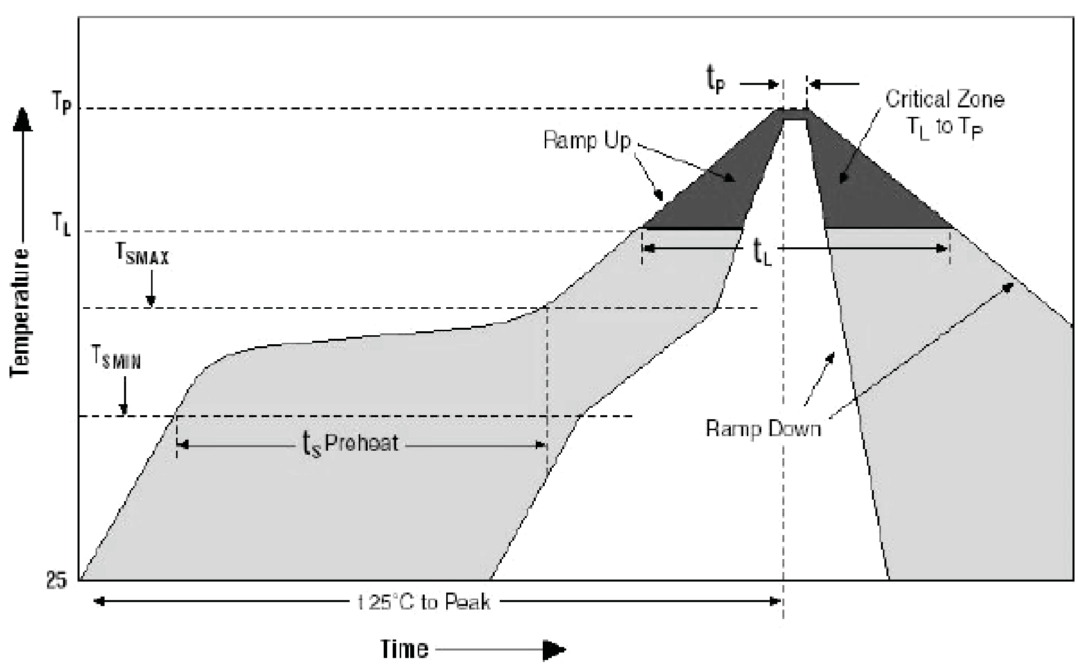
Assembly Instructions

The MPD3T28125-701 PIN Diode Drivers are capable of being placed onto circuit boards with pick and place manufacturing equipment from tube or tape-reel dispensing. The devices are attached to the circuit board using conventional solder re-flow or wave soldering procedures with RoHS type or Sn 60/Pb 40 type solders per Table I and Graph I Time-Temperature recommended profile.

Table 1: Time-Temperature Profile for Sn 60/Pb 40 or RoHS Type Solders

Profile Feature	Sn-Pb Solder Assembly	Pb-Free Solder Assembly
Average ramp-up rate (T_L to T_P)	3 °C/second maximum	3 °C/second maximum
Preheat - Temperature Minimum (T_{SMIN}) - Temperature Maximum (T_{SMAX}) - Time (Minimum to maximum) (t_S)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
T_{SMAX} to T_L - Ramp-up Rate		 3 °C/second maximum
Time Maintained above: - Temperature (T_L) - Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak Temperature (T_P)	225 +0 / -5 °C	260 +0/-5 °C
Time within 5°C of actual Peak Temperature (T_P)	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second maximum	6 °C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Graph 1: Solder Re-Flow Time-Temperature Profile



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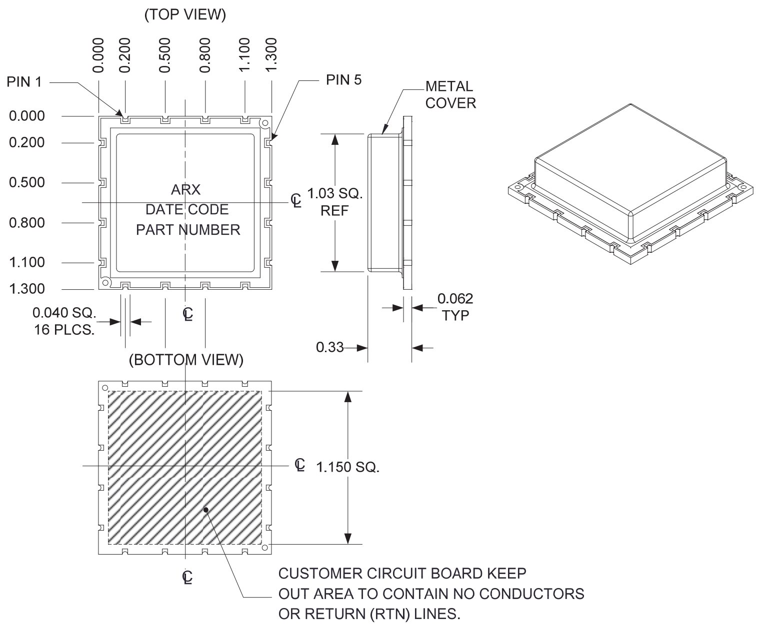
METELICS

Outline Drawing Case Style 701 (CS701)



NOTES:
1. CIRCUIT BOARD MATERIAL IS FR-4 TYPE.
2. METALLIZATION: 2oz Cu FOLLOWED BY, 150μin TYP. Ni, FOLLOWED BY 4μin TYP. Au.

Part Number Ordering Information:

Part Number	Packaging
MPD3T28125-701-T	Tube Packaging
MPD3T28125-701-R	Tape-Reel Packaging (Quantities of 250 or 500)
MPD3T28125-701-W	Waffle Packaging
MPD3T28125-701-E	Evaluation Board

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ISO 9001:2008 certified companies

AEROFLEX
A passion for performance.

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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused.

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