MP7541B

15 V CMOS
Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **ESD Protection: 2000 V Minimum**
- **Full Four Quadrant Multiplication**
- **Low Glitch Energy**
- **12-Bit Linearity (End-Point)**
- **Guaranteed Monotonic. All Grades. All Temperatures.**
- **TTL/5 V CMOS Compatible**
- **Stable, More Accurate Segmented Architecture**
  - **2.0 ppm/°C Typ. Gain Error Tempco**
  - **0.2 ppm/°C Max. Linearity Tempco**
  - **Lowest Sensitivity to Output Amplifier Offset**
- **Latch-Up Free**

APPLICATIONS

- **Industrial Automation**
- **Automatic Test Equipment**
- **Disk Drive Servo Systems**
- **Digital/Synchro Conversion**
- **Programmable Gain Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generation**
- **Digitally Controlled Filters**

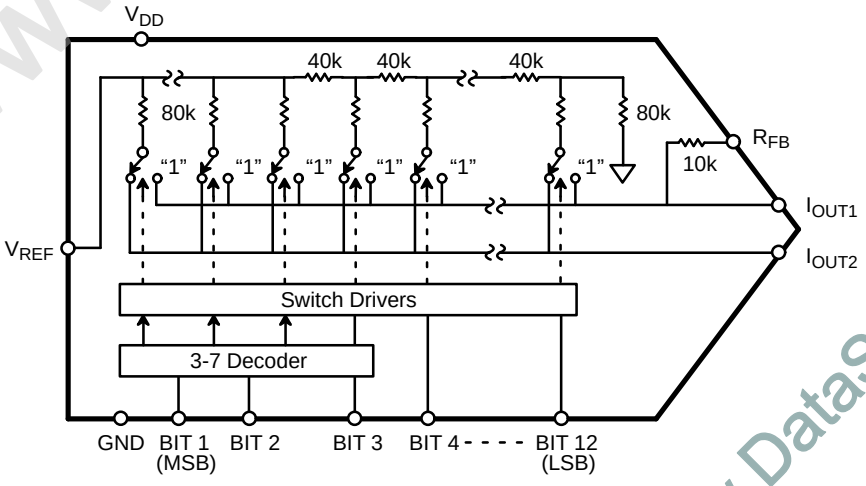
GENERAL DESCRIPTION

The MP7541B is a pin-compatible replacement which offers superior performance in latch-up and ESD protection versus the comparable 7541 and 7541A. The high ESD protection will reduce failures caused by mishandling. These devices are manufactured using patented advanced thin film resistors on a double metal CMOS process which result in ultra stable thin film and superior long life reliability and stability. The MP7541B incorporates a bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7541B's outstanding features are:

Stability: Both Integral Non-Linearity (INL) and Differential-Non-Linearity (DNL) are rated at 0.2 ppm/°C maximum. Monotonicity is guaranteed over the entire temperature range. Gain Temperature Coefficient (TCGE) is 2.0 ppm/°C typical.

Lower Sensitivity to Output Amplifier Offset: Multiplying DACs provide an output current into a virtual ground of the output op amp. Additional linearity error caused by the op amp is reduced by a factor of 3 in the MP7541B versus conventional R-2R DACs.

SIMPLIFIED BLOCK DIAGRAM



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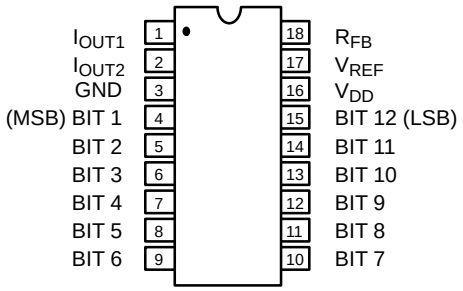
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (LSB)
Plastic Dip	–40 to +85°C	MP7541BKN	±1/2	±1/2	±5
Plastic Dip	–40 to +85°C	MP7541BJN	±1	±1	±8
SOIC	–40 to +85°C	MP7541BKS	±1/2	±1/2	±5
SOIC	–40 to +85°C	MP7541BJS	±1	±1	±8
Ceramic Dip	–55 to +125°C	MP7541BTD*	±1/2	±1/2	±5
Ceramic Dip	–55 to +125°C	MP7541BSD*	±1	±1	±8

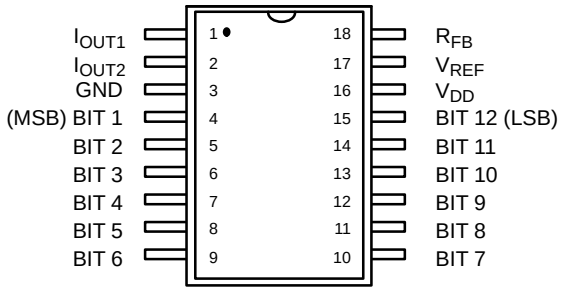
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin PDIP, CDIP (0.300")
N18, D18



18 Pin SOIC (Jedec, 0.300")
S18

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6

PIN NO.	NAME	DESCRIPTION
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10
14	BIT 11	Data Input Bit 11
15	BIT 12	Data Input Bit 12 (LSB)
16	V_{DD}	Positive Power Supply
17	V_{REF}	Reference Input Voltage
18	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

V_{DD} = + 15 V, V_{REF} = +10 V, I_{OUT1} = I_{OUT2} = GND = 0 V Unless Otherwise Noted.

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity
K, T				±1/2		±1/2		
J, S				±1		±1		
Differential Non-Linearity	DNL						LSB	All grades
K, T				±1/2		±1/2		monotonic over full
J, S				±1		±1		temperature range.
Gain Error	GE						LSB	Using Internal R_{FB}
K, T				±3		±5		
J, S				±6		±8		
Gain Temperature Coefficient[2]	TC_{GE}					±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		5	±50		±100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current	I_{LKG}		5	±10		±200	nA	Digital Inputs = 0 or 5 V
DYNAMIC PERFORMANCE[2]								RL=100Ω, C_{EXT}=13pF
Current Settling Time	t_S		0.65	1.0			µs	Full scale change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T		1.0				mV p-p	V_{REF} = 20 V p-p 10kHz, Sinewave
Glitch Energy	Egl		500				nVs	00--0 to 11--1 Input Change
Propagation Delay	t_{PD}		60				ns	From 50% of digital input to 10% of final analog output current
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{INH}, I_{INL}			±1.0		±1.0	µA	
Input Capacitance[2]								
Data	C_{IN}			8.0		8.0	pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		100				pF	DAC all 1's
	C_{OUT1}		50				pF	DAC all 0's
	C_{OUT2}		50				pF	DAC all 1's
	C_{OUT2}		100				pF	DAC all 0's
POWER SUPPLY[3]								
Functional Voltage Range[2]	V_{DD}	4.5		16	4.5	16	V	
Supply Current	I_{DD}			1.0		1.0	mA	All Digital Inputs = 0 or 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

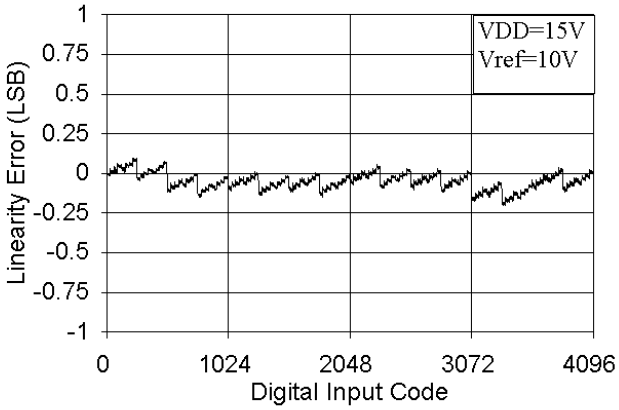
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 850mW
Derates above 75°C ..... 11mW/°C

NOTES:
1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 20mA for less than 100µs.

APPLICATION NOTES

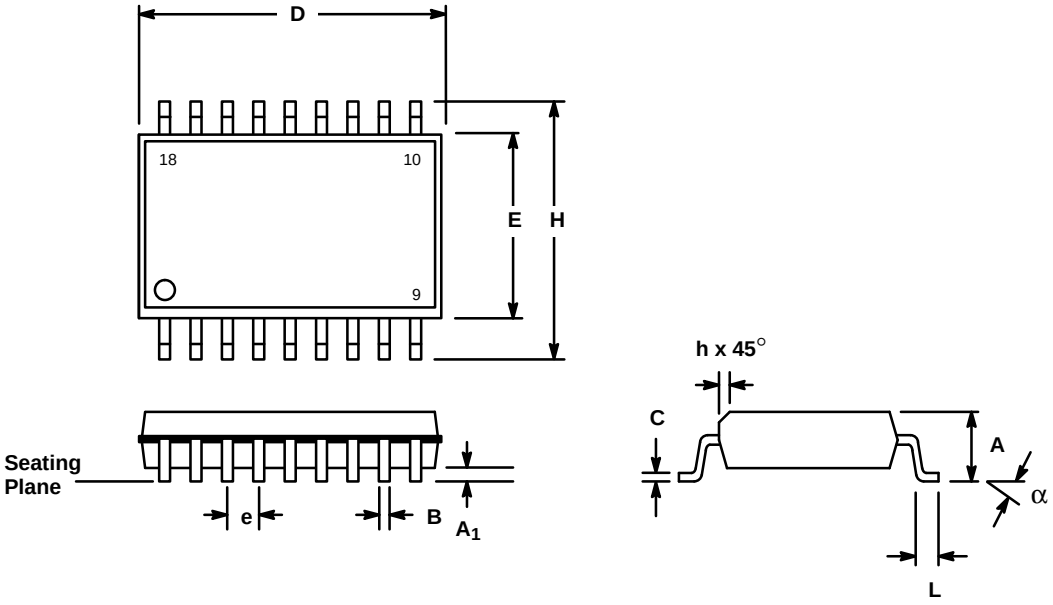
Refer to Section 8 for Applications Information

PERFORMANCE CHARACTERISTICS



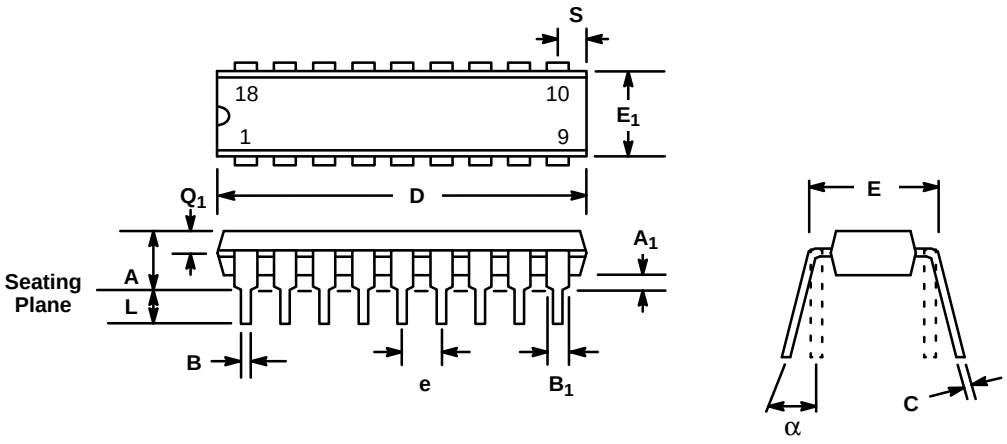
Graph 1. Linearity Error vs. Digital Input Code

18 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S18



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.641
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.451	0.461	11.46	11.71
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

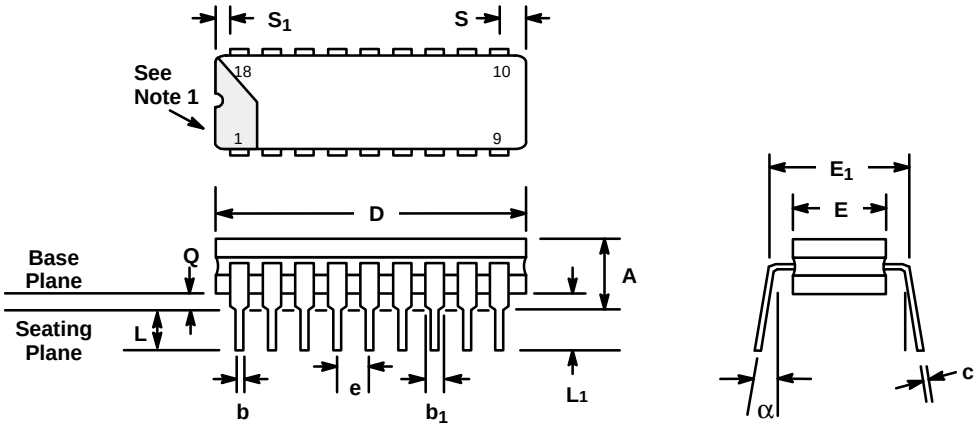
18 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N18



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.845	0.925	21.46	23.50
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.098	1.02	2.49

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

18 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D18



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

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