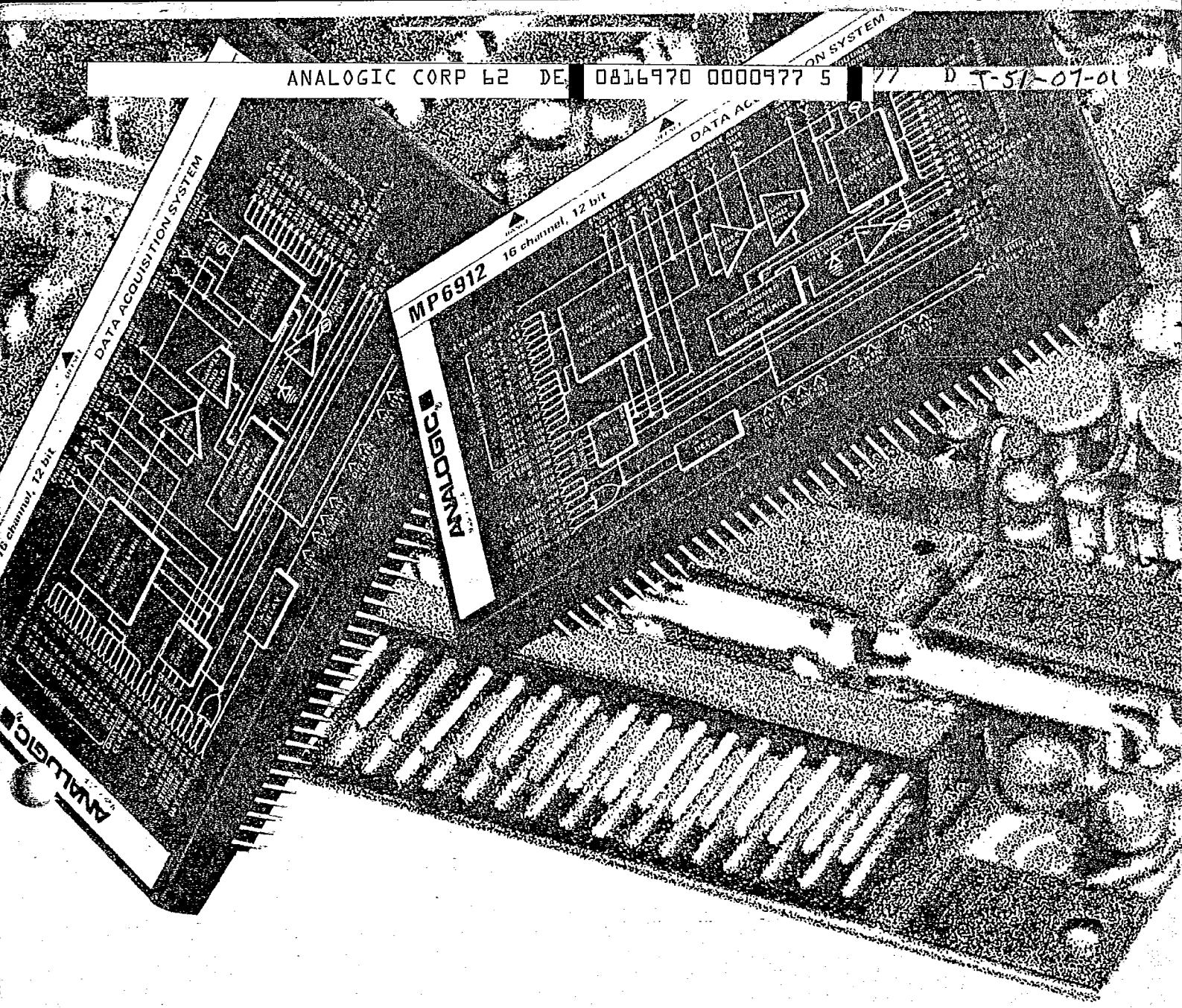


MP6912
SUBMINIATURE HIGH-SPEED DATA-ACQUISITION SYSTEM MODULE

ANALOGIC®

...The Digitizers

MP---06912-1x

The Analogic MP6912 is the smallest, highest-performance, lowest-powered, and most versatile data-acquisition module ever offered to the system designer. Despite its remarkably compact construction, this plug-in, PC-card mountable system provides all the scanning, signal-conditioning, A/D conversion, and programming/control/timing circuitry required for multi-channel high-speed 12-bit data acquisition.

OUTSTANDING FEATURES . . .

- A completely integrated subsystem — more consistent, accurate, and dependable than assemblies of individual modules.
- Effective electrostatic and electromagnetic shielding — to minimize noise problems.
- Height only 0.375" — fits 0.5" spacing.
- Very high throughput rates — from 100,000 12-bit Muxed, sampled conversions/sec to 480,000 single-channel 4-bit conversions/sec.
- Extreme flexibility of input/output/control/format.
- Insulated case can be mounted on two-sided pc board without shorting etch.

TABLE OF CONTENTS

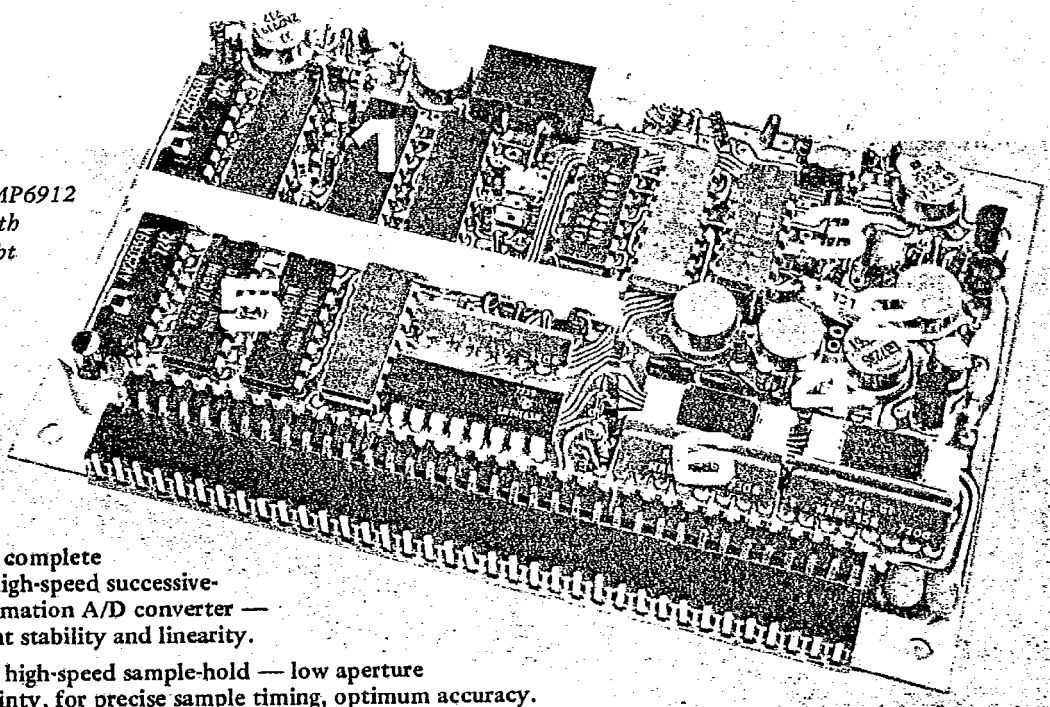


Photo of MP6912 interior with mating right angle connector in place.

1. **Built-in complete 12-bit high-speed successive-approximation A/D converter — excellent stability and linearity.**
2. **Built-in high-speed sample-hold — low aperture uncertainty, for precise sample timing, optimum accuracy.**
3. **Built-in premium reference, with excitation-current regulator.**
4. **Built-in fast, high-stability buffer amplifier — high CMRR, high impedance for optimum signal conditioning.**
5. **Built-in digital-output buffer amplifiers — high fan-out; load-isolated, will drive cables.**
6. **Built-in 16-channel Multiplexer (optionally expandable) for both single-ended and differential inputs.**

MP---06912-2X

B

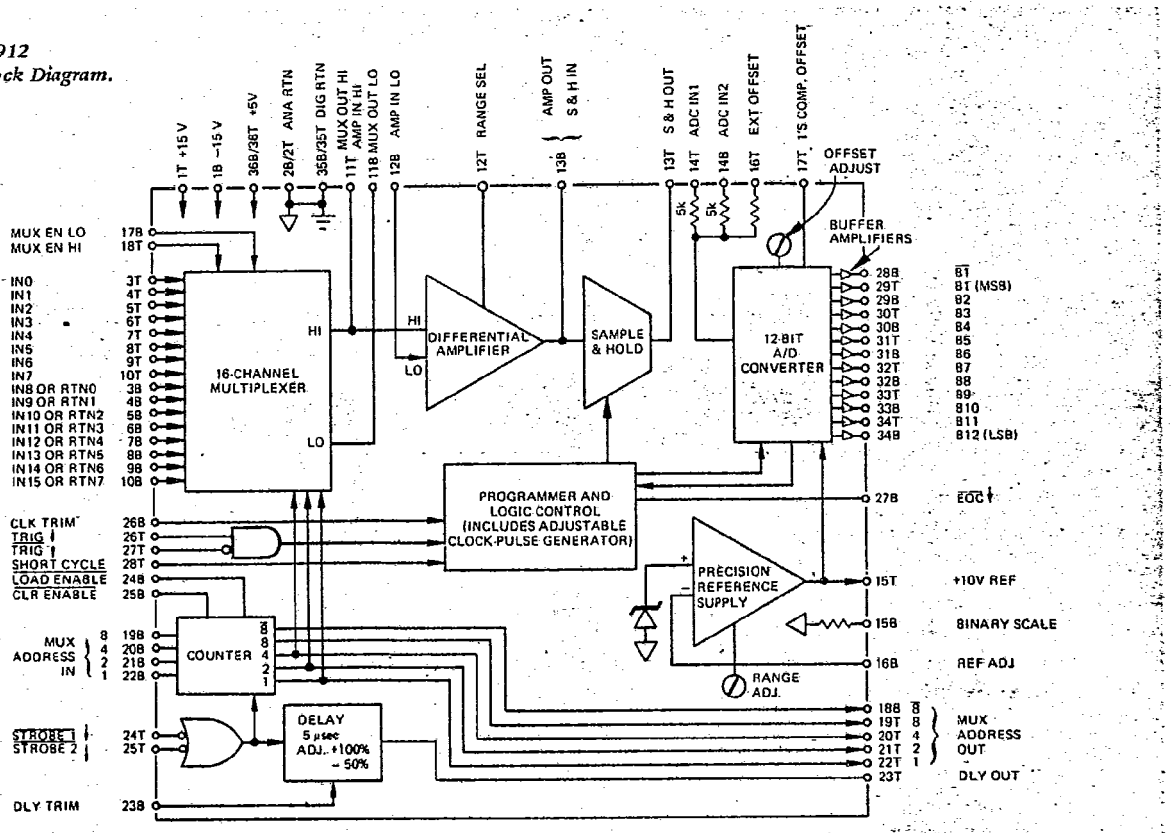
THEORY OF OPERATION

NOTE: Many of the circuit features mentioned briefly on this page are explained in more detail on subsequent pages, under DESIGN FEATURES.

The MP6912 comprises the following elements:

- A 16-input-line multiplexer, which may be used in any of three configurations: 16 single-ended input channels; 8 balanced (true-differential) input channels; or 16 "pseudo-differential" input channels, by connecting a remote "true ground", common to all signals, to the "AMP IN LO" terminal. This basic channel capacity is expandable essentially without limit by compatible accessories (see page 12).
- A high-performance differential buffer amplifier, with two jumper-selectable gains. (In conjunction with pin-selectable reference voltages, this feature provides a total of eight different full-scale input ranges).
- A high-speed sample-hold circuit, with very low aperture uncertainty (20 ns), and many advanced circuit features that increase the *effective* speed of the MUX/S-H scan/sample sequence, and minimize sampling errors at those high speeds.
- A high-performance, 12-bit, successive-approximation analog-to-digital converter, employing high-speed, low-drift quad-switch IC's, in the proven-superior Analogic current-switching DAC configuration. The reference for this configuration is a premium-grade zener-diode having very low T.C. The reference current is compensatorily slaved to the junction temperature of the most-significant quad chip. The comparator is an ultra-stable, high-speed design, with extremely fast settling time. The conversion register and conversion-control logic provide a wide choice of output codes.
- Fully buffered outputs, with high-fan-out, long-line capability not found in conventional A/D converters.
- A clock-pulse generator of great versatility, providing essentially jitter-free conversion and program-control timing, at rates that are adjustable over a wide range, by simple external control.
- A MUX-address circuit that provides a wide choice of sequential and random modes, as well as address-output, address-hold, and independent address-loading during conversion at the previous address, for higher attainable throughput rates.
- Provisions for both internal and external trimming of both range and offset . . . and many more facilities for remote adjustment or sequence-configuration of the programming and control functions, as described on later pages.

Figure 1. MP6912 Functional Block Diagram.

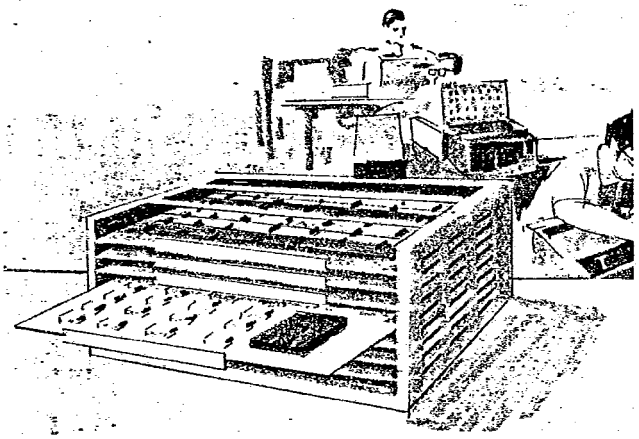


MP---06912-3x

APPLICATIONS

PROVIDING COMPLETE PLUG-IN A/D INTERFACE FOR MINICOMPUTERS

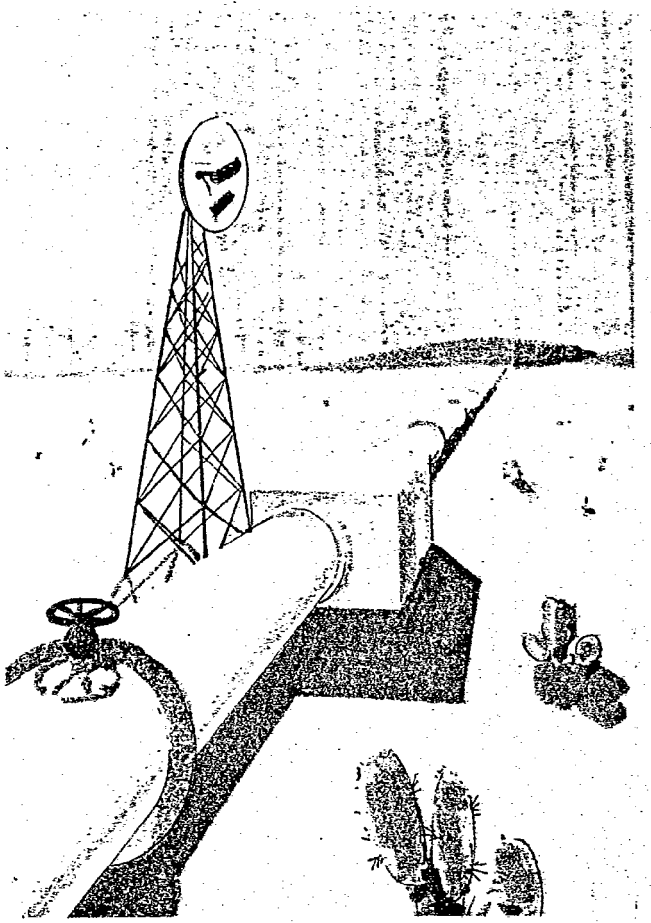
The MP6912 can be mounted on a single, small card, or on a small area on a mothercard, with or without a compatible accessory 5V-input converter power supply (see back cover), for installation into a single 0.5" slot on any standard card-cage. It can also plug *directly* into a card-cage connector. The MP6912 provides resolution/throughput-rate combinations from 12-bits at 100 kHz throughput-rate to 4 bits at 480 kHz throughput-rate . . . and every timing and control combination needed for computer programming of the data-acquisition function, through standard minicomputer "handshake" hardware.



Minicomputer A/D Interfacing

PRE-PROCESSING AND DIGITIZING ANALOG DATA AT REMOTE SITES, BEFORE TELEMETRY.

Low power drain, small size, and low cost recommend the MP6912 as the high-speed A/D interface between sensors and modems or telemetering transmitters. The flexibility of the analog interface eliminates sensor-cabling and common-mode problems, and the versatility of the control and timing functions simplifies remote control of the MUX-address, sampling, and data-synchronizing functions. For full 12-bit resolution, parallel data rates as high as 100,000 12-bit bytes per second are practical.



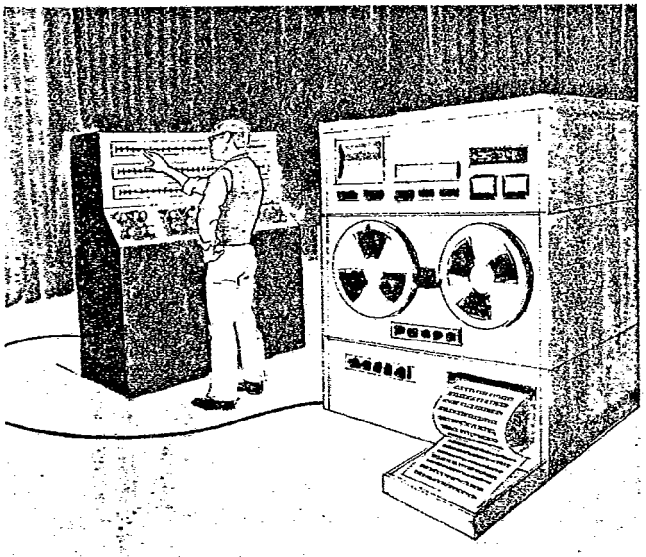
Remote-Site Telemetry

SIMPLIFYING DESIGN OF MODULAR DATA-ACQUISITION SYSTEMS — FIXED OR PORTABLE.

As the basic subsystem module in data-logging systems, the MP6912 provides many valuable functions besides A/D conversion — for example, unlimited MUX channel-capacity expansion (via compatible accessories that extend its built-in 16-channel capacity to any number desired, in multi-level increments of 32 channels). The MP6912 provides true "instrumentation-amplifier" signal-conditioning flexibility: external ranging; high CMRR (in a choice of true-differential or pseudo-differential formats, as explained on page 4); very

MP—06912-4X

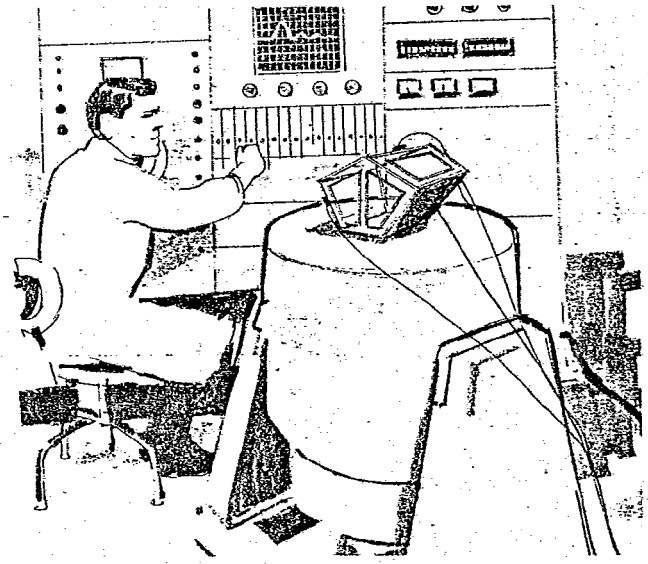
high input impedance; and very low offset voltage and current. The sample-hold circuitry in the MP6912 has state-of-the-art acquisition speed and aperture uncertainty. The MP6912 is capable of operating in the "overlap" mode, in which a new channel may be selected while the analog value from the preceding sample is being held for conversion, permitting significant increase in throughput rates. These and many other MP6912 design features (see pages 4 to 6) provide greater functional freedom, and wider performance margins, than can be obtained by combining individual modules, in this price class.



Data-Logging Systems

IMPROVING MULTI-CHANNEL FAST-FOURIER-TRANSFORM SPECTRUM-ANALYSIS SYSTEMS

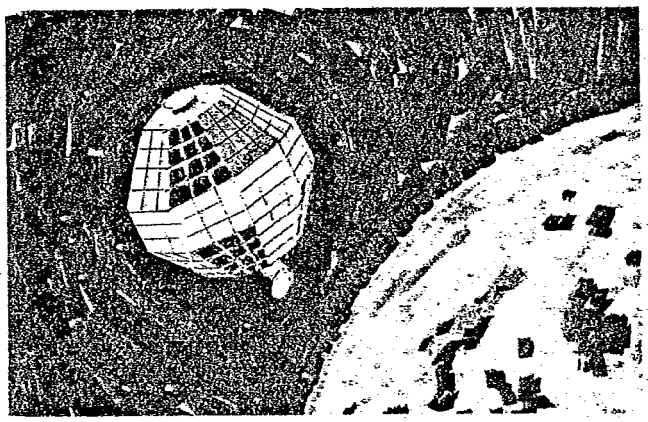
The high data-throughput rates attainable by the A/D converter in the MP6912 (see page 6) are complemented by its fast, low-jitter sample-hold, by its low-crosstalk, break-before-make MUX, and by its fast-settling buffer amplifier. These features, as well as excellent linearity and stability, and monotonicity, simplify and lower the cost of optimizing wideband high-resolution, "alias-free" spectrum-analysis instrumentation.



Vibration Spectrum Analysis Systems

REDUCING THE COST AND SIZE OF MULTI-CHANNEL PCM COMMUNICATION SYSTEMS.

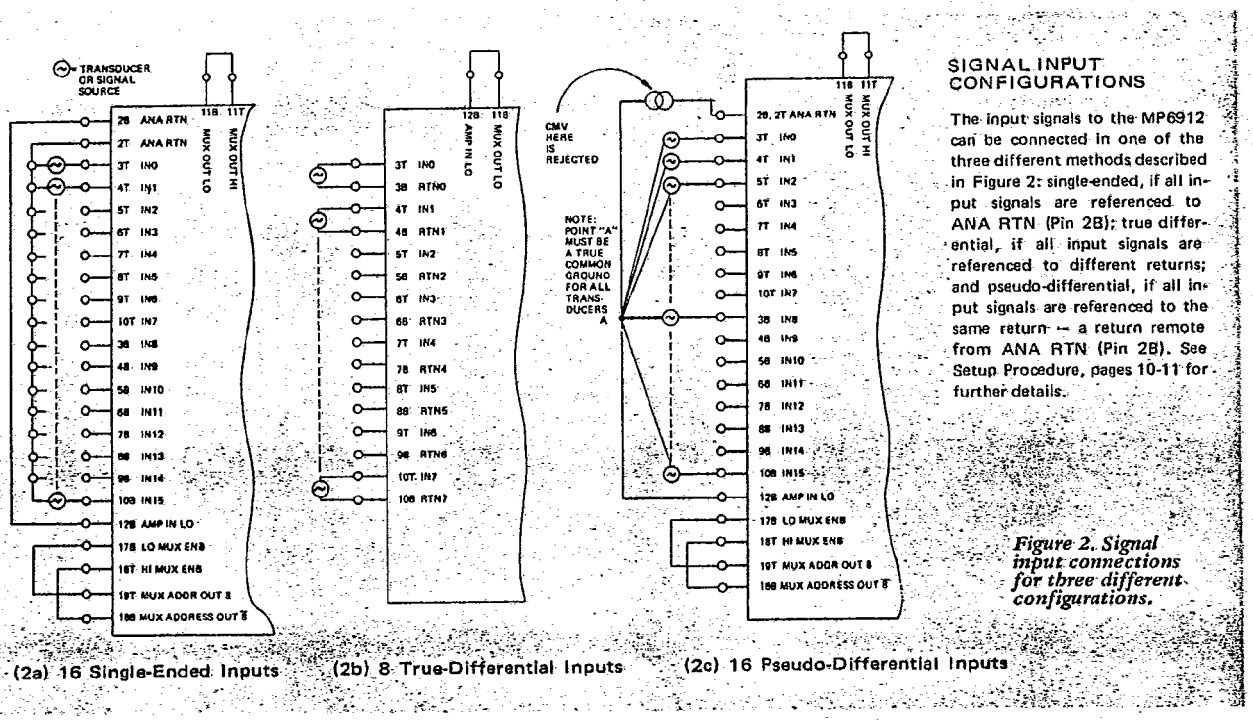
In a wide range of applications, from remote-site multiplexed audio program transmission to satellite-linked telephony, the speed, low power drain, and economy of the MP6912 make it the ideal system building block. Here, as in the other applications described on this page, the remarkable *versatility* of control/program/timing functions of this new design provide unprecedented built-in design freedom.



Telecommunications Satellite

MP---06912-5X

DESIGN FEATURES



SIGNAL INPUT CONFIGURATIONS

The input signals to the MP6912 can be connected in one of the three different methods described in Figure 2: single-ended, if all input signals are referenced to ANA RTN (Pin 28); true differential, if all input signals are referenced to different returns; and pseudo-differential, if all input signals are referenced to the same return — a return remote from ANA RTN (Pin 28). See Setup Procedure, pages 10-11 for further details.

Figure 2. Signal input connections for three different configurations.

OVERALL — Before examining the individual features of the MP6912, it would be appropriate to look at this unique design as an *entity*. Six characteristics of the design are particularly impressive:

- This extremely versatile and complete subsystem module contains *less than 120 components*. Using the latest MSI circuits, including several proprietary Analogic designs, the MP6912 has significantly fewer components than earlier designs, hence higher reliability.
- The power dissipation is so low that, despite the very small surface area provided by the MP6912's subminiature package, the *maximum hot-spot temperature rise is only 15°C*. . . a factor that greatly contributes not only to ultimate reliability and operational stability, but also to generous safety margins on such factors as timing, noise immunity, input/output rise-time tolerance, etc.
- The *unprecedented modal versatility* of this design reflects Analogic's years of experience in systems architecture and information-processing constraints.
- In fact, with the exception of a power supply (available as a compatible accessory — see back cover), it is difficult to find a data-acquisition function, range, or signal environment that is not already accommodated by the MP6912 . . . without external add-ons, or the design and debugging necessary to provide them.
- The *unique mechanical design* of the MP6912 — the first major advance in functional-module packaging in several years — offers many direct and indirect benefits to the systems designer.
- Finally, the *overall* accuracy, stability, linearity, and dynamic response of the MP6912 *are all significantly better than can be attained by assembly and trimming of individual modules* . . . unless one were to ignore cost entirely. This performance optimization is gained, *in an integrated subsystem module*, by taking advantage of two design opportunities: first, the fact that the entire subsystem has been designed as an entity allows for control of many error sources that would otherwise be subject to worst-case algebraic error summation; and second, that the geometry of an integrated module permits optimization of many signal paths that would otherwise be vulnerable to degradation, due to such effects as inter-module wiring parasitics, noise pickup, thermal EMF's, etc.

ANALOG INTERFACE FEATURES. As shown in figure 2, a choice of three input configurations are provided. In the simplest (2a), 16 single-ended inputs may be connected to the multiplexer, all referenced to ANALOG GND. Alternatively, the inputs may be presented, in 8 pairs, to the differential amplifier, merely by connecting MUX OUT LO terminal to the AMP IN LO terminal as shown in 2b. Finally, as shown in 2c, 16 "pseudo-differential" channels may be created, under favorable sensor-ground-path conditions, by using the AMP IN LO terminal as the ground-return point for all 16 sensors. (Note the constraint specified in figure 2c).

The multiplexer circuitry in the MP6912 is of very advanced design. Break-before-make switching eliminates interchannel transients and feedback of switching spikes. Very low per-channel capacitance minimizes source loading. Crosstalk, leakage, and offsets have all been reduced to negligible levels for sources having recommended impedance levels. The

MP---06912-6x

multiplexer is designed to protect both itself and its signal sources both from overvoltage failure and from fault currents due to power-off loading or MUX failure.

MUX and SAMPLE & HOLD DYNAMICS. The dynamic behavior of the multiplexer circuitry in the MP6912 fully supports the high data-throughput ratings discussed on page 6. Settling time and overshoot have been minimized, and large-signal slew rates exceed most requirements, even at the highest attainable data-throughput and channel-scanning speeds. Finally, the addressing and scan-control circuitry (which is discussed later) permits many useful variations of the scanning/sampling/conversion program.

The differential buffer amplifier and sample-hold circuitry that link the multiplexed inputs to the A/D converter may conveniently be discussed as an entity (after noting that the output of the differential amplifier is made available at terminal AMP OUT). Perhaps the most significant features of the sample-hold design are its very high speed, its very low aperture uncertainty, and its ability to operate in an "overlap" mode, in which a new channel address may be loaded into the multiplexer, selecting the next channel to be sampled, while the previously-acquired sample is being held for conversion. Statically, the amplifier/sample-hold circuit presents a very-high-impedance, very-low-current load to the active channel. The dynamic characteristics of the sample-hold circuit are shown in figure 3. Note particularly the very short acquisition and settling time, the exceptionally small aperture uncertainty, and the very slow hold decay for a sample-hold of this speed.

It is important to note that the full speed capabilities implicit in the parameters of figure 3 are actually available in the single-channel mode — i.e., when the multiplexer is held at a single address, which channel is repeatedly sampled. When the multiplexer's dynamic response must also be accounted for, the resultant (somewhat slower) data-throughput rates shown in figure 4 are attained.

The full-scale input range of the MP6912 may be set, by appropriate jumper interconnection of terminals, to any of eight different standard ranges:

0 to +10 V	0 to +5 V
0 to +10.24 V	0 to +5.12 V
−10 V to +10 V	−5V to +5 V
−10.24 V to +10.24 V	−5.12 V to +5.12 V

The 10.24 and 5.12 V levels are frequently convenient in that they yield conversion increments of exactly 5 mV/bit, 2.5 mV/bit, and 1.25 mV/bit.

The above ranges are all trimmable in either of two ways: by means of the internal gain-trimming potentiometer; or by means of an external gain-trimming potentiometer.

CONVERTER CHARACTERISTICS. The basic characteristics of the converter are given in the specification of page 7, but certain of the MP6912's features are worthy of study here. First of all, it is possible to "short-cycle" the converter, causing it to cease conversion after *less* than 12 bits, simply by connecting an external jumper between the Short Cycle terminal, and one of the output terminals. (Connection to the Nth output bit reduces conversion to N-1 bits; available resolution range is 2-12 bits). With these shorter cycles, the attainable data-throughput rate rises, as shown on curve A of figure 4. (The short-cycle terminal must be grounded for full 12-bit operation.)

The nominal clock rate of the converter may be externally trimmed over a range of approximately +80% −40%, as shown in figure 12, by varying the potential of the Clock Trim terminal, either by jumpering it to ground or +5 V, or by feeding it from the output of a potentiometer connected across +5 V and ground. But there are several other means that may be used to increase the maximum data-throughput rate of the MP6912. One of them, mentioned earlier, is to

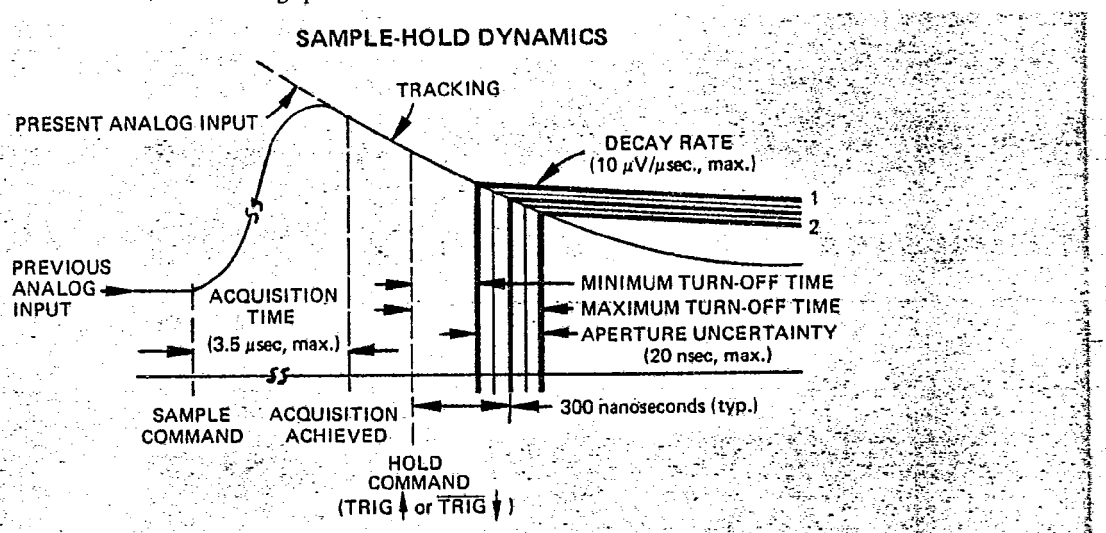


Figure 3. Sample-Hold parameters defined and specified.

MP---06912-7X

DESIGN FEATURES

use the overlap mode for the sample-hold/channel-scan sequence. This mode yields the speeds shown by curve B of figure 4. Still another gain in throughput rate is possible in *single-channel operation* (also mentioned earlier), the potential of which is shown by curve C of figure 4.

The output code of the converter may be jumper-selected, as shown on page 11, from any of the following codes:

- UNIPOLAR BINARY
- TWO'S COMPLEMENT
- OFFSET BINARY
- ONE'S COMPLEMENT

(See Code Chart on page 11 for details for all code and range combinations.)

As noted earlier, all digital outputs are *buffered*, to permit driving substantial resistive, capacitive, and active loads. Reflections from driven lines will not affect the bit flip-flops, which are isolated by the buffer amplifiers.

CONTROL/TIMING/PROGRAMMING FACILITIES. For a full appreciation of the versatility of the MP6912 in this regard, it is necessary to study figures 1 and 2 (pages 1 and 4), in conjunction with the timing diagrams on page 8. Here, however, are the highlights:

- **MUX Addressing.** Every useful terminal of the MUX-address counter is brought out, to facilitate system control. This counter/register circuit provides all of the following MUX-address modes:
  - Continuous sequential scanning, free-running.
  - Sequential scanning under external step command.
  - Single-pass sequential scanning, on command.
  - Random-access channel selection, by external address.
  - Abbreviated-scan (sequential), from 1-16 (or 1-8 differential) channels, continuously or in single passes, on command.

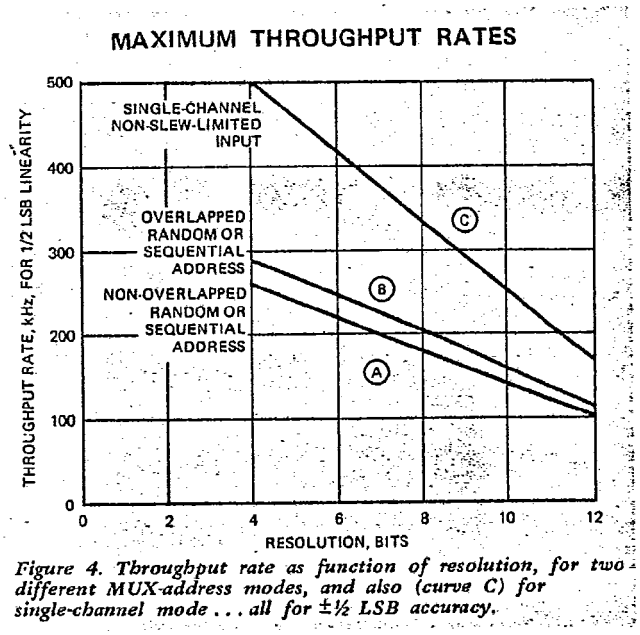


Figure 4. Throughput rate as function of resolution, for two different MUX-address modes, and also (curve C) for single-channel mode . . . all for ±½ LSB accuracy.

- **MUX Delay.** A particularly useful feature of the MP6912 is a built-in *adjustable* delay (see inside back cover), which is provided between the loading of the MUX address and the start of conversion, thus allowing time for the MUX and S/H to settle to the required accuracy . . . which is determined by the number of bits of resolution selected. This permits accurate arbitrary (external) strobing of the transition to a new channel and also establishes optimum and uniform timing for internally strobed, sequential addressing, transition, and sampling.
- **Conversion Controls.** The MP6912 may be placed in a continuous, free-running mode, or may be caused to hold a conversion until commanded to convert again. A conversion signal is provided for external control of other system elements.

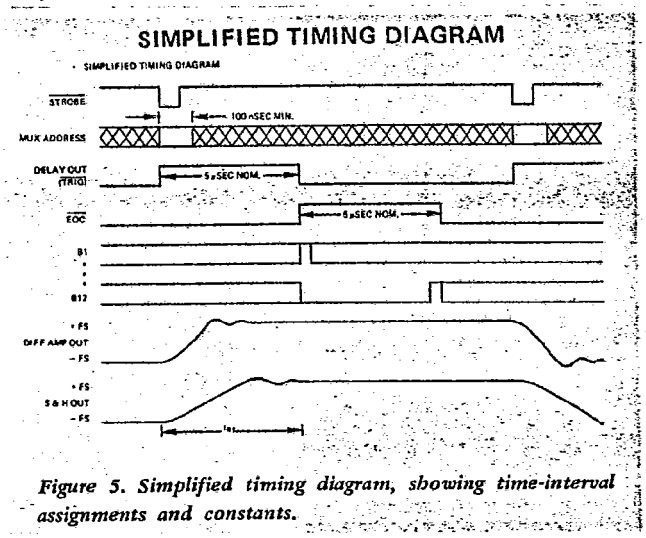


Figure 5. Simplified timing diagram, showing time-interval assignments and constants.

The simplified timing diagram of figure 5, above, shows the time constraints and sequence of events in the random-addressed mode. Note that 5 μsec (t_{01}) is assigned to the overall settling time of the MUX, buffer amplifier, and sample-hold acquisition, and another 5 μsec is allowed for a complete 12-bit conversion (B1 to B12). The diagrams on page 8 are more detailed, and describe the behavior of every control, address, output, and analog element in the data path. Figure 6 covers random and sequential addressing in the *non-overlap* mode (address held until conversion has been completed), and Figure 7 covers sequential addressing in the *overlap* mode (next address loaded while previous channel's signal is being converted).

MISCELLANEOUS DESIGN FEATURES include:

- Effective power-supply filtering, to prevent anomalous behavior due to noise or spikes.
- Effective Electrostatic and Electromagnetic Shielding.
- Compatibility with standard DC-DC power converters, computer interfaces, and standard multilevel MUX extenders (see back cover).

MP---06912-8X

SPECIFICATIONS

ANALOG INPUTS

Number of Inputs to Multiplexer	16 Single Ended, 8 True-Differential, 16 Pseudo-Differential
Input Voltage (Full Scale Range)	−10V to +10V, 0V to +10V, −5V to +5V, 0V to +5V, −10.24V to +10.24V, 0V to +10.24V, −5.12V to +5.12V, or 0V to +5.12V. (See page 11)
Maximum Input Voltage for Proper Operation (signal plus common mode)	−10.24V or +10.24V
Input Current (per channel)	< 1nA @ 25°C; 20nA @ 60°C
Input Impedance	> 100 Megohms
Input Capacitance	< 10pF for "off" channel; 100pF for "on" channel
Input Fault Current (power off or MUX failure)	Internally limited to 20mA
Direct ADC Input Impedance	5kΩ for each input line (see Fig. 1)

ACCURACY

Resolution	12 bits
Relative Accuracy	±0.025% FSR @ 100KHz thru-put rate (includes 5μsec for MUX settling and S & H acquisition time and 5μsec for A/D conversion time). ±0.015% FSR @ 50kHz thru-put rate (includes 9μsec for MUX settling and S& H acquisition time and 7.5μsec for A/D conversion time)
Absolute Accuracy	Same as relative accuracy (see page 12)
Inherent Quantizing Error	±½ LSB
3σ Noise (includes reference noise)	0.01% FSR P-P referred to input

STABILITY

Tempco of Linearity	< 3PPM FSR/°C
Tempco of Gain	< 12PPM FSR/°C
Tempco of Offset	< 0.001% FSR/°C
Power Supply Sensitivity	0.003% FSR/ % change in supply voltage

SIGNAL DYNAMICS

Maximum Throughput Rate (12 bits)	100,000 channels/sec (includes 3.5 μsec for MUX settling time, 3.5 μsec for S & H acquisition time, and 5 μsec for A/D conversion time) (see Note 2)
Sample and Hold Aperture Uncertainty	20nsec over temperature and signal amplitude
Crosstalk	80dB down at 1kHz "off" channels to "on" channel
Differential Amplifier CMRR	> 70dB (DC to 1 kHz)
Sample and Hold Feedthrough	80dB down at 1kHz
Maximum Error for F.S. to F.S. transition between successively addressed channels	1 LSB

DIGITAL INPUT SIGNALS (See Timing Diagram)

Compatibility	Standard DTL/TTL logic levels, 1 unit load/line, internal pull-up.
MUX Address Inputs (8, 4, 2, 1; Pins 19B thru 22B)	Positive true natural binary coding selects channel for random addressing mode. Must be stable for 100nsec after $\overline{\text{STROBE}}$
MUX ENABLE HI (Pin 18T)	High (logic "1") input enables MUX "HI" output (for inputs 0 thru 7)
MUX ENABLE LO (Pin 17B)	High (logic "1") input enables MUX "LO" output (for inputs 8 thru 15)
$\overline{\text{STROBE}}$ (Pin 24T or 25T)	Negative going transition (logic "1" to logic "0") updates MUX address register. $\overline{\text{STROBE}}$ 1 must be at logic "1" to enable $\overline{\text{STROBE}}$ 2. $\overline{\text{STROBE}}$ 2 must be at logic "1" to enable $\overline{\text{STROBE}}$ 1
$\overline{\text{LOAD ENABLE}}$ (Pin 24B)	High (logic "1") input allows next $\overline{\text{STROBE}}$ command to sequentially advance MUX address register
	Low (logic "0") input allows next $\overline{\text{STROBE}}$ command to update MUX address register according to external address inputs
$\overline{\text{CLEAR ENABLE}}$ (Pin 25B)	Low (logic "0") input allows next $\overline{\text{STROBE}}$ command to reset MUX address to channel "0" overriding $\overline{\text{LOAD ENABLE}}$.
TRIGGER (Pin 26T)	Positive going transition (logic "0" to logic "1") initiates A/D conversion (even during conversion); TRIGGER (Pin 27T) must be at logic "0" to allow TRIGGER function
$\overline{\text{TRIGGER}}$ (Pin 27T)	Negative going transition (logic "1" to logic "0") initiates A/D conversion; Pin 26T (TRIGGER) must be at logic "1" to allow $\overline{\text{TRIGGER}}$ function

DIGITAL OUTPUT SIGNALS (See Timing Diagram)

Compatibility	Standard DTL/TTL logic levels; 5 unit loads/line (up to a total of 36 unit loads)
Parallel Outputs (buffered)	$\overline{\text{B1}}$, B1 thru B12
Coding	Natural binary, two's complement, offset binary, or one's complement. Pin selectable (see page 11)
MUX Address Outputs (8, 8, 4, 2, 1; pins 18B, 19T thru 22T)	Positive true natural binary coding indicates channel selected
DELAY OUT (Pin 23T)	Negative going transition (logic "1" to logic "0") occuring nominally 5μsec (adjustable from 2.5 μsec to 10 μsec, see Fig. 13) after $\overline{\text{STROBE}}$ command. See timing diagram Fig. 6. Connect to TRIGGER to automatically initiate A/D conversion
$\overline{\text{EOC}}$ (Pin 27B)	High (logic "1") output during A/D conversion

ADJUSTMENTS

Offset Adjust	Externally accessible internal adjustment or remote external adjustment calibrates zero offset. See p. 12, Fig. 10. Use with RANGE ADJ to calibrate absolute accuracy
Range Adjust	Externally accessible internal adjustment or remote external adjustment calibrates range See p. 12, Fig. 11. Use with OFFSET ADJ to calibrate absolute accuracy

CONTROLS

CLOCK TRIM (Pin 26B)	Clock period factory set to 400nsec/bit, nom. Can be adjusted externally (see Fig. 12).
DELAY TRIM (Pin 23B)	Delay interval after $\overline{\text{STROBE}}$ falling edge is factory set to 5μsec, nom. Can be adjusted externally (see fig. 13).
SHORT CYCLE (Pin 28T)	Connect to ground for full 12 bit resolution. Connect to B_n output for resolution to B_{n-1} bits
Channel Selection Mode (MUX Address Loading Mode)	Random, sequential continuous, and sequential triggered. Pin selectable (see page 10)
A-D Conversion/Channel-Select Sequence	Normal (input channel remains selected during its A/D conversion) and overlap (next channel selected during A/D conversion). Pin selectable (see page 11)
Range Select (Pin 12T)	Differential Amplifier gain control: connect to ANA RTN (Pin 2T) for X1 gain; connect to AMP OUT (Pin 13B) for X2 gain. This control is used in FSR selection procedure (see page 11)
BINARY SCALE (Pin 15B)	Connect to REF ADJ (Pin 16B) to set reference to 10.24V. This control is used in FSR selection procedure.
OUTPUT CODING (Pin 17T)	Ground for 1's complement output code; connect to −15VDC for other available codes (see page 11)

POWER REQUIREMENTS

+15V ±3%	60mA
−15V ±3%	80mA
+ 5V ±5%	300mA

ENVIRONMENT & PHYSICAL

Operating Temperature	0° to 60°C
Storage Temperature	−25°C to +85°C
Relative Humidity	Up to 95% non-condensing
Electrical Shielding	RFI & EMI 6 sides (except connector area)
Packaging	Insulated steel case 3.00 x 4.6 x 0.375 inches

Analogic may upgrade these specifications at any time.
Note 1: The recommended recalibration interval is 6 months.
Note 2: MUX and S & H settling time is $\sqrt{3.5^2 + 3.5^2} = < 5$ μsec.

ORDERING GUIDE

Simply Specify — MP6912, for complete system module, including all facilities shown in Figure 1, page 1. (Shipped complete with mating right angle connector.)

Optional Accessories — Also see back cover.

AN87 Programmable PC-card/connector assembly. Contains all necessary facilities (less power supply) for complete check-out and use of MP6912 and is laid out to minimize input signal interference.

MP--06912-9X

TIMING DIAGRAMS

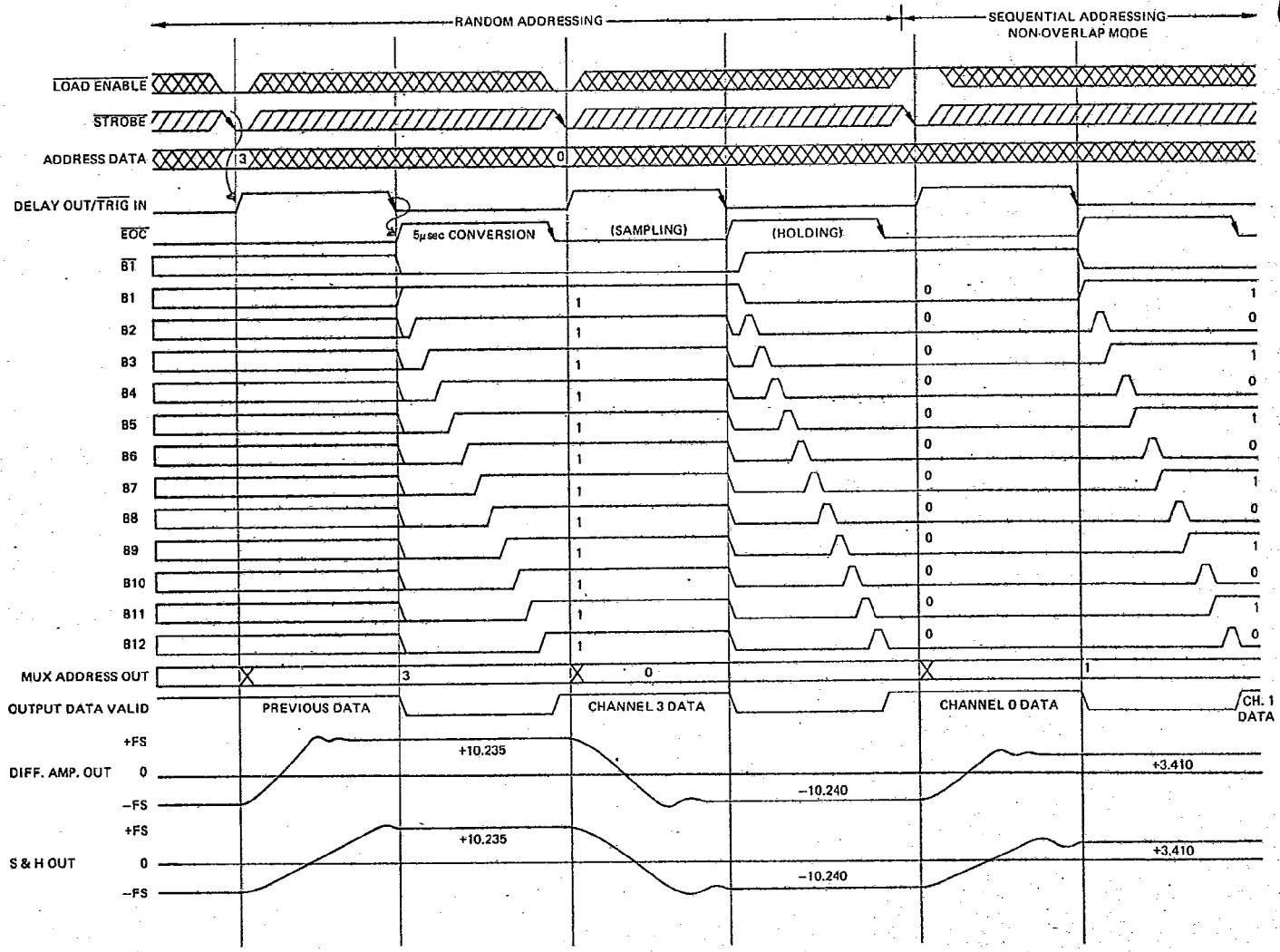


Figure 6. Timing for non-overlap operation in both random and sequential addressing modes. For status keys and signal condition data, refer to box below.

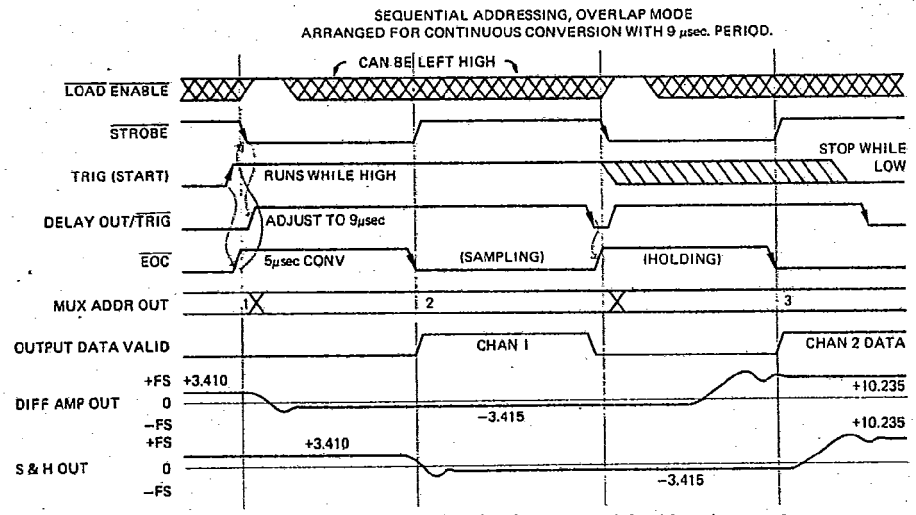


Figure 7. Timing diagram for overlap operation in the sequential addressing mode. For status keys and signal condition data, see box at right.

SIGNAL CONDITIONS AND STATUS KEYS FOR FIGURES 7 AND 8.

CH. 2 = –3.415 V. CODE 010 101 010 101
CH. 3 = +10.235 V. CODE 111 111 111 111
CH. 0 = –10.240 V. CODE 000 000 000 000
CH. 1 = +3.410 V. CODE 101 010 101 010

ADC SET UP FOR ±10.24 V. INPUT, OFFSET BINARY. (FOR TWO'S COMPLEMENT, USE $\overline{B1}$ FOR M.S.B.)

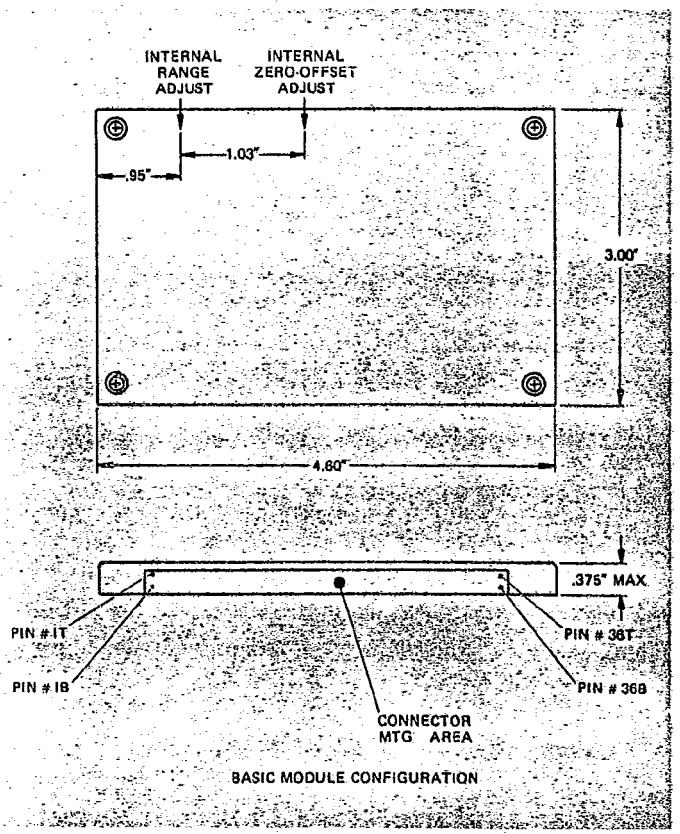
KEY	INPUTS	OUTPUTS
XXX	MAY CHANGE	DON'T KNOW
///	MAY CHANGE 0 TO 1	CHANGES 0 TO 1
\\\	MAY CHANGE 1 TO 0	CHANGES 1 TO 0
OR	MUST BE STABLE	WILL BE STABLE

MP---06912-10X

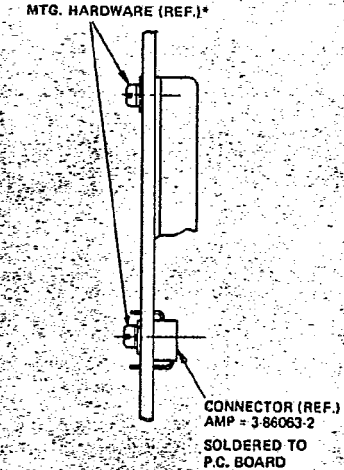
OUTLINE DRAWINGS & PIN CONNECTIONS

MP6912 Connector Pin Diagram

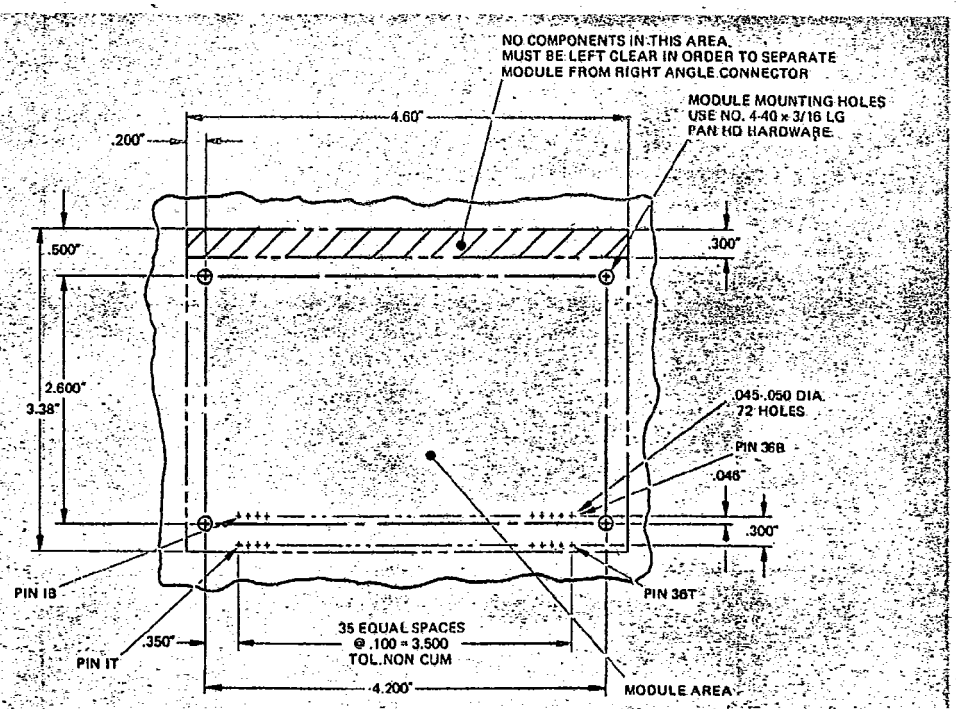
+15V	1T	1B	−15V
ANA RTN	2T	2B	ANA RTN
CH 0 IN	3T	3B	CH 8 IN (CH 0 RTN)
CH 1 IN	4T	4B	CH 9 IN (CH 1 RTN)
CH 2 IN	5T	5B	CH 10 IN (CH 2 RTN)
CH 3 IN	6T	6B	CH 11 IN (CH 3 RTN)
CH 4 IN	7T	7B	CH 12 IN (CH 4 RTN)
CH 5 IN	8T	8B	CH 13 IN (CH 5 RTN)
CH 6 IN	9T	9B	CH 14 IN (CH 6 RTN)
CH 7 IN	10T	10B	CH 15 IN (CH 7 RTN)
MUX HI OUT	11T	11B	MUX LO OUT
RANGE SEL	12T	12B	AMP IN LO
S & H OUT	13T	13B	AMP OUT
ADC IN 1	14T	14B	ADC IN 2
+10V REF	15T	15B	BINARY SCALE
EXT OFFSET	16T	16B	REF ADJ
OUTPUT CODING	17T	17B	ENABLE LO
ENABLE HI	18T	18B	$\overline{8}$ OUT
8 OUT } MUX	19T	19B	8 IN } MUX
4 OUT } ADDRESS	20T	20B	4 IN } ADDRESS
2 OUT } LINES	21T	21B	2 IN } LINES
1 OUT }	22T	22B	1 IN }
DLY OUT	23T	23B	DLY TRIM
STROBE 1	24T	24B	LOAD ENB
STROBE 2	25T	25B	CLR ENB
TRIG	26T	26B	CLK TRIM
$\overline{\text{TRIG}}$	27T	27B	EOC
SHT CYC	28T	28B	$\overline{\text{B1}}$ OUT
B1 OUT	29T	29B	B2 OUT
B3 OUT	30T	30B	B4 OUT
B5 OUT	31T	31B	B6 OUT
B7 OUT	32T	32B	B8 OUT
B9 OUT	33T	33B	B10 OUT
B11 OUT	34T	34B	B12 LSB OUT
DIG RTN	35T	35B	DIG RTN
+5V	36T	36B	+5V



BASIC MODULE CONFIGURATION



*MP6912 plugs into connector and is held in position by four mounting screws. Insulated case can be mounted on two-sided P.C. board without shorting etch.



P. C. BOARD LAYOUT (COMPONENT SIDE)

MP---06912-11X

RECOMMENDED 8-STEP SET-UP PROCEDURE

1 Select input configuration

Connect all *unused* input terminals to ANA RTN (Pin 2B or 2T).

INPUT CONFIGURATIONS	ANALOG INPUT CONNECTIONS	ANALOG INPUT RETURN	JUMPER CONNECTIONS
16-Single-Ended Inputs (Figure 2a)	3T thru 10T and 3B thru 10B	All input returns to 2B or 2T	11B to 11T 12B to 2B or 2T 17B to 19T 18T to 18B
8 Differential Inputs (Figure 2b)	3T through 10T	3B through 10B	11B to 12B
16 Pseudo-Differential Inputs (Figure 2c)	3T thru 10T and 3B thru 10B	Common input return to 12B	11B to 11T 17B to 19T 18T to 18B

Grounding Considerations. In order to minimize noise pick-up, ground loop currents and ground-path voltage drops, careful attention must be paid to how the electrical returns and voltage reference points are connected. (The MP6912 provides internal connection for ANA RTN and DIG RTN.) A typical system using the model MP6912 has several "grounds" which include:

1. ±15V Return
2. +5V Return
3. Signal Returns
4. Computer Ground
5. Chassis
6. Third-Wire Ground

Each of these must be connected correctly to the system. The following rules generally apply:

1. If the ±15V power supply is floating (a good idea for optimum analog accuracy), connect its return to ANA RTN (Pin 2B or 2T). If the ±15V power supply is *not* floating, connect its return to DIG RTN (Pin 35T or 36T).
2. Connect the +5V supply return to DIG RTN (Pin 35T or 36T). If this supply also powers additional equipment (i.e. a computer), run *separate, parallel returns* to the equipment ground and to DIG RTN (Pin 35T or 36T).
3. To minimize signal grounding problems, single-ended input signals should only be returned to ANA RTN (Pin 2B or 2T). If this is not possible, then connect the input signals in either the "true differential" or "pseudo-differential" configurations (see Figure 2, page 4).
4. Connect computer ground, generally the return for the digital I/O signals, to DIG RTN (Pin 35T or 35B). Use heavy wire (#14AWG), or ground planes.
5. The computer chassis should be connected to the computer and power supply grounds at only one point. If this is not possible, a ground loop will exist. Its effect can be minimized by assuring that the components of the loop (i.e. chassis to MP6912 ground, MP6912 to ±15V supply ground, and the chassis to ±15V supply ground) are physically as close as possible.
6. Connect the third-wire ground from main AC power input to the computer power supply return.

2 Select MUX address-loading mode

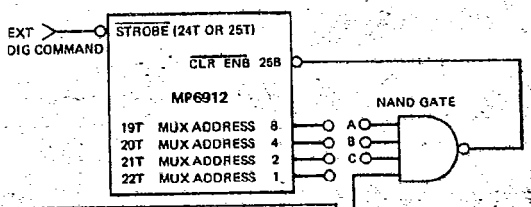
The method of addressing the multiplexer can be selected by connecting the unit as follows:

RANDOM. Set Pin 24B (LOAD ENB) to logic "0." The next falling edge of STROBE will load the address presented to Pins 19B thru 22B (8, 4, 2, 1). The code on these lines must be stable during the falling edge of STROBE plus 100 nsec.

SEQUENTIAL FREE RUNNING. Float or set to logic "1" Pin 24B (LOAD ENB) and 25B (CLR ENB). Connect Pin 27B (EOC) to Pin 24T (STROBE 1). Connect Pin 23T (DLY OUT) to Pin 27T (TRIG). Use Pin 26T (TRIG) as a run/stop control (i.e. channel selection – A/D conversion will continue while TRIG is high and will stop while TRIG is low).

SEQUENTIAL TRIGGERED. Float or set to logic "1" Pins 24B (LOAD ENB) and 25B (CLR ENB). Connect Pin 24T (STROBE) to external triggering source. The multiplexer address register will automatically advance by one channel whenever a STROBE command is received. The initial channel can be selected by setting Pin 24B (LOAD ENB) to logic "0" during only one STROBE command. The multiplexer address will then be determined by the logic levels on Pins 19B thru 22B (the external MUX address lines). Channel "0" can be selected as the initial channel by setting Pin 25B (CLR ENB) to logic "0" during only one STROBE command. The final channel can be selected by following the procedure presented in Figure 8.

MUX SCAN-CONTROL CONNECTIONS



LAST CHANNEL	MUX ADDRESS 8	4	2	1	DIG. GROUND
1	X	X	X	A	X
2	X	X	B	X	X
3	X	X	B	A	X
4	X	C	X	X	X
5	X	C	X	A	X
6	X	C	B	X	X
7	X	C	B	A	X
8	C	X	X	X	X
9	C	X	X	A	X
10	C	X	B	X	X
11	C	X	B	A	X
12	B	C	X	X	X
13	B	C	X	A	X
14	A	C	B	X	X
15	X	X	X	X	A

X = NO CONNECTION

If LOAD ENB. is also used, connect this input to it (to 24B). This gives loading preference over clearing.

Note: For initial channel = M, connect gate output to LOAD ENB. (24B) and code channel in 8, 4, 2, 1 to address M; however, this precludes random addressing.

Figure 8. To shorten scanning sequence of multiplexer channels, make the appropriate connections, (as shown in the chart) between an external NAND gate and MUX ADDRESS terminals 19T to 21T.

MP---0691 2-12

3 Select A-D Conversion/Channel-Select sequence (see Fig. 4)

a. Normal (input channel remains selected during its A/D conversion)
b. Overlap (next channel is selected during A/D conversion) as shown below.
c. Repetitive Single Channel

1. NORMAL (input channel remains selected during its A/D conversion). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$).

2. OVERLAP (next channel is selected during A/D conversion). Connect Pin 27B ($\overline{\text{EOC}}$) to TTL compatible inverter input. Connect inverter output to Pin 24T ($\overline{\text{STROBE}}$). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$). Adjust the delay to 9 μsec (See Fig. 13). The signal on Pin 26T (TRIG) serves as RUN/STOP control.

3. REPETITIVE SINGLE CHANNEL. After selecting the input channel to be repetitively sampled (see MUX ADDRESS LOADING MODE, above), set Pin 27T ($\overline{\text{TRIG}}$) to logic "0". Connect Pin 26T (TRIG) to a triggering source. Conversion process is initiated by positive edge of TRIG command.

4 Select output resolution

a. Full 12 bit resolution: connect Pin 28T (SHT CYC) to Pin 35B (DIG RTN).

b. Bn (Bn < 12) bit resolution: connect Pin 28T to the output pin for Bn+1.

5 Select optimum thru-put rate

The system clock frequency and the $\overline{\text{STROBE}}$ to $\overline{\text{TRIG}}$ delay (if used) can be trimmed to optimize the accuracy/thru-put rate trade-off. See Figs. 12 and 13, under CALIBRATION PROCEDURE, facing page 12.

6 Select input voltage full scale range

FOR FULL-SCALE RANGE OF:	MAKE THE FOLLOWING CONNECTIONS:
0 to +10V	12T to 2T; 14T and 14B to ADC Source.*
0 to +10.24V	same as 0 to +10V, *plus* 15B to 16B.
0 to +5V	12T to 13B; 14T and 14B to ADC Source.*
0 to +5.12V	same as 0 to +5V, *plus* 15B to 16B
−10V to +10V	12T to 2T; 14T to 15T; and 14B to ADC Source.*
−10.24V to +10.24V	same as −10V to +10V, *plus* 15B to 16B.
−5V to +5V	12T to 13B; 14T to 15T; and 14B to ADC Source.*
−5.12V to +5.12V	same as −5V to +5V, *plus* 15B to 16B.

*ADC Source is usually Sample and Hold Output (13T), but may be any signal source including Diff Amp Output (13B) if Sample and Hold is not desired.

7 Select output digital coding

OUTPUT CODE SELECTION

CODE	CONNECTIONS
Unipolar Binary	Connect 17T to −15V Use 29T (B1) for MSB
2's Complement	Connect 17T to −15V Use 28B ($\overline{\text{B1}}$) for MSB
Offset Binary	Connect 17T to −15V Use 29T (B1) for MSB
1's Complement	Connect 17T to 2B Use 28B ($\overline{\text{B1}}$) for MSB

12-BIT OUTPUT CODING (FOR 10V F.S. RANGE)*

Unipolar binary:

	B1, B2 ...			B12
+9.9976V =	111	111	111	111
0.0000V =	000	000	000	000

Two's Complement:

	$\overline{\text{B1}}$, B2 ...			B12
+9.9951V =	011	111	111	111
0.0000V =	000	000	000	000
−10.0000V =	100	000	000	000

Offset Binary:

	B1, B2 ...			B12
+9.9951V =	111	111	111	111
0.0000V =	100	000	000	000
−10.0000V =	000	000	000	000

One's Complement:

	$\overline{\text{B1}}$, B2 ...			B12
+9.9951V =	011	111	111	111
0.0000V =	000	000	000	000
0.0000V =	111	111	111	111
−9.9951V =	100	000	000	000

*For 5V ranges, divide analog voltage by 2; for 5.12V ranges, multiply analog voltages by 0.512; and for 10.24V ranges, multiply analog voltages by 1.024.

8 Connect power supplies

Use power supplies that meet or exceed the regulation and output requirements established in the SPECIFICATIONS, page 7. See the discussion of Grounding Considerations, in Step 1, page 10. For optimum stability, a tantalum capacitor ≥ 47 μF, 20 V, should be connected between +10 V REF (Pin 15T) and ANA RTN (Pin 2B/2T).

MP---06912-13x

MULTIPLEXER EXPANSION

CALIBRATION

Figure 9 shows the interconnection scheme for expanding the basic multiplexer channel capacity of an MP6912 (16 single-ended/8 differential/16 psuedodifferential) to a total of 256 single-ended or psuedodifferential channels. For this capacity, 8 Analogic MUX-expansion modules (MP6932) are added (externally) to the MP6912 and powered appropriately.

The level of expansion shown is arbitrary; the expansion module provides 32 channels, and any number of modules up to 8 can be added. Other interconnection schemes can be used to generate up to 128 differential inputs. Consult Analogic for further documentation on expansion.

The MP6932 optionally provides, in addition to expansion, a capability for programmable gain as well as autozeroing of the front end. The following versions are available:

MP6932-version	Contains
-1	32 channels of MUX expansion, logic programmable amplifier, autozero loop
-2	programmable amplifier, autozero loop
-3	32 channels of MUX expansion

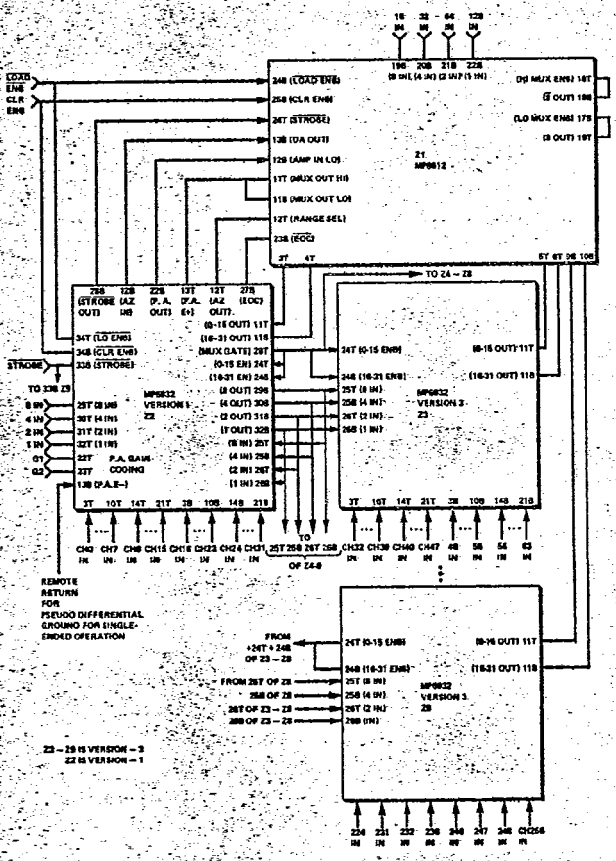


Figure 9. Simplified diagram showing the use of external MUX-expansion modules to increase the channel capacity of an MP6912.

Absolute Accuracy

The rated linearity and relative accuracy of the MP6912 are ensured by component and circuit integrity. *Absolute* accuracy is established by calibrating the zero offset and full-scale range. This is accomplished either locally, by adjusting externally accessible built-in trimming potentiometers; or remotely, by means of the external trimming circuitry shown in Figures 10 and 11.

Zero Offset

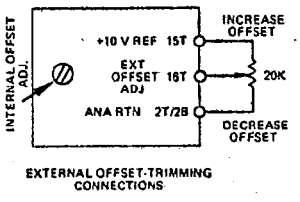
To recalibrate the OFFSET: Apply the input voltage shown in the accompanying table, and adjust the OFFSET control so that the LSB of the output codes listed in the table alternates equally between "1" and "0". Offset should be readjusted whenever the selected range is changed.

RANGE	INPUT	OUTPUT CODE ($B_1, B_2 \ldots B_{12}$)			
−10V to +10V	+0.0024V	100	000	000	000/1
−10.24V to +10.24V	+0.0025V				
0V to +10V	+0.0012V	000	000	000	000/1
0V to +10.24V	+0.0013V				
−5V to +5V	+0.0012V	100	000	000	000/1
− 5.12V to +5.12V	+0.0013V				
0V to +5V	+0.0006V	000	000	000	000/1
0V to +5.12V	+0.0006V				

Range (OFFSET should be trimmed before adjusting RANGE)

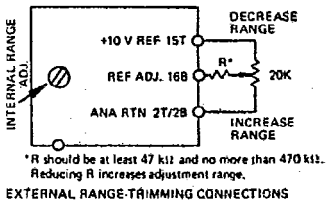
To recalibrate the RANGE: Apply the input voltage shown in the accompanying table, and adjust the RANGE control so that the LSB of the output code alternates equally between "1" and "0". Range should be readjusted whenever the selected range is changed.

−10V to +10V	+ 9.9927V	111	111	111	110/1
−10.24V to +10.24V	+10.2325V				
0V to +10V	+ 9.9853V				
0V to +10.24V	+10.2363V				
− 5V to +5V	+ 4.9853V				
− 5.12V to +5.12V	+ 5.1163V				
0V to +5V	+ 4.9927V				
0V to +5.12V	+ 5.1182V				



EXTERNAL OFFSET-TRIMMING CONNECTIONS

Figure 10.



*R should be at least 47 kΩ and no more than 470 kΩ. Reducing R increases adjustment range.

EXTERNAL RANGE-TRIMMING CONNECTIONS

Figure 11.

MP---06912-14

PROCEDURE

Clock Rate

The clock rate may be adjusted for best conversion time/accuracy trade-off. The conversion time is varied by means of the external circuitry shown in Figure 12. An open CLK TRIM terminal (Pin 26B) results in 400 nsec/bit nominal conversion time. A grounded CLK TRIM terminal (for highest accuracy) results in a conversion time of more than 625 nsec/bit.

Delay Time

The DLY OUT signal may be adjusted to vary the A/D converter triggering time by means of the external circuitry shown in Figure 13. An open DLY TRIM terminal (Pin 23B) results in a nominal delay time of 5 μsec. A grounded DLY TRIM terminal (for highest accuracy) results in more than 9μsec of delay time.

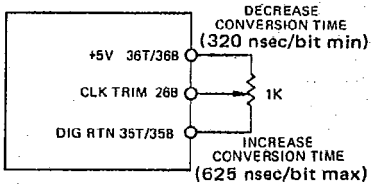


Figure 12.

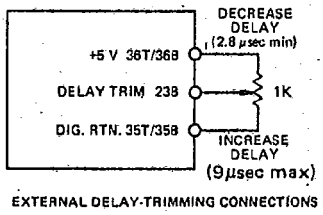


Figure 13.

CHECKOUT PROCEDURE

Operation of the MP6912 can easily be demonstrated by implementing the connections listed in Table I. These connections set the following functional conditions:

A. Single-ended input configuration with only channel "0" selected
B. Normal A/D conversion — channel-select sequence
C. 12-bit output resolution at 100,000 kHz max. thru-put rate
D. −10V to +10V input-voltage full-scale range
E. 2's complement output digital coding (use $\overline{B1}$ as MSB)

The outputs, Pins 28B thru 34B and 30T thru 34T, may be monitored. The output code now represents the input signal level. Calibration procedure is given above. Following calibration, the MP6912 may be exercised in the following ways:

1. Linearity and monotonicity may be verified by varying the input signal over the allowable range.
2. Other output codes may be selected by following Set-Up Procedure Step 7 on page 11.
3. Other full scale ranges may be selected by following Set-Up Procedure Step 6 on page 11.
4. True differential or pseudo-differential input configurations may be selected by following Set-Up Procedure Step 1 on page 10.
5. Other input channels may be selected by connecting them to the signal source.

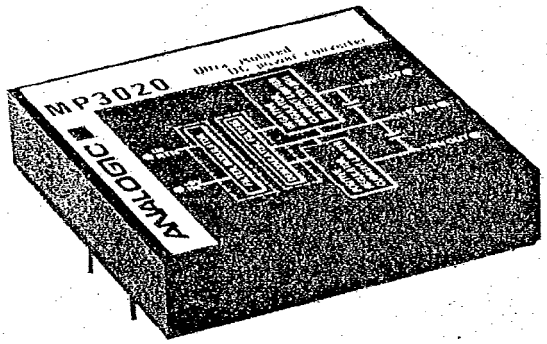
TABLE I

CONNECTION	FUNCTION
1. Jumper Pin 17B to 19T, 18T to 18B	Sets multiplexer for 16 channel operation
2. Jumper Pin 12B to 2B	Grounds Low Differential amplifier input
3. Jumper Pin 11B to 11T	Connects both MUX outputs together for 16 channel operation
4. 12T to 2T, 14T to 15T 14B to 13T	Sets input voltage range to ±10V
5. 17T to 1B	Sets output coding to 2's complement (use $\overline{B1}$ as MSB)
6. 25B to 35T	Keeps MUX address lines on logic "0". Set to logic "1" for sequencing.
7. 23T to 27T	Delays A/D conversion for 5 μsec
8. 28T to 35T	Sets resolution to 12 bits
9. Connect +15 to Pin 1T, −15V to 1B, +5V to 36T, power returns to 35T,	Powers the system
10. Jumper Pins 4T thru 10T and 3B thru 10B to 2T	Grounds channels 1 thru 15
11. Connect a stable, accurate bipolar DC, adjustable signal source (e.g., Analogic's AN3100 SECONDARY DC VOLTAGE STANDARD) between input terminals 3T (IN0) and 2T (ANA RTN)	Connects channel 0 to input signal
12. Connect trigger source (convenient rep rate is 1 KHz) to Pin 24T	Initiates data acquisition/conversion process

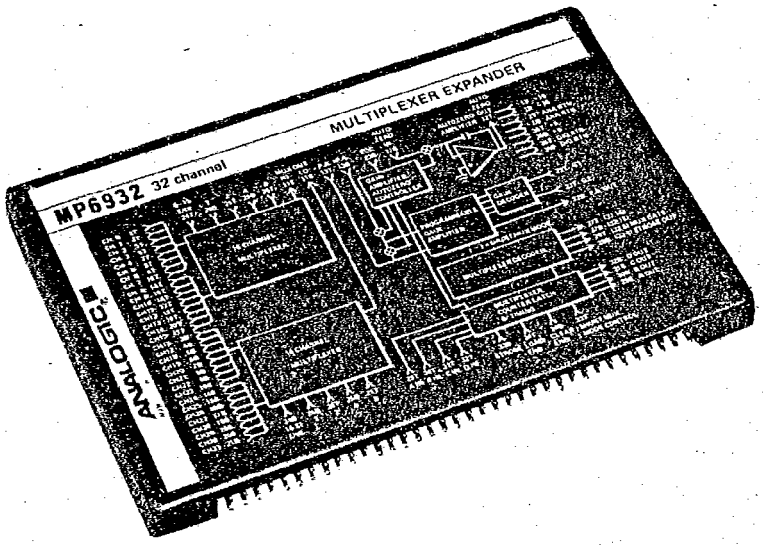
MP---06912-15X

OPTIONAL ACCESSORIES

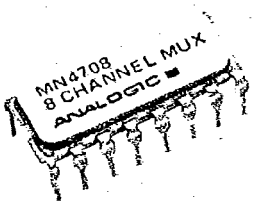
30



MP3020 DC POWER CONVERTER — a tightly regulated, very stable, 0.375-inch high supply ideal for driving analog circuitry from digital logic 5V power sources. Output capacity is 150 milliamperes at +15 and −15V, at an efficiency of 65 percent. Regulation is 0.1 percent for a full-load change.



MP6932 MUX EXPANDER — provision for expanding from the original 12 channels of the MP6912 to a total of 48 channels. Optionally available with the expander are provisions for programmable gain and for autozeroing of the front end to reduce internal drift errors essentially to zero before the start of each A/D conversion. Three versions are available: MP6932-1, 32 channels of mux expansion, logic, programmable gain amplifier, and autozero loop; MP6932-2, programmable amplifier and autozero loop only; MP6932-3, 32 channels of mux expansion only.



MN4708 MUX EXPANDER — an 8 channel analog multiplexer packaged in a standard 16-pin, dual-in-line case. A high-speed CMOS design, the MN4708 features leakage current of 0.1nA, access time of 250ns, total power dissipation of 200mw, and an "on" resistance of 250 ohms.

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MP---06912 - 16X

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