MP2790

4-Cell to 10-Cell, High-Accuracy Battery Monitor and Protector with Coulomb Counting

DESCRIPTION

The MP2790 is a robust battery management device, providing a complete analog front-end (AFE) monitoring and protection solution. It is designed for multiple-cell series battery management systems (BMS). The device can support I²C or serial peripheral interface (SPI) communication. It supports connections for 4-cell to 10-cell series battery packs, with an absolute voltage exceeding 80V on particular pins.

The MP2790 integrates two separate analog-to-digital converters (ADCs). The first ADC measures each channel's differential cell voltage (up to 10 channels), die temperature, and 4-channel temperatures via external NTC thermistors. The second ADC measures the current via an external current-sense resistor. The dual ADC architecture enables synchronous voltage and current measurements for cell and pack impedance monitoring.

When paired with an MPF4279x fuel gauge, the MP2790 can achieve state-of-charge (SOC) error to within 2%.

The MP2790 includes high-side MOSFET (HS-FET) drivers for charge and discharge independent control. The discharge (DSG) MOSFET driver includes a configurable soft start (SS) that provides a controlled turn-on, eliminating the need for an external pre-charge circuit. The DSG MOSFET driver incorporates protections such as discharging over-current (DOC), short-circuit (SC), battery under-voltage (UV), over-temperature (OT), and under-temperature (UT) protection. The CHG MOSFET driver incorporates protections such as charging over-current (COC), SC, and battery over-voltage (OV), UT, and OT protection. All of these protections have configurable thresholds.

Internal passive balancing MOSFETs can be used to equalize mismatched cells, supporting up to 58mA. There is also the option to drive external balancing transistors (MOSFET or BJT).

The MP2790 is available in a TQFP-48 (7mmx7mm) package.

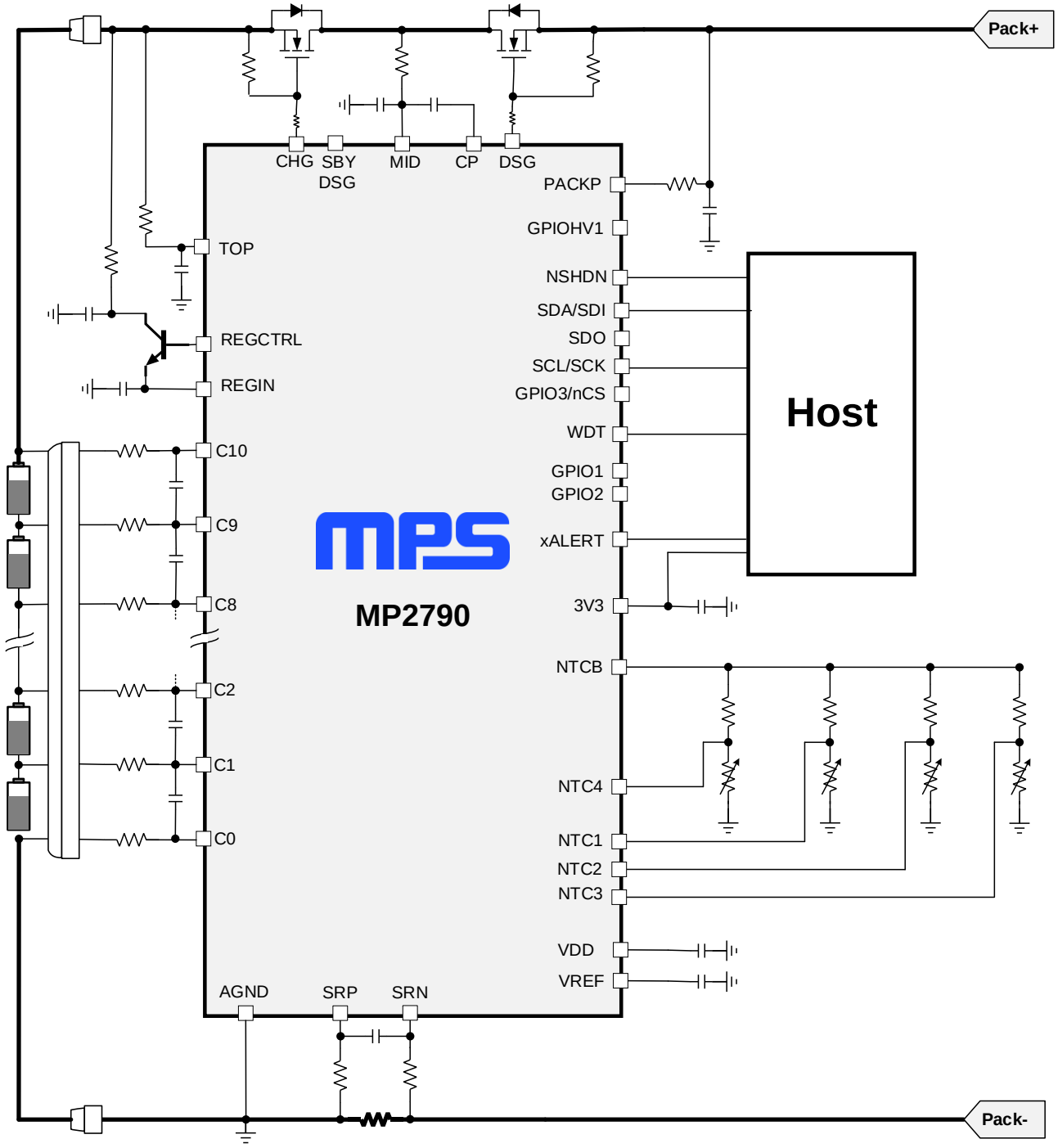
FEATURES

- Incorporates Dual ADC Architecture:
  - <±2% State-of-Charge (SOC) Error with MPF4279x Fuel Gauge
  - Cell Voltage Measurement Error <5mV
  - Current/Coulomb Counter Error <±0.5%
  - Strictly Synchronized Current/Voltage Measurement for Impedance Sensing
- Includes High-Side N-Channel MOSFET Drivers for Charge and Discharge Control:
  - Supports FET Soft-Start Discharge Control to Eliminate Pre-Charge Circuit
  - Drives Up to 100A DC with Parallel N-Channel MOSFETs
- Hardware Configurable Protections with Recovery Option:
  - Charge/Discharge OC and SC
  - Cell UV and OV
  - Pack UV and OV
  - Cell UT and OT
  - Die High-Temperature Protection
- Passive Cell Balancing up to 58mA per Cell:
  - Can Drive External Balancing Transistors
  - Automatic or Manual Control
- Additional Features:
  - Integrated 3.3V and 5V LDOs
  - Load and Charger Plug-In Detection
  - High-Voltage and Low-Voltage GPIOs
  - Dedicated Thermistor Inputs
  - Open Wire Detection
  - Persistent Dead Battery Flag
  - Lockable MTP for Key Thresholds
- I²C or SPI Interface with 8-Bit CRC
- Random Cell Connection Tolerant
- Available in a TQFP-48 (7mmx7mm) Package

APPLICATIONS

- E-Bikes, E-Scooters
- Light Electric Vehicles (LEVs)
- Power and Gardening Tools
- Battery Backups and UPS

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating	Communication
MP2790DFP-xxxx**	TQFP-48 (7mmx7mm)	*See Below*	3	-
MP2790DFP-0000	TQFP-48 (7mmx7mm)	*See Below*	3	I^2C
MP2790DFP-0002	TQFP-48 (7mmx7mm)	*See Below*	3	SPI
EVKT-MP2790-0000	Evaluation kit	N/A	N/A	N/A

* For Tray, add suffix -T (e.g. MP2790DFP-xxxx-T).

** “xxxx” is the configuration code identifier for the register settings. Each “x” can be a hexadecimal value between 0 and F. The default codes are “0000” and “0002” for I^2C communication and SPI communication, respectively. Contact an MPS FAE to create this unique number.

TOP MARKING (MP2790)

MPSYYWW
MP2790
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP: MPS prefix
2790: Part number
LLLLLLLLL: Lot number

EVALUATION KIT EVKT-MP2790-0000

EVKT-MP2790-0000 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2790-0000-FP-00B	MP2790DFP-0000 I^2C evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

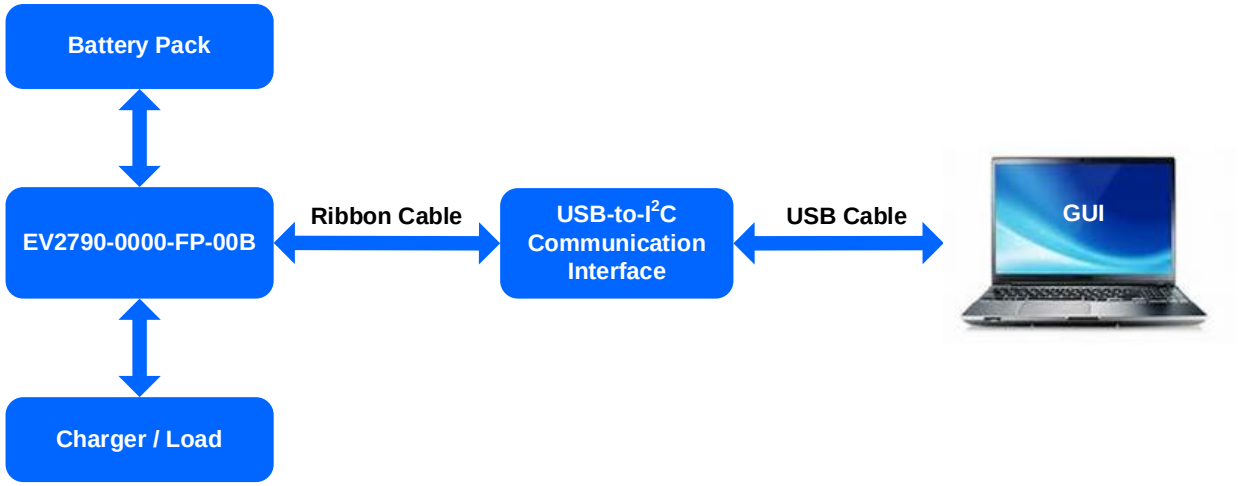
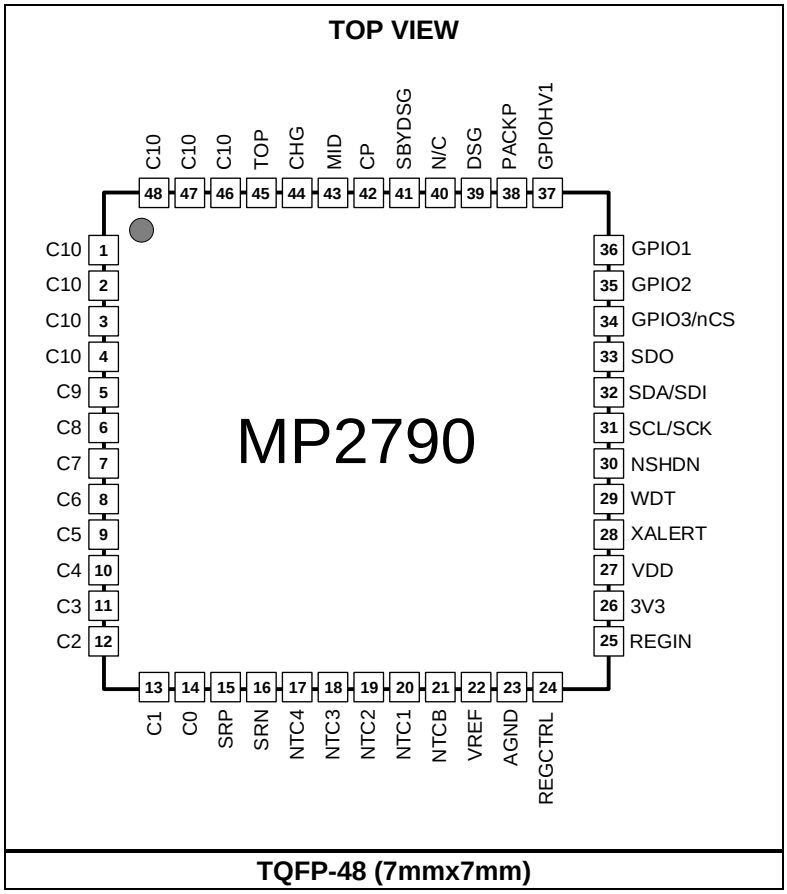


Figure 1: EV2790-0000-FP-00B Evaluation Kit Set-Up

PACKAGE REFERENCE



TQFP-48 (7mmx7mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
26	3V3	P	**3.3V voltage output to drive external peripherals.** Bypass 3V3 with an external 1µF capacitor.
23	AGND	P	**Ground.** Connect AGND near the positive connection (SRP) of the low-side sense resistor.
45	TOP	P	**Connect to the positive of battery pack and Low-current positive supply pin.** TOP must be connected to the top of the battery stack, which is the highest positive voltage in the battery pack.
1, 2, 3, 4, 46, 47, 48	C10	I	**Connect to the positive pin of cell 10.**
5	C9	I	**Connect to the positive pin of cell 9.**
6	C8	I	**Connect to the positive pin of cell 8.**
7	C7	I	**Connect to the positive pin of cell 7.**
8	C6	I	**Connect to the positive pin of cell 6.**
9	C5	I	**Connect to the positive pin of cell 5.**
10	C4	I	**Connect to the positive pin of cell 4.**
11	C3	I	**Connect to the positive pin of cell 3.**
12	C2	I	**Connect to the positive pin of cell 2.**
13	C1	I	**Connect to the positive pin of cell 1.**
14	C0	I	**Connect to the negative pin of cell 1.**
44	CHG	O	**Charge MOSFET driver.**
39	DSG	O	**Discharge MOSFET driver.**
36	GPIO1	I/O	**General-purpose pin 1.**
35	GPIO2	I/O	**General-purpose pin 2.**
37	GPIOHV1	I/O	**General-purpose, high-voltage pin 1.**
30	NSHDN	I	**Active-low shutdown input signal.**
20	NTC1	I	**Thermistor 1 terminal.**
19	NTC2	I	**Thermistor 2 terminal.**
18	NTC3	I	**Thermistor 3 terminal.**
17	NTC4	I	**Thermistor 4 terminal.**
21	NTCB	O	**NTC bias.**
40	N/C		**Not connected.**
38	PACKP	I/O	**Pack-sensing voltage (load-side).**
24	REGCTRL	P	**Turn-on control for the external BJT low-dropout (LDO) regulator.**
25	REGIN	P	**Internal regulator input.** Connect an external 3.3µF bypass capacitor from REGIN to AGND.
41	SBYDSG	O	**Discharge bypass P-channel MOSFET driver.**
29	WDT	I/O	**Watchdog timer pin.**
28	xALERT	O	**Interrupt alert output.**
16	SRN	I	**Negative sense pin.**
15	SRP	I	**Positive sense pin.**
42	CP	P	**Charge pump regulated voltage.** Connect a 47nF capacitor from CP to MID, then adjust the value based on the number of parallel DSG and CHG MOSFETs.
27	VDD	P	**1.8V rail for internal use.** Connect a 1µF bypass capacitor from VDD to AGND.
43	MID	P	**Protection MOSFET middle point.**

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
22	VREF	P	**ADC reference voltage.**
34	GPIO3/nCS	I/O	**Multi-function pin.** This pin can be set as GPIO3, or it can be set for SPI cable selection.
31	SCL/SCK	I	**Multi-function pin.** This pin can be set as the I^2C interface clock or the SPI interface clock.
32	SDA/SDI	I/O	**Multi-function pin.** This pin can be set as the I^2C interface data or the SPI serial data input.
33	SDO	O	**SPI serial data output.**

ABSOLUTE MAXIMUM RATINGS (1)

CHG, DSG, CP to AGND .....-0.3V to +90V
SBYDSG to AGND .....-0.3V to +75V
GPIOHV1 to AGND .....-0.3V to +75V
GPIOHV1 to TOP 0.3V
TOP to AGND .....-0.3V to +75V
PACKP to AGND .....-0.5V to +75V
MID to AGND .....-0.3V to +75V
Cx - C (x - 1) (x: 1 to 10) .....-0.3V to +10V
Cx to AGND (x: 1 to 10) ..... - 0.3V to *x* x 7V
C0 to AGND .....-0.5V to +5.7V
SRP, SRN to AGND .....-0.5V to +6V
VDD to AGND .....-0.5V to +2V
CP to MID .....-0.3V to +20V
REGCTRL to AGND .....-0.3V to +15V
NSHDN to AGND .....-0.3V to +9V
All other pins to AGND .....-0.3V to +6V
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... - 65°C to +150°C

ESD Ratings

Human body model (HBM) (2) 500V
Charged-device model (CDM) (3) 500V

Recommended Operating Conditions (4)

TOP voltage .....10V to 47V
Cx - C (x - 1) (x: 1 to 10) (5) .....1V to 5V
C0 to AGND ..... -0.25V to +0.3V
Operating temperature (T_J) ..... -40°C to +85°C
SRP to SRN .....-100mV to +100mV

Thermal Resistance (6)

Junction-to-ambient ($R_{\theta JA}$) ..... 46.6°C/W
Junction-to-case (top) ($R_{\theta JC(TOP)}$)..... 14.5°C/W
Junction-to-board (top) ($R_{\theta JB(TOP)}$) ..... 27.1°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Tested per ANSI/ESDA/JEDEC JS-001.
3) Tested per ANSI/ESDA/JEDEC JS-002.
4) The device is not guaranteed to function outside of its operating conditions.
5) The stack voltage should exceed 10V.
6) Metrics provided using set-up conditions compliant with EIA/JESD51-2, 7, and 8.

ELECTRICAL CHARACTERISTICS

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
Supply Current and Leakage						
Total shutdown current	I_{TOT_SHDN}	TOP + REGIN current, NSHDN pin low, 3.3V off, T_A = 25°C		1		µA
		TOP + REGIN current, NSHDN pin low, 3.3V off, T_A = -40°C to +85°C			2.5	µA
		TOP + REGIN current, 3.3V on, NSHDN pin low, T_A = 25°C		13.5		µA
		TOP + REGIN current, 3.3V on, NSHDN pin low, T_A = -40°C to +85°C			20	µA
Total safe state current	I_{TOT_SAFE}	TOP + REGIN current, communication interface enabled, safe state (all MOSFETs off), hardware monitoring off, plug-in detection disabled, T_A = 25°C		23		µA
		TOP + REGIN current, communication interface enabled, safe state (all MOSFETs off), hardware monitoring off, plug-in detection disabled, T_A = -40°C to +85°C			30	µA
Cell leakage	I_{Cx_LEAK}	T_A = 25°C	-200		+200	nA
		T_A = -40°C to +85°C	-600		+600	nA
Supported Series Cells						
Supported cell number (7)	N_{CELL}		4		10	
TOP supply voltage range	V_{TOP_SUPPLY}	T_A = -40°C to +85°C	10		47	V
TOP under-voltage lockout (UVLO) threshold	V_{TOP_UVLO}	Rising edge, T_A = -40°C to +85°C	8.2	9.15	10.1	V
		Falling edge, T_A = -40°C to +85°C	7.5	8.5	9.2	
TOP under-voltage (UV) hysteresis	$V_{TOP\_UVLO\_HYST}$	T_A = 25°C		1		V
Current Sense						
Current analog-to-digital converter (ADC) conversion time	t_{IADC}	16 bits (15 bits + sign)		2		ms
Current ADC measurement range	V_{SRPN}	T_A = -40°C to +85°C	-100		+100	mV
Current ADC measurement gain error	$I_{ADC\_GAIN\_ERR}$	16-bit conversion, FSR = 100mV, SRP-N common mode: +300mV to -125mV from GND, T_A = 25°C	-0.5		+0.5	%
		16-bit conversion, FSR = 100mV, SRP-N common mode: +300mV to -125mV from GND, T_A = -40°C to 85°C	-1		+1	%

Note:

7) Guaranteed by design.

ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
Current-sense offset (8)	$V_{IADC\_ACC\_OFFSET}$	SRP - SRN = 0V, SRP-N common mode: +300mV to -125mV from GND, T_A = -40°C to +85°C	-12		+12	µV
SRP and SRN leakage	I_{SRPN_LEAK}	IADC not running, T_A = -40°C to +85°C	-500		+500	nA
SRP and SRN differential input current	I_{SRPN_DIFF}	IADC running, |SPR - SRN| = 100mV, absolute value, T_A = -40°C to +85°C		0.5		µA
		IADC running, |SPR - SRN| < 5mV, T_A = -40°C to +85°C		50		nA
Sigma Delta Voltage ADC						
Voltage ADC conversion time	t_{VADC}	15 bits, T_A = 25°C		2		ms
Cell Voltage Measurement						
Cell ADC measurement range	V_{CELL}	T_A = -40°C to +85°C	1		5	V
Total cell measurement error (9)	V_{CELL_ERR}	V_{CELL} = 1V to 4.5V, T_A = 25°C	-5		+5	mV
		V_{CELL} = 1V to 4.5V, T_A = -20°C to +65°C	-7.5		+7.5	mV
		V_{CELL} = 1V to 4.5V, T_A = -40°C to +85°C	-12.5		+12.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-15		+15	mV
C0 to AGND voltage	$V_{C0\_TO\_AGND}$	C0 to AGND voltage drop resulting in less than 15mV error on cell 1, T_A = -40°C to +85°C	-0.25			V
Cell ADC input current	$I_{IN\_CELL\_CONV}$	Input current during ADC conversion when V_{CELL} = 5V, T_A = 25°C, cell 1 is measured by the C1 to C0 voltage		1.2		µA
Die Temperature						
Die temperature operating range	T_{DIE}		-40		+85	°C
Over-temperature (OT) analog shutdown threshold	T_{DIE_OTSD}			140	155	°C
Negative Temperature Coefficient (NTC) Temperature Measurement						
NTC voltage measurement range	V_{NTC}	Nominal NTC range within a percentage of NTCB, T_A = 25°C	0		100	%
NTC total measurement error	V_{NTC_ERR}	15-bit conversion, NTCB = 3.3V, T_A = -40°C to +85°C	-55		+55	LSB

Note:

8) The current measurement offset error is specified after completion of post-PCB assembly calibration. Contact an MPS FAE for the related application note.

9) No calibration required. The error can be further reduced by post-PCB assembly calibration. Contact an MPS FAE for the related application note.

ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
NTCx input leakage	$I_{NTC\_IN\_LEAK}$	ADC off, on each NTC pin, T_A = -40°C to +85°C			250	nA
NTCx input leakage ADC on	$I_{NTC\_LEAK\_CONV}$	ADC converting NTCx, on each NTC pin, T_A = 25°C			250	nA
TOP Measurement						
TOP measurement range	V_{TOP}	T_A = -40°C to +85°C	10		47	V
TOP total measurement error	V_{TOP_ERR}	15-bit conversion (positive range), T_A = -40°C to +85°C	-250		+250	mV
PACKP Measurement						
Pack measurement range	V_{PACKP}	T_A = -40°C to +85°C	2.5		47	V
Pack total measurement error	V_{PACKP_ERR}	15-bit conversion (positive range), T_A = -40°C to +85°C	-250		+250	mV
GPIO Measurement						
GPIO measurement range	V_{GPIO}	T_A = 25°C	0		3.3	V
GPIO total measurement error	V_{GPIO_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
GPIO input current during ADC reading	$I_{GPIO\_CONV\_IN}$	GPIO pins input current during ADC conversion, T_A = -40°C to +85°C		1		µA
Regulators Measurements						
REGIN measurement error	V_{REGIN_ERR}	ADC reading, T_A = 25°C	-15		+15	mV
		ADC reading, T_A = -40°C to +85°C	-25		+25	mV
3V3 total measurement error	V_{3V3_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
VDD total measurement error	V_{VDD_ERR}	15-bit ADC reading, T_A = 25°C	-15		+15	mV
		15-bit ADC reading, T_A = -40°C to +85°C	-25		+25	mV
Hardware Protection						
Cell over-voltage (OV) and UV steps (7)	$V_{CELL\_TH\_STEP}$			19.5		mV
Cell OV/UV threshold accuracy	$V_{CELL\_TH\_ACC}$	V_{CELL} = 2V to 4.5V, T_A = 0°C to 60°C	-19.5		+19.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-40		+40	mV
Pack OV/UV steps (7)	$V_{PACK\_TH\_STEP}$			19.5		mV
Pack OV/UV threshold accuracy	V_{PACKTH_ACC}	T_A = -40°C to +85°C	-312.5		+312.5	mV
Deep discharge steps (7)	V_{DEEPTH_STEP}			19.5		mV

Note:

7) Guaranteed by design

ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
Deep discharge threshold accuracy	V_{DEEPTH_ACC}	V_{CELL} = 2V to 4.5V, T_A = 0°C to 60°C	-19.5		+19.5	mV
		V_{CELL} = 1V to 5V, T_A = -40°C to +85°C	-40		+40	mV
Short-circuit (SC) fastest detection time	$t_{SC\_DGL\_MIN}$	Fastest deglitch setting and latency, T_A = -40°C to +85°C			120	µs
Over-current (OC1) discharge FSR value	$V_{OC1\_DSG\_FSR\_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		80		mV
OC1 discharge full scale accuracy	$V_{OC1\_DSG\_FSR\_1X\_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC1 discharge offset	$V_{OC1\_DSG\_FSR\_1X\_OFF}$	Range and LSB selector = 0 (1x), offset on LSB, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC1 discharge FSR value	$V_{OC1\_DSG\_FSR\_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		240		mV
OC1 discharge full scale accuracy	$V_{OC1\_DSG\_FSR\_3X\_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC1 discharge offset	$V_{OC1\_DSG\_FSR\_3X\_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC2 discharge FSR value	$V_{OC2\_DSG\_FSR\_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		80		mV
OC2 discharge full scale accuracy	$V_{OC2\_DSG\_FSR\_1X\_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC2 discharge offset	$V_{OC2\_DSG\_FSR\_1X\_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC2 discharge FSR value	$V_{OC2\_DSG\_FSR\_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		240		mV
OC2 discharge full scale accuracy	$V_{OC2\_DSG\_FSR\_3X\_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC2 discharge offset	$V_{OC2\_DSG\_FSR\_3X\_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC charge FSR value	$V_{OC\_CHG\_FSR\_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		51.2		mV

ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
OC charge full scale accuracy	$V_{OC\_CHG\_FSR\_1X\_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC charge offset	$V_{OC\_CHG\_FSR\_1X\_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
OC charge FSR value	$V_{OC\_CHG\_FSR\_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		153		mV
OC charge full scale accuracy	$V_{OC\_CHG\_FSR\_3X\_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
OC charge offset	$V_{OC\_CHG\_FSR\_3X\_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
SC discharge FSR value	$V_{SC\_DSG\_FSR\_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		176		mV
SC discharge full scale accuracy	$V_{SC\_DSG\_FSR\_1X\_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
SC discharge offset	$V_{SC\_DSG\_FSR\_1X\_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
SC discharge FSR value	$V_{SC\_DSG\_FSR\_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		528		mV
SC discharge full scale accuracy	$V_{SC\_DSG\_FSR\_3X\_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
SC discharge offset	$V_{SC\_DSG\_FSR\_3X\_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-2		+2	mV
SC charge FSR value	$V_{SC\_CHG\_FSR\_1X}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = 25°C		80		mV
SC charge full scale accuracy	$V_{SC\_CHG\_FSR\_1X\_ACC}$	Range and LSB selector = 0 (1x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%
SC charge offset	$V_{SC\_CHG\_FSR\_1X\_OFF}$	Range and LSB selector = 0 (1x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
SC charge FSR value	$V_{SC\_CHG\_FSR\_3X}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = 25°C		240		mV
SC charge full scale accuracy	$V_{SC\_CHG\_FSR\_3X\_ACC}$	Range and LSB selector = 1 (3x), FSR (max setting), T_A = -40°C to +85°C	-15		+15	%

ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
SC charge offset	$V_{SC\_CHG\_FSR\_3X\_OFF}$	Range and LSB selector = 1 (3x), offset on smallest setting, T_A = -40°C to +85°C	-1.5		+1.5	mV
Cell-Balancing						
$R_{DS(ON)}$ balancing MOSFET	$R_{DS(ON)\_BAL\_FET}$	T_A = 25°C		28		Ω
		T_A = -40°C to +85°C	15		50	Ω
Open Wire						
Open-wire pull-up current	I_{OW_PUP}	T_A = 25°C		100		µA
Open-wire pull-down current	I_{OW_PD}	T_A = 25°C		100		µA
Low-Dropout Regulator (LDO) Supply and References						
REGCTRL output voltage	$V_{REGCTRL}$	With external REGIN BJT, V_{TOP} = 10V to 47V, with REGCTRL load current = 0mA and 1mA, T_A = -40°C to +85°C	5.45	5.6	5.75	V
REGIN output voltage (10)	V_{REGIN}	With external REGIN BJT, V_{TOP} = 10V to 47V, with load current = 1mA and 50mA, T_A = -40°C to +85°C	4.65	5.1	5.4	V
REGIN analog UV	V_{REGIN_UV}	With external REGIN BJT, falling edge, V_{TOP} = 10V to 47V, T_A = -40°C to +85°C	4.16	4.3	4.44	V
3V3 nominal voltage	V_{3V3}	T_A = 25°C		3.3		V
3V3 output accuracy	V_{3V3_ACC}	T_A = -40°C to +85°C	-5		+5	%
3V3 short-circuit current	I_{3V3_EFET}	With external REGIN BJT, T_A = -40°C to +85°C	55	68	80	mA
VDD output voltage	V_{DD}	T_A = 25°C		1.8		V
Reference voltage	V_{REF}	T_A = 25°C		3.3		V
NTCB pull-up voltage	V_{NTCB}	NTCB enabled, no load, T_A = 25°C		3.3		V
NTCB load	$I_{NTCB\_MAXLOAD}$	NTCB enabled, max load, T_A = 25°C		4		mA
		NTCB enabled, max load, T_A = -40°C to +85°C	3.2		4.8	mA
3V3 analog UV	V_{3V3_UV}	Falling edge		2.85		V
General-Purpose Input/Output (GPIO)						
GPIO input voltage (high)	V_{IH_GPIO}	Voltage high (V_H) = 3.3V or 5V, T_A = -40°C to +85°C	0.8 x V_H		V_H	V
GPIO input voltage (low)	V_{IL_GPIO}	V_H = 3.3V or 5V, T_A = -40°C to +85°C	0		0.2 x V_H	V
GPIO output voltage (high)	V_{OH_GPIO}	V_H = 3.3V or 5V, I_{SOURCE} = 1.5mA, T_A = -40°C to +85°C	V_H - 0.5		V_H	V

Note:

10) Guaranteed by design. The REGIN voltage is limited by the $V_{REGCTRL}$ and is equal to $V_{REGCTRL}$ - V_{BE_ON}.

ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
GPIO output voltage (low)	V_{OL_GPIO}	V_H= 3.3V or 5V, I_{SINK} = 1.5mA, T_A = -40°C to +85°C	0		0.4	V
GPIO push-pull resistor (up)	R_{GPIO_PUP}	GPIO high voltage = 3.3V, external BJT as REGIN regulator		430		Ω
GPIO push-pull resistor (down)	R_{GPIO_PDOWN}	GPIO low voltage = 0V		110	200	Ω
GPIO pull-up mode	$R_{GPIO\_WEAK\_PUP}$			17		kΩ
GPIO HV						
GPIO HV input voltage high level	V_{IH_GPIOHV}	T_A = -40°C to +85°C	2.4			V
GPIO HV input voltage low level	V_{IL_GPIOHV}	T_A = -40°C to +85°C			0.7	V
GPIOHV max pull-up current	I_{GPIOHV_PUP}			11		mA
GPIOHV max pull-down current	I_{GPIOHV_PDOWN}			8		mA
NSHDN Pin						
NSHDN internal pull down	R_{SHDN_PD}	NSHDN 0V to 5V		5		MΩ
NSHDN configuring voltage	V_{NSHDN_PROG}		7.5	7.6	7.7	V
NSHDN deglitch to enter shutdown	$t_{NSHDN\_DGL\_ENTER}$	T_A = 25°C, IC stays in safe mode for longer than $t_{NSHDN\_DGL\_ACTIVE}$		8		ms
NSHDN deglitch active time	$t_{NSHDN\_DGL\_ACTIVE}$	T_A = 25°C		4		ms
NSHDN falling threshold	V_{NSHDN_FALL}			1		V
NSHDN rising threshold	V_{NSHDN_RISE}	3V3 enabled at shutdown mode		2.65		V
		3V3 disabled at shutdown mode		2		V
WDT Pin						
Reset pulse length	$t_{WDT\_RSTPULSE\_LEN}$			10		ms
High-Side MOSFET (HS-FET) Drive						
CHG gate drive voltage	V_{CHG}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 47V, V_{GS} = 10V, T_A = 25°C		10		V
CHG gate drive voltage accuracy	V_{CHG_ACC}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 47V, 10V selected, T_A = -40°C to +85°C	9.3		10.7	V
CHG gate drive turn-on resistance	R_{CHG_ON}	FET drive turned on, PACKP = V_{TOP}, T_A = 25°C		2600		Ω

ELECTRICAL CHARACTERISTICS *(continued)*

Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
CHG gate driver turn-off resistance	R_{CHG_OFF}	MOSFET driver turned off, PACKP = V_{TOP}, T_A = 25°C		840		Ω
DSG gate drive voltage	V_{DSG}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 47V, V_{GS} = 10V, T_A = 25°C		10		V
DSG gate driver voltage accuracy	V_{DSG_ACC}	C_{LOAD} = 80nF, static value at transition completed, V_{TOP} = 18V to 47V, 10V selected, T_A = -40°C to +85°C	9.3		10.7	V
DSG gate driver turn-on resistance	R_{DSG_ON}	FET driver turned on, PACKP = V_{TOP}, T_A = 25°C		2600		Ω
DSG gate driver turn-off resistance	R_{DSG_OFF}	MOSFET driver turned off, PACKP = V_{TOP}, DSG = PACKP + 5V, T_A = 25°C		600		Ω
SBYDSG gate driver voltage	V_{SBYDSG}	C_{LOAD} = 10nF, static value at transition completed, V_{TOP} = 18V to 47V, V_{GS} = -10V, T_A = -40°C to +85°C	-12	-10	-9	V
SBYDSG gate driver on resistance	R_{SBYDSG_ON}	FET driver turned on, T_A = -40°C to +85°C		14.3		kΩ
SBYDSG gate driver off resistance	R_{SBYDSG_OFF}	FET driver turned off, T_A = -40°C to +85°C		2.7		kΩ
Charge Pump						
Charge pump output voltage	V_{CP}	Gate driver voltage = 10V, regular normal control mode, T_A = 25°C		14.7		V
		Gate driver voltage = 6V, regular lower control mode, T_A = 25°C		8.35		V
Charge pump output voltage accuracy	V_{CP_ACC}	Accuracy of select V_{CP} average value, T_A = -40°C to +85°C	-1		+1	V
Charge pump turn-on time	t_{CP_TON}	CP transition from V_{TOP} to V_{TOP} + V_{CP}, 10nF capacitor on CP, V_{TOP} = 21V, for both low-power mode and regular control mode, T_A = -40 to +85°C			2	ms
Pull-Up Comparators						
PACKP charge	I_{PACKP_PUP}	V_{TOP} = 10V to 47V, T_A = 25°C		250		µA
PACKP discharge	I_{PACKP_PDOWN}	V_{TOP} = 10V to 47V, T_A = 25°C		250		µA
PACKP exceeds V_{TOP}	$V_{PACKP\_HGR\_VTOP}$	V_{TOP} = 10V to 47V, T_A = 25°C		280		mV
PACKP is below V_{TOP}	$V_{PACKP\_LWR\_VTOP}$	V_{TOP} = 10V to 47V, T_A = 25°C		-1.77		V
Standby comparator accuracy	$V_{SBY\_COMP\_ACCU}$	Offset on smallest setting, T_A = 25°C	-125		+125	µV
PACKP short recovery threshold	$V_{PACKP\_SCOC\_REC\_TH}$	T_A = 25°C		110		mV
Short recovery current-source accuracy	I_{SCOC_PUP}	Offset on smallest setting, T_A = 25°C	-50		+50	µA

ELECTRICAL CHARACTERISTICS *(continued)*

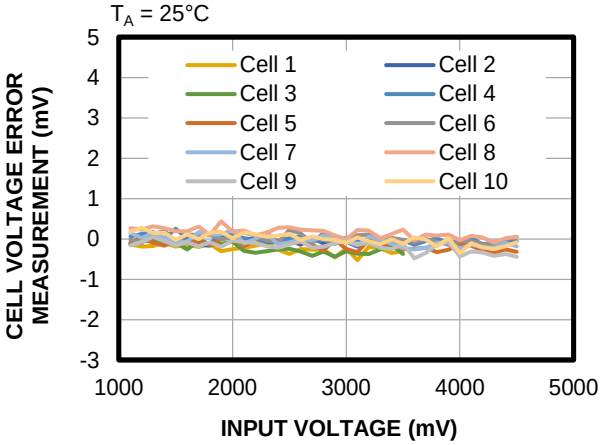
Connected cells = 10, each cell voltage = 3.75V, V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

Parameter Name	Symbol	Condition	Min	Typ	Max	Units
Internal Clock						
Internal clock frequency	f_{2M_CLOCK}	V_{TOP} = 10V to 47V, T_A = 25°C		2		MHz
Internal clock frequency	f_{2M_CLOCK}	V_{TOP} = 10V to 47V, T_A = -40°C to +85°C	1.85	2	2.15	MHz
Low-frequency internal clock	f_{32K_CLOCK}	V_{TOP} = 10V to 47V, T_A = 25°C	31.2	32	32.8	kHz
Low-frequency internal clock	f_{32K_CLOCK}	V_{TOP} = 10V to 47V, T_A = -40°C to +85°C	30.7		33.3	kHz
I^2C Communication Interface						
I^2C clock frequency	f_{I2C}	T_A = 25°C			400	kHz
SCL, SDA input voltage low	V_{ILOW}	T_A = -40°C to +85°C			0.25 x 3V3	V
SCL, SDA input voltage high	V_{IHIGH}	T_A = -40°C to +85°C	0.7 x 3V3			V
SCL, SDA input hysteresis	V_{IHYST}	T_A = -40°C to +85°C		0.2 x 3V3		V
Serial Peripheral Interface (SPI) Communication Interface						
SPI clock frequency	f_{SPI}	T_A = 25°C			1.0	MHz
SPI input low	$V_{SPI\_IN\_LOW}$	SDI, CLK, T_A = -40°C to +85°C			0.25 x 3V3	V
SPI input high	$V_{SPI\_IN\_HIGH}$	SDI, CLK, T_A = -40°C to +85°C	0.7 x 3V3			V
SDO high-side (HS) on resistance	$R_{SDO\_DRV\_HI}$	I_{SOURCE} = 1.5mA, T_A = -40°C to +85°C		100		Ω
SDO low-side (LS) on resistance	$R_{SDO\_DRV\_LOW}$	I_{SINK} = 1.5mA, T_A = -40°C to +85°C		52		Ω

TYPICAL PERFORMANCE CHARACTERISTICS

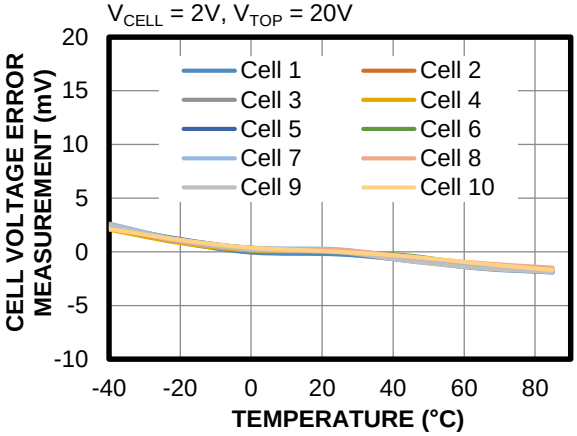
Cell Voltage Error Measurement vs. Input Voltage

T_A = 25°C



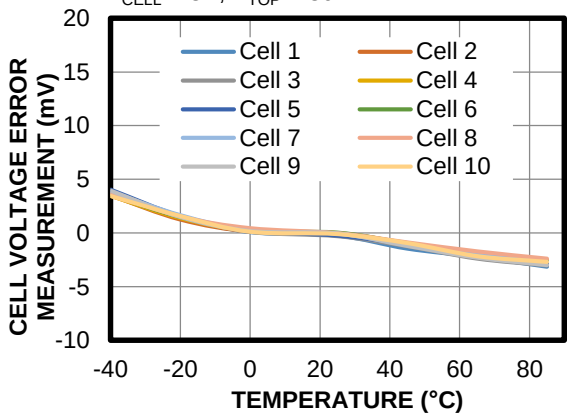
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 2V, V_{TOP} = 20V



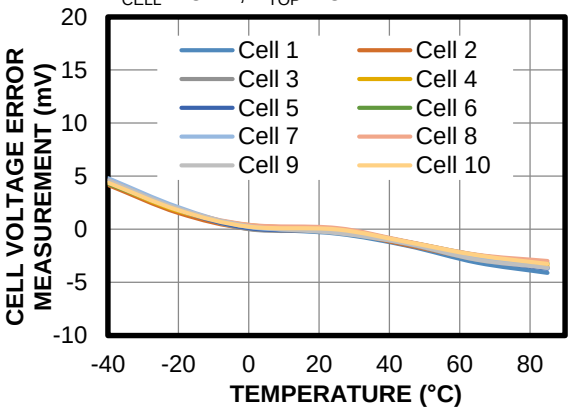
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 3V, V_{TOP} = 30V



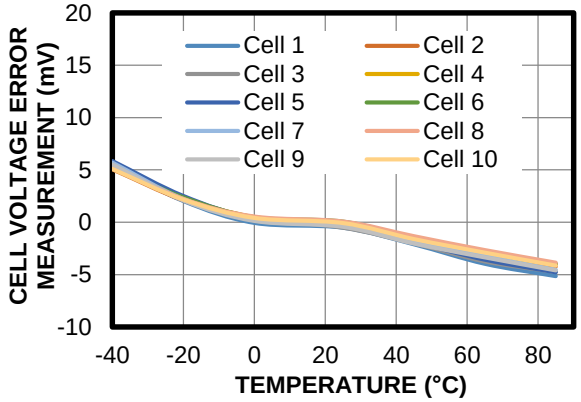
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 3.7V, V_{TOP} = 37V



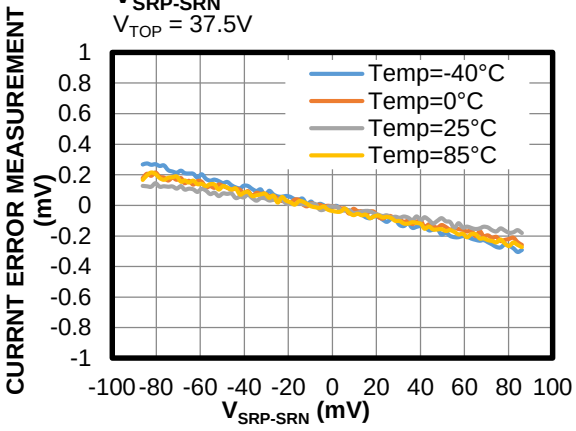
Cell Voltage Error Measurement vs. Temperature

V_{CELL} = 4.5V, V_{TOP} = 45V



Current Error Measurement vs. $V_{SRP-SRN}$

V_{TOP} = 37.5V

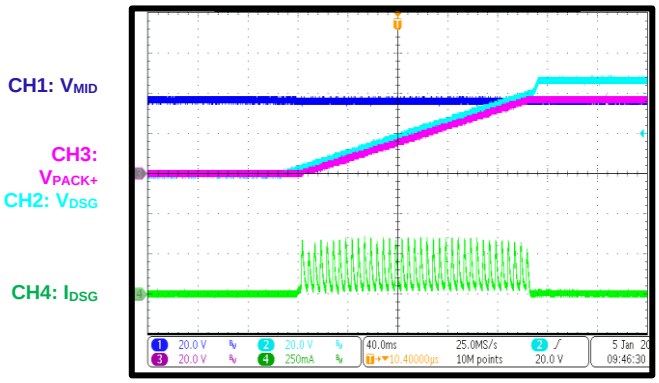


TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves and waveforms are tested on the evaluation board. V_{TOP} = 37.5V, T_A = 25°C, unless otherwise noted.

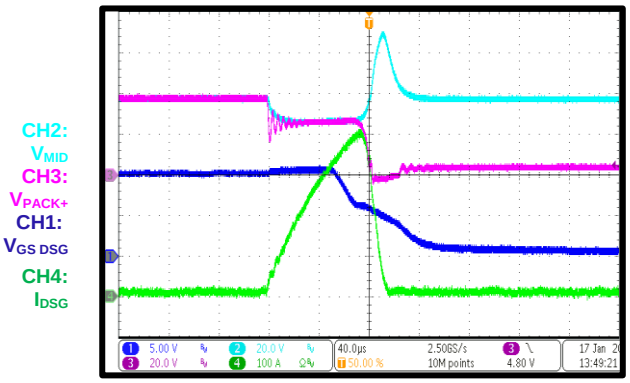
DSG Soft Start

PACK+ is connected to a 1mF capacitor, the DSG slope is 0.2V/ms



DSG Fast-Off in Short-Circuit

$R_{SRP-SRN}$ = 1mΩ, short-circuit threshold is 55mV, deglitch off, 4 paralleled CRSS042N10N devices act as the DSG N-channel MOSFETs, which has a typical C_{ISS} of 6772pF



TYPICAL PERFORMANCE WHEN PAIRED WITH MPF4279X FUEL GAUGE

The MP2790 battery monitor includes strictly synchronized cell and pack voltage and current measurements, for the purpose of maximizing state-of-charge (SOC) determination. MPS's MPF4279x family of fuel gauges are designed to take advantage of this feature. This section illustrates the SOC accuracy of the MP2790 battery monitor when combined with MPS's MPF4279x fuel gauge family.

Constant-Current/Constant-Voltage (CC/CV) Charge and Dynamic Discharge Cycle

The next scenarios consist of charging a 10S1P (11) battery using the typical CC/CV method, followed by a highly dynamic discharge at different ambient temperatures. The charge constant current rate is 1C, while the charge termination current in this example is 0.1C. The highly dynamic discharge corresponds to a typical e-bike's current profile, with an average current of 1C and maximum peak currents up to 2.8C. Figure 3 shows the current profile of the complete cycle at 25°C.

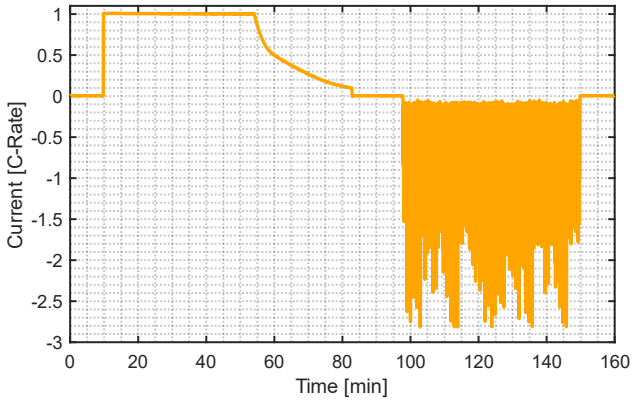


Figure 3: CC/CV Charge and Dynamic Discharge Current Profile

Figure 4 shows the performance of the combined MP2790 and MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 25°C. During charge, the root-mean-squared (RMS) (12) and maximum pack SOC error are 0.61% and 1.03%, respectively. During discharge, the root-mean-squared and pack SOC error are 0.78% and 1.94%, respectively.

Notes:

11) 10S1P refers to the battery configuration. There are 10 groups of 1 parallel cell connected in series.

12) The RMS error is equal to $\sqrt{\frac{\sum_{n=1}^{N}(\theta_n-\hat{\theta}_n)^2}{N}}$, where θ is the actual SOC, $\hat{\theta}$ is the estimated SOC, and *N* is the number of samples.

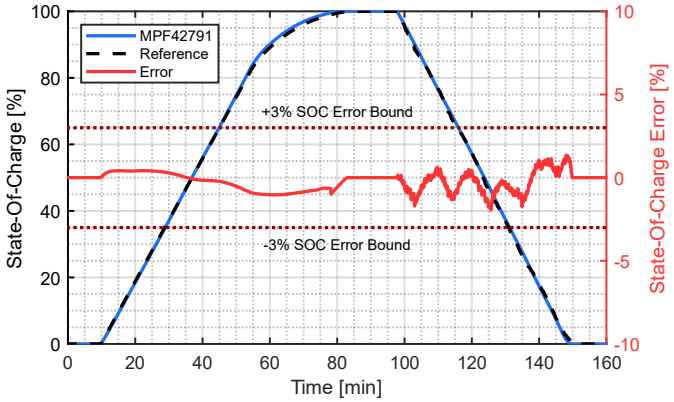


Figure 4: Combined MP2790 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 25°C)

Figure 5 shows the performance of the combined MP2790 + MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 0°C. During charge, the root-mean-squared and maximum pack SOC error are 0.68% and 1.22%, respectively. During discharge, the root-mean-squared and pack SOC error are 1.15% and 2.97%, respectively.

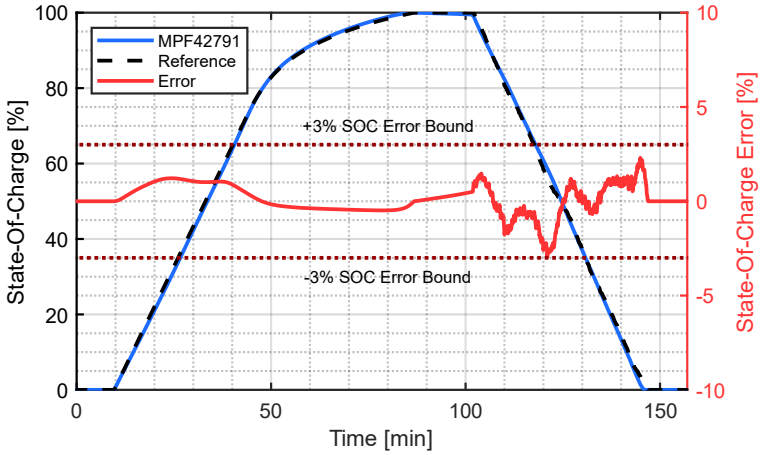


Figure 5: Combined MP2790 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 0°C)

Figure 6 shows the performance of the combined MP2790 + MPF42791 for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 40°C. During charge, the root-mean-squared and maximum pack SOC error are 0.40% and 0.60%, respectively. During discharge, the root-mean-squared and pack SOC error are 0.77% and 1.89%, respectively.

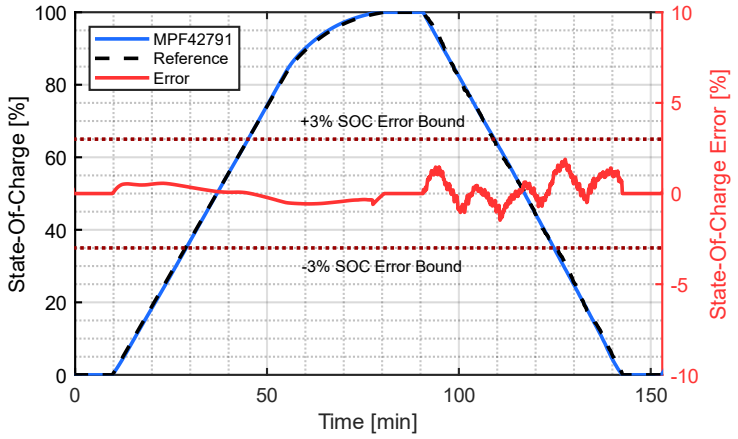


Figure 6: Combined MP2790 + MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 40°C)

Performance Summary

This section provides a summary of the combined MP2790 + MPF42791 real-world performance. Table 1 shows a summary of the pack SOC performance metrics for a 10S1P battery.

Table 1: MPF42791 SOC Root-Mean-Squared (and Maximum) Error

Test Case	0°C	25°C	40°C
CC/CV charge	0.68% (1.22%)	0.61% (1.03%)	0.40% (0.60%)
Dynamic discharge	1.15% (2.97%)	0.78% (1.94%)	0.77% (1.89%)

FUNCTIONAL BLOCK DIAGRAM

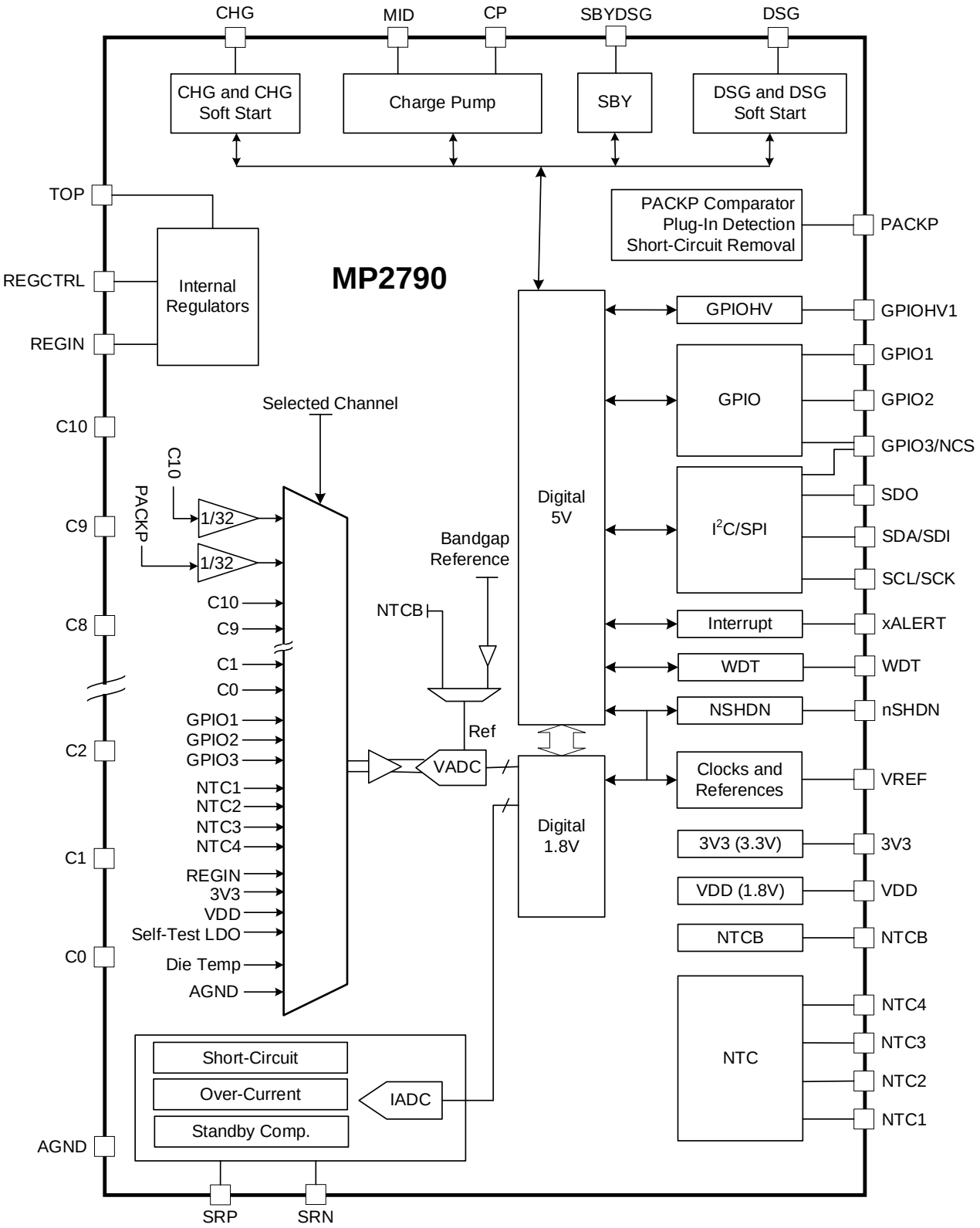


Figure 7: Functional Block Diagram

OPERATION

The MP2790 is a high-accuracy monitor and protector with an integrated high-side MOSFET (HS-FET). It supports 4-cell to 10-cell in series.

The host controller can obtain each cells' voltage, current, and temperature via the I²C or serial peripheral interface (SPI) commands. Based on this information, the host controls the HS-FET's on-/off-state to protect the cells, calculate the pack state-of-charge (SOC), and balance the mismatched cell(s).

The MP2790 can be enabled for protection functions, which can automatically monitor the cells' voltage, current, and temperature. If any value exceeds the configured threshold, the MP2790 automatically turns off the charge (CHG) or the discharge (DSG) MOSFET depending on the fault condition. Refer to the Fault section starting on page 35 for more information.

Regulators and Power Domains

There are three main power rails:

- REGIN (5V): supplies power to the AFE analog circuitry
- 3V3 (3.3V): powers an external microcontroller (MCU)
- VDD (1.8V): internal use only; powers the digital domain

The 3.3V rail can be configured to be on or off in shutdown mode.

Registers (Default and Lock)

Most of the configuration settings and options have a configurable default value. Certain registers can be configured independently by an external MCU, and they can be locked in read-only mode. This prevents critical safety features from being changed.

Non-Volatile Memory (NVM) Configuration

The default values of most registers can be configured through the non-volatile memory (NVM). Some registers are one-time programmable (OTP), while others are multiple-time programmable (MTP). The MTP registers can be configured up to three times. These values can be locked, so that the same version of the IC can be adjusted for similar projects with minor differences.

To configure the MTP, apply 7.5V to the NSHDN pin and follow the steps below:

1. Ensure that the NSHDN pin is set to 7.5V.
2. Write the appropriate value to the register that allows MTP.
3. Write prior to the store command with the following command access code: 0xA5B6 (B9h = 0xA5B6).
4. Send the command to store the register's current value to the NVM by writing 1 to STORE_NVM_CMD (B8h, bit[3]).
5. Wait for STORE_IN_PROGRESS to go back to 0.
6. Recover the NSHDN pin to 3.3V.

Main Modes

The MP2790's main operation modes are listed and described below (see Figure 8 on page 23).

Shutdown Mode

It is vital to preserve a battery's capacity. Shutdown mode minimizes the amount of leakage from the battery pack, which extends the battery pack's shelf storage life.

In shutdown mode, the communication interface is unavailable and REGIN is loosely regulated, which means its voltage is below the normal voltage without any load capacity. However, it is possible to keep the 3.3V rail active in shutdown mode with a slight margin for current consumption (when the 3.3V rail is active, REGIN is regulated normally).

If any of the following situations occur, the device enters the shutdown mode.

- NSHDN pin is low.
- V_{TOP} is below V_{TOP_UVLO}.
- The die temperature exceeds TDIE_OTSD.

Safe Mode

To enter safe mode from shutdown mode, pull up the NSHDN pin and wait at least 5ms before issuing an I²C or SPI command.

If any functional commands are required in safe mode (e.g. high-resolution voltage scanning, Coulomb counting, MOSFETs turn on, voltage protection monitoring, open wire, cell-balancing), then the I²C or SPI bus must be idle for at least 200µs after the functional command is enabled.

Safe mode is characterized by the following conditions:

- The protection MOSFETs are turned off.
- The over-voltage (OV) and under-voltage (UV) hardware autonomous protection state machine is disabled, unless it is forcibly enabled.
- The communication interface is enabled.

To leave safe mode, see the High-Side MOSFET Control section on page 17.

In safe mode, the analog front-end (AFE) provides a P-channel MOSFET bypass function, which is controlled by GPIOHV1.

In safe mode, it is possible to enable hardware protection monitoring (cell OV, cell UV, high/low temperature, and current monitoring).

Normal Mode

Normal mode is divided into three states: A, B and C. When only one driver is turned on from safe mode, the chip enters the normal A state first; if the other driver is also enabled, the chip enters the normal B state.

If only one FET driver is off due to a fault, the state is maintained. If both FETs are off due to a fault, the chip enters a normal C state (see Figure 8).

In normal mode, hardware protection monitoring is always enabled. The time between hardware protection monitoring intervals is set by NORM_MONITOR_CFG.

Standby Mode

Standby mode reduces current consumption by using a standby P-channel MOSFET to power the system (instead of DSG N-channel MOSFET), and conducts through the CHG N-channel MOSFET's body diode. To enter standby mode, standby mode must be enabled (refer to the STB_CFG (06h) section on page 49 for more information), the current must be below the standby current threshold, and the Coulomb counter is not enabled.

In standby mode, the time interval between hardware protection monitoring can be independently lengthened via the STBY_MONITOR_CFG register. This reduces average current consumption.

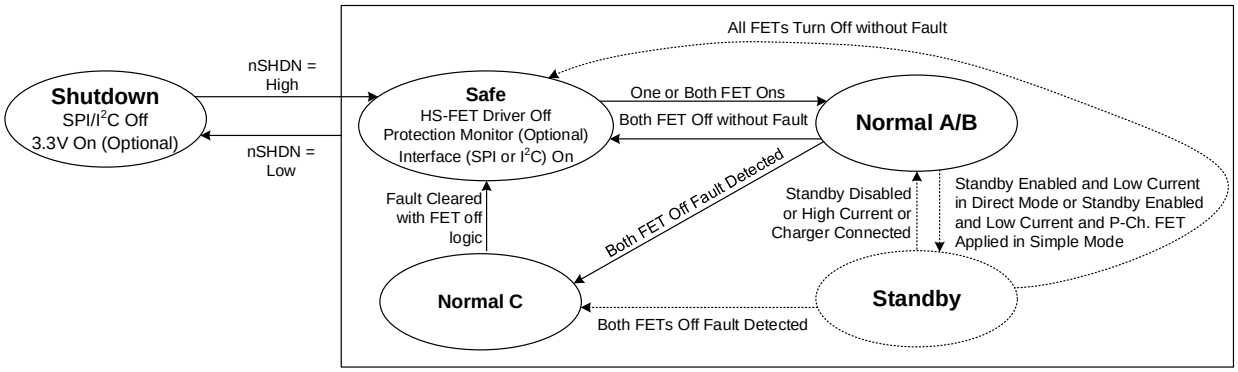


Figure 8: Main States Diagram

High-Resolution Voltage ADC Scan for the MCU

A voltage scan can convert the following classes of inputs:

- Die temperature voltage
- NTC1, NTC2, NTC3, and NTC4 voltages
- Cell voltages
- C10 to AGND voltage
- PACKP pin voltage
- GPIO voltages (GPIO1, GPIO2, and GPIO3)
- Regulators (VDD (1.8V), 3V3, and REGIN)

If a class of inputs is not enabled, the scan skips to the next class.

Control bits are provided to enable individual channels in each class (see HR_SCAN0 (9Ch), HR_SCAN1 (9Dh), and HR_SCAN2 (9Eh) starting on page 121 for more information). The device is notified when the scan is complete, and the results are available for reading.

Synchronized Voltage and Current Reading

For cell and pack voltages, the exact, synchronized current readings can be read in dedicated registers paired with the matching voltage reading. Synchronous current readings can be enabled using CELL_SYNC_EN and VTOP_SYNC_EN (see the HR_SCAN0 (9Ch) section on page 121 for more details).

The synchronized voltage and current reading can be requested concurrently with Coulomb counting monitoring. In this scenario, the voltage in the ADC settles, and the conversion time for each channel is longer than 2ms.

Cell-Balancing

The battery pack reaches its end of life (EOL) when the capacity of the weakest cell is too low to be usable. Unbalanced cells yield the same effect, with one cell at a higher SOC, and another at a lower SOC. To reduce the effects of this issue, it is critical to balance lithium cells.

Unbalanced cells can be caused by cell temperature differences, different self-discharge rates, and general production tolerances that can affect cell chemistry and alter the aging rates among strings of parallel cells. Cell-balancing can extend the usable life of the battery pack by keeping the voltage of each cell within the defined safe operating area (SOA).

Figure 9 shows the cell-balancing sequence for the cell-balancing list.

Internal MOSFET Balancing

The MP2790 supports direct cell balancing, without the use of external MOSFETs or BJTs, for currents up to about 58mA (with a 4V cell voltage). The balance current for each cell is dictated by the combined filter resistor and the on resistance ($R_{(DS)ON}$) of the internal balancing MOSFET. The MP2790 can simultaneously balance only even or odd cells. Internal logic handles the sequencing between even and odd cells.

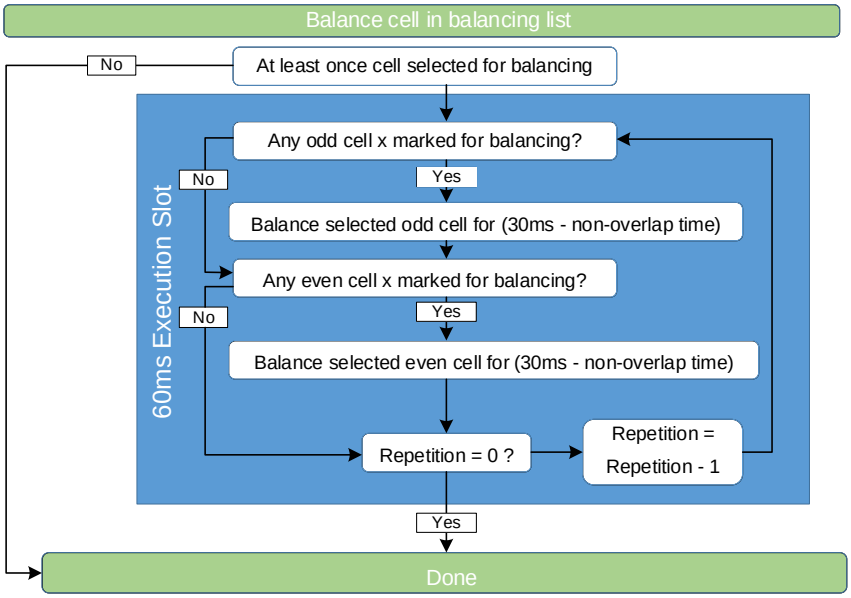


Figure 9: Executing Balancing for Cell in Balancing List

External Balancing

A balancing current exceeding 58mA can be achieved by adding external balancing MOSFETs or BJTs. This balancing current is limited by board thermals and the wiring resistance.

For external MOSFETs, it is also limited by the MOSFETs' $R_{(DS)ON}$ at the appropriate gate voltage (V_{GS}). For external BJTs, it may be limited by the h_{FE}.

For external MOSFETs, a minimum gate threshold voltage of 1.8V is required (assuming a 4.2V lithium cell) to turn on the balancing MOSFETs.

Manual Cell-Balancing

The cells that need to be balanced are manually marked by writing to the appropriate register (see the BAL_LIST (A5h) section on page 125).

The balancing time for marked cells can be configured via BAL_REPETITION, with 0 to 31 repetitions. When BAL_REPETITION is set to 0, there is only one 30ms execution (see the BAL_CFG (A7h) section on page 127).

The host MCU should periodically read the AFE die temperature to ensure it is within the operating range, as an excessive temperature can lead to OT shutdown.

Automatic Cell-Balancing

Automatic cell-balancing offers the following configurations:

1. Enable automatic cell balancing by setting BALANCE_MODE_REG = 1 (see the BAL_CFG (A7h) section on page 127).
2. Configure the method for initiating automatic cell-balancing via BALANCE_MODE_CTRL (see the BAL_CFG (A7h) section on page 127). The MP2790 can be configured to use BALANCE_GO control (see the BAL_CTRL (A6h) section on page 126) or GPIO3 control to initiate automatic cell-balancing.
3. Disable constant automatic balancing by setting AUTO_BAL_ALWAYS = 0 (see the BAL_CFG (A7h) section on page 127). BAL_REPETITION sets the number of cell-balancing iterations. The cell-balancing repetition number is ignored if AUTO_BAL_ALWAYS = 1, and the device constantly balances the cells until AUTO_BAL_ALWAYS is set to 0, or until the balancing list is empty.
4. Set the balancing threshold via BAL_MSM_TH (see the BAL_THR (A8h) section on page 127). This is the minimum voltage difference between the current cell voltage and the lowest cell voltage to be eligible for cell balancing. This value ranges between 19.5mV and 87.855mV, with 9.765mV steps.
5. Set the minimum balancing voltage via CELL_BAL_MIN (see the BAL_THR (A8h) section on page 127). This is the minimum cell voltage for a cell to be eligible for balancing. This value ranges between 2500mV and 4961mV, with 39mV steps.
6. Set ABAL_ON_CHARGE = 1 (see the BAL_THR (A8h) section on page 127) to enable automatic cell-balancing when the state of the current is in charge mode. Set ABAL_ON_STBY = 1 to enable automatic cell-balancing when the state of the current is in standby mode.

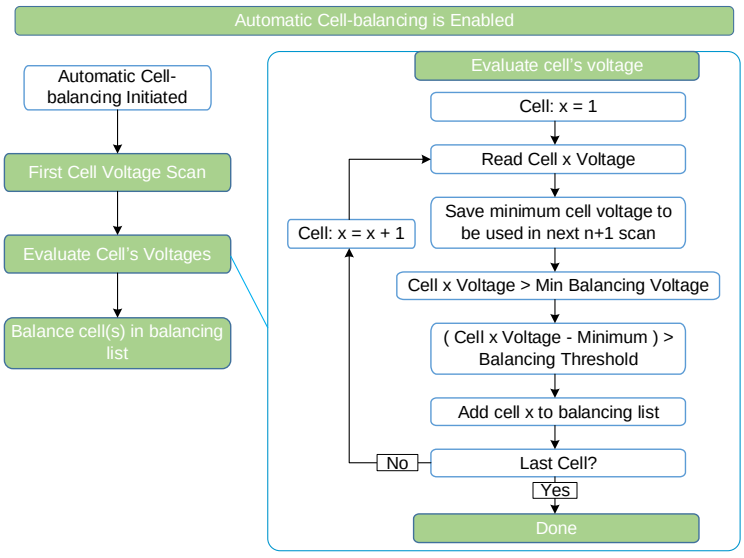


Figure 10: Automatic Cell-Balancing (Cell Voltage Evaluation)

If the state of the current is in discharge mode, automatic cell-balancing will be skipped.

The die temperature threshold can be used to prevent or suspend balancing. The MP2790 can be configured to suspend constant automatic cell-balancing (AUTO_BAL_ALWAYS = 1), when the die temperature threshold has been exceeded via STOP_ON_HOT (see the BAL_THR (A8h) section on page 127). Once the OT condition is removed, constant automatic cell-balancing resumes.

Figure 10 on page 25 shows the cell-balancing list update for automatic cell-balancing.

Open-Wire Detection

The open-wire state machine automatically controls the pull-up and pull-down current sources during open-wire detection, and it detects the voltage changes on each cell (see Figure 11). The cells that are detected can be set via CELL_S_CTRL (see the CELLS_CTRL (00h) section on page 46).

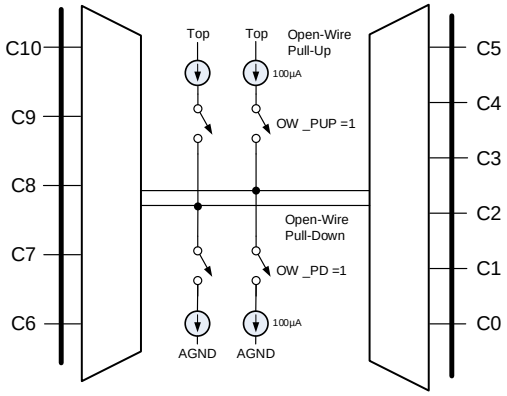


Figure 11: Open-Wire Detection Architecture

The open-wire detection current uses a pair of 100µA pull-up/-down currents. The interval can be configured to be between 1ms and 16ms, with a 1ms resolution. The default is 8ms (see the OPEN_CFG (57h) section on page 103).

The threshold that determines how much change can be accepted for an open circuit is a configurable voltage threshold ranging between 39.06mV and 625mV, with 39.06mV steps. The default is 195mV (see the OPEN_CFG (57h) section on page 103).

The host MCU can trigger open-wire detection with a dedicated command register (see the SFT_GO (55h) section on page 101). If multiple open wires are present simultaneously, then the detection logic reports at least one open wire, which tells the device to avoid using the overall battery pack (see Figure 11).

Coulomb Counter

The MP2790 can accumulate up to 2 seconds worth of the current ADC reading.

When the accumulation process is complete, the value is stored in CC_ACC_LSBS (lower 2 bytes) and CC_ACC_MSBS (upper 2 bytes) for MCU reading, and an interrupt is posted. The sequence below provides the typical steps to handle a Coulomb counting conversion:

1. Set CC_EN to enable starting the conversion in a normal B or normal C state.
2. Accumulation reaches the amount specified in CC_INT_CNT.
3. CC_ACC_LSBS and CC_ACC_MSBS are updated to the values reported in CC_RT_ACC_LSBS and CC_RT_ACC_MSBS.
4. When back-to-back Coulomb counting accumulation is disabled (see the CC_CFG (9Ah) section on page 119), the CC_DONE flag can be checked to verify that accumulation has been completed. Readings are available in CC_ACC_LSBS and CC_ACC_MSBS.
5. If back-to-back conversion is enabled, the CC_RT_ACC_xSBS registers are automatically cleared and Coulomb counting restarts. The integrated value for completed accumulation can be read from CC_ACC_xSBS. If CC_ACC_INT_EN is enabled, a Coulomb counting done interrupt is triggered when CC_ACC_xSBS updates.
6. If back-to-back Coulomb counting accumulation is disabled, CC_EN can be set to disable clearing CC_DONE. To stop Coulomb counting if back-to-back conversions are enabled, the back-to-back flag should be cleared first so that the ongoing conversion does not trigger a new conversion.
7. If Coulomb counting is required in safe mode, CC_EN_SAFE should be set to 1.

8. If an CC_ACC_INT_STS interrupt is detected, it should be cleared using the CC_ACC_STS_INT_CLEAR command.

Supported Concurrency

Table 2 shows which features can be enabled once another feature is active. When multiple features are enabled simultaneously, some remaining features can still be activated.

It is possible to use a high-resolution voltage scan during cell-balancing, but this requires considerations, as this affects voltage readings on the cell being balanced and adjacent cells.

Table 2: Supported Concurrencies

Active Task	Triggered By	Concurrent Features
High-resolution voltage scan	ADC_SCAN_GO	• Cell-balancing • Coulomb counter
Cell-balancing	BALANCE_GO	• High-resolution voltage scan • Coulomb counter
Open wire	OPEN_WIRE_GO	N/A
Coulomb counter	CC_EN	• High-resolution voltage scan • Cell-balancing

High-Side MOSFET (HS-FET) Control

The MP2790 can leave safe mode and enter normal mode via pin control or register control to turn on the HS-FETs, though only one control method can be selected at a time. The FET_SRC bit selects whether to use the ACTIVE_CTRL register or GPIO1/2 pin(s) to determine whether the device should remain in safe mode or normal mode.

There are two control strategies that can be selected via the FET_CFG register: simple or direct. See the ACT_CFG (05h) section on page 48 for more information.

MOSFET Driving Ability

The HS-FET driver can drive multiple DSG/CHG FETs in parallel. The CP capacitor value must be increased, depending on the number of parallel MOSFETs in the application. See the Selecting the CP Capacitor section on page 141 for more details.

The driver also has a strong turn-off capability, which is equivalent to connecting a resistor (R_{CHG_OFF} or R_{DSG_OFF} in the Electrical Characteristics section page 15) between the gate and source of the MOSFETs while they turn off.

When the TOP voltage (V_{TOP}) is below 18V, CP cannot operate at the normal voltage. For applications with lower series battery packs, it is recommended to set the driver volatge low via FET_DRV_LVL. If FET_DRV_LVL is equal to 0 to 2, the CP voltage regulates in lower mode, which is about 50% of the normal CP voltage. To ensure that the MOSFETs conduct with a low driver voltage, the minimum V_{TOP} for low series battery packs is 10.4V.

DSG MOSFET during Soft Start (SS) (13)

One of the biggest challenges when designing a battery management system (BMS) with HS-FETs is limiting the inrush current and protecting the DSG MOSFET from exceeding its safe operating area (SOA) during turn-on when a large capacitive load is present.

To address this issue, most system designers add what is commonly referred to as a pre-charge or pre-biased external circuit. This type of external circuit requires additional MOSFETs and large power resistors, which act to limit the discharge current while the load capacitance is charging. To eliminate the significant size and cost of this circuit, the MP2790 DSG N-channel MOSFET driver includes an innovative soft-start discharge FET control circuit.

When DSG_SOFTON_EN (see the FET_MODE (13h) section on page 56) is enabled, SS controls the rising slope of the DSG voltage by setting DSG_SOFTON_DV (see the FET_CFG (14h) section on page 58), and thereby reducing the discharging current. To ensure that the DSG MOSFET's SOA is not exceeded during SS, the MP2790 provides three separate over-current (OC) thresholds with different deglitch times (which can be condsidered the response time).

Note:

13) For detailed design guidelines on how to configure the DSG MOSFET SS settings, contact an MPS FAE for the related application note.

Short-Circuit Detection before the DSG MOSFET Starts

The MP2790 supports short-circuit detection before the DSG driver starts to avoid MOSFET damage due to exceeding the SOA. When DSGFET_ON_RUN_SC_DET_EN = 1 (see the FET_MODE (13h) section on page 56) and $V_{PACKP} < V_{TOP}$, short-circuit detection starts if the device receives the DSG start signal. There are several configurable times for this function ranging between 125ms and 1s. The circuit functions by sourcing current onto the PACKP pin for this time and then compares whether the voltage exceeds $V_{PACKP\_SCOC\_REC\_TH}$; if it does, the DSG MOSFET starts. If it does not, the DSG MOSFET does not start and reports the driver fault. There should be a DSG turn-on delay caused by SC detection, and this delay time depends on SCOC_DET_TIME (see the FT1_CFG (62h) section on page 110).

CHG MOSFET Soft Start (SS)

The CHG MOSFET driver supports a configurable SS using CHG_SOFTON_PUP (see the FET_CFG (14h) section on page 58) to set pull-up current values ranging between 3μA and 10μA. When CHG_SOFTON_EN (see the FET_MODE (13h) section on page 56) is enabled and V_{PACKP} exceeds V_{TOP}, the MOSFET drive circuit automatically uses CHG MOSFET soft start to control the output current of the CHG pin, so that V_{GS} rises slowly.

Load and Charger Plug-In Detection

There is an analog comparator between PACKP and TOP that reports whether V_{PACKP} is equal to, greater than, or less than V_{TOP} (see the STB_STATUS (02h) section on page 47).

When CH_PLUGIN_DET_EN or LD_PLUGIN_DET_EN is set to 1, PACK pulls a 250μA current up or down in attempt to make V_{PACKP} equal to V_{TOP}. The expiration time is set by T_PLUGIN_PRECHARGE_MAX. If V_{PACKP} cannot reach V_{TOP}, LDDET_FAIL or CHGDET_FAIL reports to 1. Once V_{PACKP} equals V_{TOP}, CHGDET_ENGAGED or LDDET_ENGAGED reports to 1. If a charger or a load are inserted, the PACKP comparator's state changes.

For the PACKP comparator state and plug-in detection reports, the status can be determined via polling or via interrupts (e.g. CONN_DET_INT_STS, PACKP_V_INT_STS, and PACKP_COMP_STS). See the Interrupts section on page 32 for more details.

GPIO Pins

The GPIO pins can be directly controlled by the MCU via the registers, or they can be assigned to special functions. The GPIO pins have the following functions:

- Push-pull output: The pull-up voltage can be configured to REGIN or 3V3.
- Pull-up capability: Connect a 20kΩ pull-up resistor to REGIN or 3V3.
- Digital input.
- Analog input: Can act as a buffered ADC input with a 0V to 3.3V range. In addition to the GPIO functions, the GPIO1 and GPIO2 pins can also be configured to control the HS-FETs.

In addition to the GPIO capability, GPIO3 can be configured to initiate automatic cell-balancing.

GPIOHV1 Pin

The GPIOHV1 pin can drive the output to V_{TOP} or ground, or be placed in a high-impedance (Hi-Z) state, which can be used to control the bypass P-channel MOSFET. It can also be set as an input and read the logic value.

WDT Pin

The WDT pin is controlled by the watchdog timer (WDT), and provides the following functions:

- Toggles high pulse when a watchdog event occurs to reset an external IC (e.g. the host MCU).
- Triggers a self-reset to the IC by bringing the device back to its default values.
- Can be pulled high externally to reset the device.

Alert (xALERT)

The xALERT pin can be configured to be an active high (3.3V) or active low interrupt pin. When set to active low, xALERT goes low if there is a pending interrupt. When set to active high, this pin goes high if there is a pending interrupt.

Protections and other events trigger this pin, but certain bits must be enabled to ensure that only the relevant sources generate an interruption.

Protections, Interrupts, and Faults

Hardware protections can trigger both interrupts and faults independently (see Figure 12).

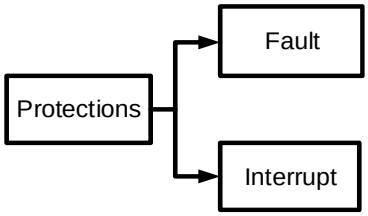


Figure 12: General Faults and Interrupts Architecture

Current Protections

Over-Current Protection (OCP)

All over-current protection (OCP) monitoring is performed with the same over-current (OC) analog comparator. Two possible range (RNG) levels are available for each threshold.

The threshold limit and deglitch are available via the MTP so that the value can be customized during battery pack assembly for different projects. OC1_DCHG_EN_CTRL, OC2_DCHG_EN_CTRL, and OC_CHG_EN_CTRL are the enable bits for discharge OC1, discharge OC2, and charge OC monitoring.

Once enabled, the monitoring function starts during the transition from safe mode to normal mode, and keeps running in normal mode. Use SAFE_SCOC_EN to enable monitoring in safe mode.

The enable bits for OC monitoring can be permanently locked in read-only mode, preventing the MCU from performing further changes. Once OC monitoring is enabled, the interrupt and fault polices can be set.

Discharge Over-Current Protection (OCP)

Two different, independent thresholds are available for discharge OCP: OC1 and OC2. Table 3 lists the resolution and ranges for discharge OC1 and OC2.

Table 3: Discharge OC1 and OC2

Threshold	RNG = 0	RNG = 1 (3x)
LSB (mV)	2.5	7.5
FSR (mV)	80	240

Each limit has its own configurable deglitch time (OC1_DSG_DGL and OC2_DSG_DGL) with two configurable ranges (see Table 4).

In standby mode when the N-channel MOSFETs off, the discharge OC thresholds are set to 2.5mV and the deglitch filter is the shorter value between the configured value and 1ms.

Table 4: OC1 and OC2 Deglitch Times

Deglitch Range	OCx_DSG_ DGL_RNG = 0	OCx_DSG_ DGL_RNG = 1
LSB (ms)	5	40
FSR (ms)	315	2520

Charge Over-Current Protection (OCP)

Table 5 lists the resolution and range for charge OCP.

Table 5: Charge OCP

Threshold	RNG = 0	RNG = 1 (3x)
LSB (mV)	1.6	4.8
FSR (mV)	51.2	153.6

The charge OC limit has its own configurable deglitch time with two configurable ranges (see Table 6).

Table 6: Charge OC Deglitch Time

Deglitch Range	OC_CHG_ DGL_RNG = 0	OC_CHG_ DGL_RNG = 1
LSB (ms)	5	40
FSR (ms)	315	2520

Short-Circuit Protections (SCP)

All short-circuit protection (SCP) monitoring is performed on a single short-circuit analog comparator. Each limit has a configurable deglitch time ranging between 60μs and 25.4ms.

SC_DCHG_EN_CTRL and SC_CHG_EN_CTRL are the enable bits for discharge short-circuit and charge short-circuit monitoring, respectively. Once monitoring is enabled and the MP2790 goes from safe mode to normal mode, the IC begins monitoring.

The SAFE_SCOC_EN register can enable monitoring in safe mode.

Once short-circuit current monitoring is enabled, the interruption and fault polices can be set.

Discharge Short-Circuit

Table 7 on page 31 shows the resolution and range for the discharge short-circuit current limit.

Table 7: Discharge Short-Circuit Current Limit

	Limit		Deglitch Range
	RNG = 0	RNG = 1	
LSB	5.5mV	16.5mV	200µs
FSR	176mV	528mV	25.4ms

Charge Short-Circuit

Table 8 shows the resolution and range for the charge short-circuit current limit.

Table 8: Charge Short-Circuit Current Limit

	Limit		Deglitch Range
	RNG = 0	RNG = 1	
LSB	2.5mV	7.5mV	200µs
FSR	80mV	240mV	25.4ms

Voltage Protections

When enabled, all voltage protections are automatically monitored without needing an MCU to schedule ADC conversion.

An autonomous hardware state machine periodically schedules the conversion for all relevant channels, and the results are internally checked and compared to the limits.

The deglitch filters refer to the number of consecutive readings during which the relevant channel exceeds its thresholds. The interval between readings is typically 254ms, though this value depends on the device's state (e.g. normal mode or standby mode) and how hardware monitoring is configured (e.g. the ACTIVE_MONITOR_CFG register for normal mode and STBY_MONITOR_CFG for standby mode).

Cell Under-Voltage (UV) and Over-Voltage (OV) Thresholds

When fewer than 10 cells are used, only the cells enabled by CELL_S_CTRL are monitored for under-voltage (UV) and over-voltage (OV) conditions.

These thresholds are available in the MTP, which means they can be customized during battery pack assembly for different projects. Table 9 lists the values for the cell OV and UV thresholds.

Table 9: Cell OV and UV Thresholds

Cell OV/UV	Limit	Hysteresis	Deglitch
LSB	19.5mV	19.5mV	1 reading
FSR	4.98V	292.5mV	16

Pack Under-Voltage (UV) and Over-Voltage (OV) Thresholds

The pack OV and UV thresholds are monitored on the C10 pin. These thresholds are available in the MTP, which means they can be customized during battery pack assembly for different projects (see Table 10).

Table 10: Pack OV and UV Thresholds

Pack OV/UV	Limit	Hysteresis	Deglitch
LSB	19.5mV	78mV	1 reading
FSR	80V	4.922V	16

Negative Temperature Coefficient (NTC) Temperature

The negative temperature coefficient (NTC) voltages are checked during the automatic hardware monitoring sequence.

Figure 13 on page 32 shows the block diagram of the NTC-sensing architecture.

All NTC channels are monitored in a ratiometric conversion. This means that the ADC reference is switched to NTCB for the NTC channels. In this scenario, all effects related to NTCB drifts due to the temperature and operating conditions are removed from the reading.

NTC1~4 have limits that can be set according to two modes:

1. Cell monitor mode: The NTC monitors the temperature of the cell. The MP2790 provides four cell temperature limits: hot charging, cold charging, hot discharging, and cold discharging. The hot and cold charging faults can be set to turn off the CHG MOSFETs or the CHG and DSG MOSFETs; the hot and cold discharging faults turn off the CHG and DSG MOSFETs.

   These thresholds can be configured via the MTP, and they can be customized during battery pack assembly for different projects.

2. PCB monitor mode: The NTC monitors the PCB or the protection MOSFET's temperature. A standard hot temperature limit is provided for both the charge and discharge current.

Note that using NTCs results in a lower voltage threshold for OT (hot) conditions and a higher voltage threshold for under-temperature (cold) conditions.

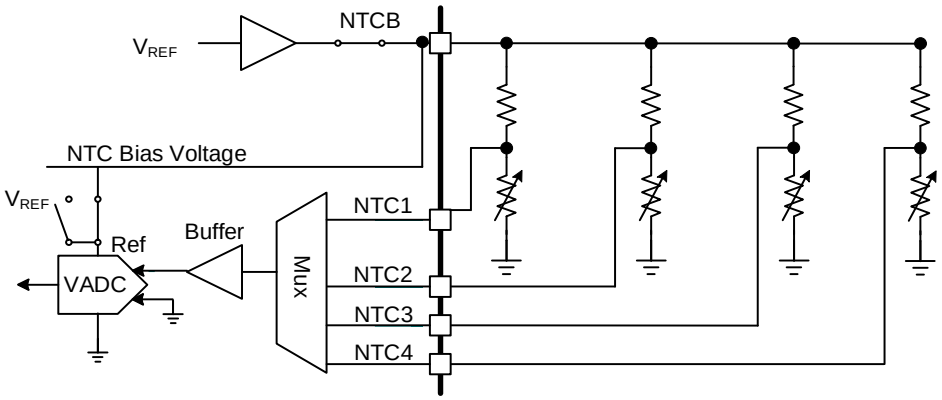


Figure 13: Architecture for NTC ADC Acquisition

Die Temperature

The die temperature alarm has two thresholds. The first is a digital threshold that can be configured between 70°C and 120°C. With this threshold, the comparator's output can put the IC into normal C mode. The second is an analog threshold that forces the device to shut down at 140°C.

The digital die temperature threshold is typically used as an early warning, since the analog threshold forces the IC to shut down. Until the analog OT condition is resolved, the IC remains in a forced shutdown state, and the communication interface is unavailable.

Dead Cells

The pack is monitored at a cell level for dead cells. A dead cell is defined as any cell whose voltage falls below the manufacturer's specified final discharge voltage, in which continued charging should be avoided. If dead cell detection is enabled, the MP2790 checks if any cell is below the configurable threshold (CELL_DEAD_LIMIT), which is typically much lower than the cell's UV threshold.

Once a dead cell condition is detected, the persistent dead cell flag (CELL_DEAD_LOG_STS) is set to 1. When the default values for CELL_DEAD_EN and CELL_DEAD_FAULT_EN are enabled via the OTP, this flag remains at 1 even if the device enters and exits shutdown mode. This flag can be cleared by the CELL_DEAD_DET_CLEAR command, WDT reset, or the fully powered down.

Mismatched Cells

Excessively mismatched or unbalanced cells can be detected by monitoring the maximum and minimum cell voltages.

If the difference between the maximum cell voltage and the minimum cell voltage exceeds a defined threshold, then a cell mismatch status is triggered. The mismatched cell with the higher voltage is reported as an individual flag. The cell with the lowest voltage is reported in the CELL_MSMT_LOWER register.

Diagnostics and Integrity

LDO (REGIN, 3.3V and 1.8V) Rail Monitoring

Low-dropout (LDO) regulator UV thresholds are provided for the REGIN, 3.3V, and 1.8V rails. The UV thresholds are compared to the ADC readings with the same refresh interval as the other voltage monitors, so it measures the nominal rail voltage rather than detecting the spike voltage.

Once LDO monitoring is enabled, the related interrupt and fault polices can be set.

ADC Self-Test Monitoring

The ADC converts a known voltage value and determines whether the conversion result is within a predefined window that accounts for tolerance and temperature shifts.

Once ADC self-test monitoring is enabled, the related interrupt can be set.

NVM Cyclic Redundancy Check (CRC)

NVM CRC is executed when the device exits shutdown mode. If the NVM CRC fails, the device can be configured to enter normal C mode, preventing the BMS from turning on the protection MOSFETs.

Communication CRC

Typically, the CRC detects errors in exchanged data. The MP2790 supports CRC for exchanged data. When this functionality is enabled, the following is possible:

- Write a transaction to 1 register (2 bytes) to append a 1-byte CRC. A correct CRC is required for a successful write transaction.
- Read a transaction for 1 register (2 bytes) to append a 1-byte CRC.
- The read transaction length can be temporarily increased to 126 bytes using a dedicated register. The CRC is appended at the end of the transaction.

The communication CRC is implemented by the CRC-8 algorithm. The CRC can detect 1 incorrect bit. However, all CRC techniques encounter limitations when there are more incorrect bits.

If more than 1 bit is corrupted, error detection depends on the specific pattern. In this scenario, detection can occur, but it is not guaranteed. In general, the ability to detect errors decreases when there is more data to check. For more details, see the I²C Read section on page 39 and the SPI Read section on page 40.

Watchdog Timer

The watchdog timer monitors communication via the I²C or SPI interface. If there is no write to the WDT_RST register within a certain interval, the timer is triggered. The watchdog has a bark-bite style.

The bark notifies the device when the MCU has failed to clear the watchdog timer. This results in a bark timeout, which can be configured to trigger the alert pin. The WDT bark counter setting is 25ms per LSB, with up to 3.2 seconds maximum.

After a bite timeout, there is an optional feature to reset the device's registers to the default values. The WDT bite counter setting is 25ms per LSB, with up to 3.2 seconds maximum.

Using the bidirectional, configurable WDT, it is possible to set up the IC to self-reset and/or to reset an external IC if its reset trigger is connected to the WDT pin.

Interrupts

Interrupt statuses are split between 2 register addresses (RD_INT0 and RD_INT1). Each interrupt source has a matching enable bit and a dedicated clear bit to clear the interrupt. Table 11 on page 34 shows the main interrupts. Table 12 on page 35 shows additional interrupts.

The interrupt source can be configured using a TYPE selector. Depending on the interrupt, the TYPE selector provides a few options:

- Level (high)
- Rising edge
- Falling edge
- Rising and falling edge

Each interrupt that is related to a protection flag follows the processes described above.

Table 11: Main Interrupts (RD_INT0)

Condition	Flag	Description	Related Status Register(s)
Cell OV	CELL_OV_INT_STS	Unified flag for cell OV conditions. The related register reports each cell's OV flag, which is checked to determine which cell is generating the interrupt.	Flags in address, RD_CELL_OV
Cell UV	CELL_UV_INT_STS	Unified flag for cell UV conditions. The related register reports each cell's UV flag, which is checked to determine which cell is generating the interrupt.	Flags in address, RD_CELL_UV
Stack TOP OV	VTOP_OV_INT_STS	Dedicated flag for battery pack OV conditions detected on the C10 pin.	
Stack TOP UV	VTOP_UV_INT_STS	Dedicated flag for battery pack UV conditions detected on the C10 pin. This is unrelated to the V_{TOP} UV analog threshold.	
OC	OVER_CURR_INT_STS	OC interrupt for charge, discharge 1, and discharge 2.	OC1_DCHG_STS, OC2_DCHG_STS, OC_CHG_STS
SCP	SHORT_CURR_INT_STS	Short-circuit interrupt for both charge and discharge.	SC_CHG_STS, SC_DCHG_STS
NTC discharge	NTC_DSG_INT_STS	Unified flag for cell NTC discharging hot/cold conditions for all NTC channels. To identify which NTC is the source of the interrupt, the additional individual flags can be checked.	NTC1_CELL_DSG_STS, NTC2_CELL_DSG_STS, NTC3_CELL_DSG_STS, NTC4_CELL_DSG_STS
NTC charge	NTC_CHG_INT_STS	Unified flag for cell NTC charging hot/cold conditions for all NTC channels. To identify which NTC is the source of the interrupt, the additional individual flags can be checked.	NTC1_CELL_CHG_STS, NTC2_CELL_CHG_STS, NTC3_CELL_CHG_STS, NTC4_CELL_CHG_STS
Watchdog interrupt	WDT_INT_STS	Notification for either a bite or bark event from the communication watchdog timer.	WDT_BARKED, WDT_BITE
Fault recovered	RECOVERED_INT_STS	Notification that the system recovers from a normal C state, including both automatic fault recovery and a manual MCU clearing.	
AFE mode change	AFE_MODE_CHANGE_INT_STS	The AFE has changed states (e.g. safe mode, normal A/B/C mode, standby mode).	PWR_STATE
Scan complete	VSCAN_DONE_INT_STS	Notification that the high-resolution voltage ADC scan has finished converting of all the channels on its list.	
CC done	CC_ACC_INT_STS	Flag reporting that a new Coulomb counting accumulation value has been updated to CC_ACC_LSBS and CC_ACC_MSBS.	
Plug-in detection	CONN_DET_INT_STS	The plug-in detection logic reports that either a device (capacitive load or charger) has been connected, or the detection cannot be successfully complete.	LD_IN, CHG_IN, CHGDET_FAIL, LDDET_FAIL
Pack current	PACK_CURRENT_INT_STS	Interrupt indicating a change in the battery pack current range (discharge, standby, or charge).	PACK_CURRENT_STATUS

Table 12: Additional Interrupts (RD_INT1)

Name	Flag	Description	Related Status Register(s)
FET driver	FET_DRIVER_INT_STS	Reports a MOSFET driver issue such as the following: • FET timeout: the DSG or CHG driver did not reach its final voltage within the timeout interval • A lower level OC condition occurs during CHG or DSG soft start • A short-circuit is issued before DSG turns on	FET_TIMEOUT
PACKP voltage	PACKP_V_INT_STS	The voltage on PACKP node has changed compared to V_{TOP}. Note that the PACKP comparator is invalid when disabled or during short-circuit removal, but still reports to the interrupt.	PACKP_COMP_STS
Balancing complete	BAL_DONE_INT_STS	Balancing has been completed.	Flags in address, BAL_STS
Self-test fail	SELF_TEST_INT_STS	The ADC is failing its self-diagnostic test and/or the conversion of this value is outside the specified boundaries.	SELF_TEST_STS_OV, SELF_TEST_STS_UV
Scheduler error	FSM_ERROR_INT_STS	The scheduler was busy when a new feature command was requested, and concurrent operation is not supported. For example, the device may report that an MCU conversion command is ignored since open-wire detection is running, or it may report that a cell-balancing command is ignored since open-wire detection is running.	
PCB temperature hot	PCB_MNTR_HOT_INT_STS	Unified flag for NTC hot conditions for all NTC channels configured in PCB mode. To identify which NTC is the source of the interrupt, the individual flags should be checked.	NTC1_PCB_MNTR_HOT_STS, NTC2_PCB_MNTR_HOT_STS, NTC3_PCB_MNTR_HOT_STS, NTC4_PCB_MNTR_HOT_STS
Die temperature	DIE_TEMP_INT_STS	The die temperature is too high, reported by the digital die temperature check.	
Mismatched cells	CELL_MISMATCH_INT_STS	The voltage difference between cells is too great.	Flags in address, RD_CELL_MSMT
Dead cell	CELL_DEAD_INT_STS	The dead cell threshold has been reached.	Flags in address, RD_CELL_DEAD
Open wire	OPEN_WIRE_INT_STS	Open-wire detection is complete. The open-wire interrupt status register must be checked to identify if there are any disconnected wires.	Flags in address, RD_OPENH, RD_OPENL
VDD	VDD_INT_STS	The VDD rail is below the defined UV threshold.	
3V3	3V3_INT_STS	The 3.3V rail is below the defined UV threshold.	
REGIN	REGIN_INT_STS	The REGIN rail is below the defined UV threshold.	
OTP CRC	OTP_CRC_EVENT_INT_STS	The CRC stored in the OTP does not match the computed CRC value from OTP memory readback. The manual CRC check is completed.	

Fault

After the device has triggered the fault protection, it performs the appropriate MOSFET turn-off behavior according to the type of fault. Faults can be cleared either by an automatic recovery or manual MCU clearing.

The fault enable control bit is effective when the function has been enabled. For example, the cell OV fault is enabled by CELL_OV_FAULT_EN = 1 (fault enable) and CELL_OV_EN_CTRL = 1 (function enable).

The fault enable control bit for each fault has a configurable default value, and the option to permanently lock the register in read-only mode.

Table 13 lists certain faults and their recovery methods. Table 14 on page 38 lists additional faults and their recovery methods.

Table 13: Fault and Recovery Management (Part I)

Fault	Enable Control	Behavior in Fault	Recovery Method(s)
Cell OV	CELL_OV_ FAULT_EN	Configurable by CELL_OV_FAULT_ACTION 0: Turn off CHG FETs 1: Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (CELL_OV_FAULT_CLR) • Automatic recovery: This method is enabled with CELL_OV_REC An additional logic option is available via CELL_OV_CHG_REC_MODE. When it is set to 1, if automatic recovery is enabled and set as CHG FET off only, the CHG FET automatically turns on when a discharge condition is detected (V_{PACKP} < V_{TOP} or discharge current), while the fault state remains until the cell voltage returns to normal.
Cell UV	CELL_UV_ FAULT_EN	Configurable by CELL_UV_FAULT_ACTION 0: Turn off DSG FETs 1: Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (CELL_UV_FAULT_CLR) • Automatic recovery: This method is enabled with CELL_UV_REC An additional logic option is available via CELL_UV_DSG_REC_MODE. When it is set to 1, if automatic recovery is enabled and set as DSG FET off only, the DSG FET automatically turns on when a charge condition is detected (V_{PACKP} > V_{TOP} or discharge current), while the fault state remains until the cell voltage returns to normal.
Dead cell	CELL_DEAD_ FAULT_EN	Turn off CHG and DSG FETs	The host MCU writes to the fault clear command (CELL_DEAD_FAULT_CLR). CELL_DEAD_LOG_STS prevents the IC from entering normal mode, which can be cleared by the CELL_DEAD_DET_CLEAR command.
Cell mismatch	CELL_MSMT_ FAULT_EN	Turn off CHG and DSG FETs	The host MCU writes to CELL_MSMT_FAULT_CLR.
Open wire	OPEN_WIRE_ FAULT_EN	Turn off CHG and DSG FETs	The host MCU writes to OPEN_WIRE_FAULT_CLR.
Stack TOP OV	VTOP_OV_ FAULT_EN_ CTRL	Turn off CHG and DSG FETs	The host MCU writes to VTOP_OV_FAULT_CLR.
Stack TOP UV	VTOP_UV_ FAULT_EN_ CTRL	Turn off CHG and DSG FETs	The host MCU writes to VTOP_UV_FAULT_CLR.

Cell NTC too hot (discharge)	NTC_CELL_DSG_FAULT_EN	Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_DSG_FAULT_CLR) • Automatic mode: The device recovers when the NTC voltage (V_{NTC}) exceeds (hot discharge threshold + hysteresis). This method is enabled with NTC_CELL_DSG_REC. If NTC_CELL_STBY_MODE = 0, when the battery pack current status is in standby, the fault action and recovery is the same as it would be for discharge.
Cell NTC too cold (discharge)	NTC_CELL_DSG_FAULT_EN	Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_DSG_FAULT_CLR) • Automatic mode: The device recovers when V_{NTC} falls below (cold discharge threshold - hysteresis). This method is enabled with NTC_CELL_DSG_REC. If NTC_CELL_STBY_MODE = 0, when the battery pack current status is in standby, the fault action and recovery is the same as it would be for discharge.
Cell NTC too hot (charge)	NTC_CELL_CHG_FAULT_EN	Configurable by NTC_CELL_CHG_ACTION 0: Turn off CHG FETs 1: Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_CHG_FAULT_CLR) • Automatic recovery: The device recovers when V_{NTC} exceeds (hot charge threshold + hysteresis). This method is enabled with NTC_CELL_CHG_REC. An additional recovery logic option is available via NTC_CELL_CHG_REC_MODE. If it is set to 1, automatic recovery is enabled, and set as CHG FET off only. The CHG FET automatically turns on when a discharge current is detected. The fault state remains until V_{NTC} exceeds (hot charge threshold + hysteresis). If NTC_CELL_STBY_MODE = 1, when battery pack current status is standby, the fault action and recovery is the same as it would be for charge.
Cell NTC too cold (charge)	NTC_CELL_CHG_FAULT_EN	Configurable by NTC_CELL_CHG_ACTION 0: Turn off CHG FETs 1: Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The MCU writes to the clear bit (NTC_CELL_CHG_FAULT_CLR) • Automatic recovery: The device recovers when V_{NTC} falls below (cold charge threshold - hysteresis). This method is enabled via NTC_CELL_CHG_REC. An additional recovery logic option is available via NTC_CELL_CHG_REC_MODE. If it is set to 1, automatic recovery is enabled, and set as CHG FET off only. The CHG FET automatically turns on when a discharge current is detected. The fault state remains until V_{NTC} falls below (cold charge threshold - hysteresis). If NTC_CELL_STBY_MODE = 1, when battery pack current status is standby, the fault action and recovery is the same as it would be for charge.

Table 14: Fault and Recovery Management (Part II)

Fault	Enable Control	Behavior in Fault	Recovery Method(s)
Pack OC discharge 1	OC1_DCHG_ FAULT_EN	Turn off DSG FETs only	Manual recovery only. The host MCU writes to the fault clear command (OC1_DCHG_FAULT_CLR)
Pack OC discharge 2	OC2_DCHG_ FAULT_EN	Turn off DSG FETs only	Manual recovery only: The host MCU writes to the fault clear command (OC2_DCHG_FAULT_CLR)
Pack OC charge	OC_CHG_ FAULT_EN	Turn off CHG FETs only	Manual recovery only: The host MCU writes to the fault clear command (OC_CHG_FAULT_CLR)
Pack short-circuit current discharge	SC_DCHG_ FAULT_EN	Turn off DSG FETs only	Manual recovery only: The host MCU writes to the fault clear command (SC_DCHG_FAULT_CLR)
Pack short-circuit current charge	SC_CHG_ FAULT_EN	Turn off CHG FETs only	Manual recovery only: The host MCU writes to the fault clear command (SC_CHG_FAULT_CLR)
3.3V or VDD UV	3V3_VDD_ FAULT_EN	Turn off CHG and DSG FETs	Manual recovery only. The host MCU writes to the fault clear command (3V3_VDD_FAULT_CLR).
PCB monitor too hot	PCB_MNTR_ FAULT_EN	Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (PCB_MNTR _FAULT_CLR) • Automatic recovery: The device recovers when the NTC voltage exceeds (monitor hot threshold + hysteresis). This method is enabled with PCB_MNTR_REC.
Die too hot digital	DIE_TEMP_ DIG_FAULT_ EN	Turn off CHG and DSG FETs	Configurable for manual or automatic recovery. • Manual recovery: The host MCU writes to the fault clear command (DIE_TEMP_FAULT_CLR) • Automatic recovery: The device waits for the die temperature to drop below (digital temperature threshold - hysteresis). This method is enabled with DIE_TEMP_FAULT_REC.
Die too hot analog	N/A; hardcoded enable	Turn off CHG and DSG FETs	The IC returns to safe mode from shutdown mode once the die temperature drops below (analog temperature threshold - hysteresis).
Driver turn on fail	N/A; hardcoded enable	Turn off CHG and DSG FETs	Manual recovery only. The host MCU writes to the fault clear command (DRIVER_FAULT_CLR).

I²C Interface

The MP2790 can use an I²C interface to flexibly set parameters and report device statuses instantaneously. The I²C is a two-wire serial interface with two bus lines: a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are open drains, and they must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device that receives control inputs from the master device, such as a microcontroller (MCU). SCL is always driven by the master device. The I²C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A start command is defined as a high-to-low transition on the SDA while the SCL is high. A stop command is defined as a low-to-high transition on the SDA while the SCL is high (see Figure 14).

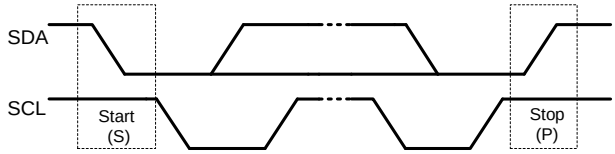


Figure 14: Start and Stop Commands

For data validity, the data on the SDA must be stable during the high period of the clock. The high or low state of the SDA can only change when the clock signal on the SCL is low (see Figure 15).

Every byte on the SDA must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

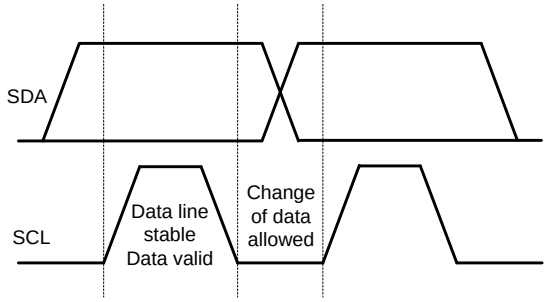


Figure 15: Bit Transfer on the I²C Bus

Each byte must be followed by an acknowledge (ACK) bit, which is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal occurs when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low. The SDA line stays low during the high period of the ninth clock.

If the SDA line is high during the 9th clock pulse, this is defined as a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer, or a repeated start (Sr) command to start a new transfer.

After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 16 shows the address bit arrangement.

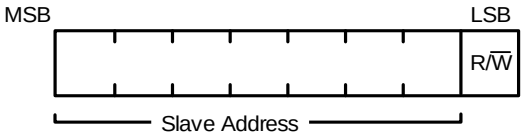


Figure 16: 7-Bit Address

Figure 17 shows a data transfer on the I²C bus.

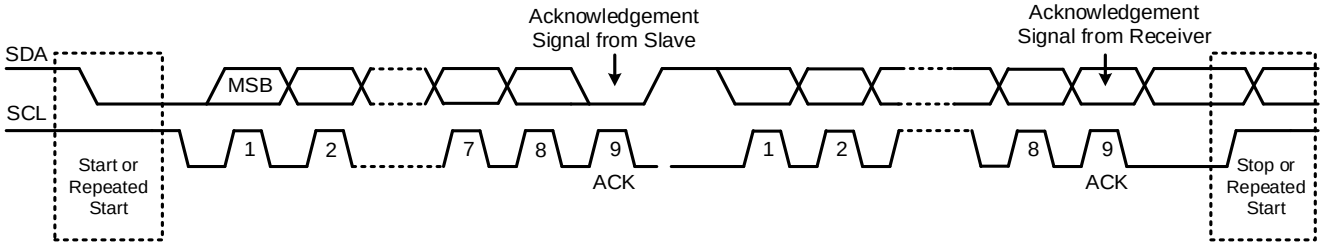


Figure 17: Data Transfer on the I²C Bus

I²C Read

When CRC is enabled, the payload is limited to 2 bytes by default. This value can be increased to 63 words (126 bytes) using the XFR_NUM_RD_WORDS register. XFR_NUM_RD_WORDS retains the new value only for the next transaction, so ensure that the next transaction uses the increased payload count (see Figure 18).

CRC in an I²C Read Transaction

After completing the request for a read transaction, the host MCU must ensure that the CRC matches the value provided in the read transaction to confirm that no bits were corrupted during the transmission.

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes, following the order in which the bytes are transmitted or received. If it were bit-wise, the MSB would be processed first in each byte. An example of this sequence is shown below:

1. Slave address byte + write (0x02)
2. Register address byte (0x00)
3. Slave address byte + read (0x03)
4. Register address byte (0x00)
5. Word 1 - byte 1 / bits[7:0] (0x7C)
6. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x36 being appended as the last CRC byte.

Although this byte of the fourth sequence does not exist in the actual read sequence, it must be added in the CRC calculation.

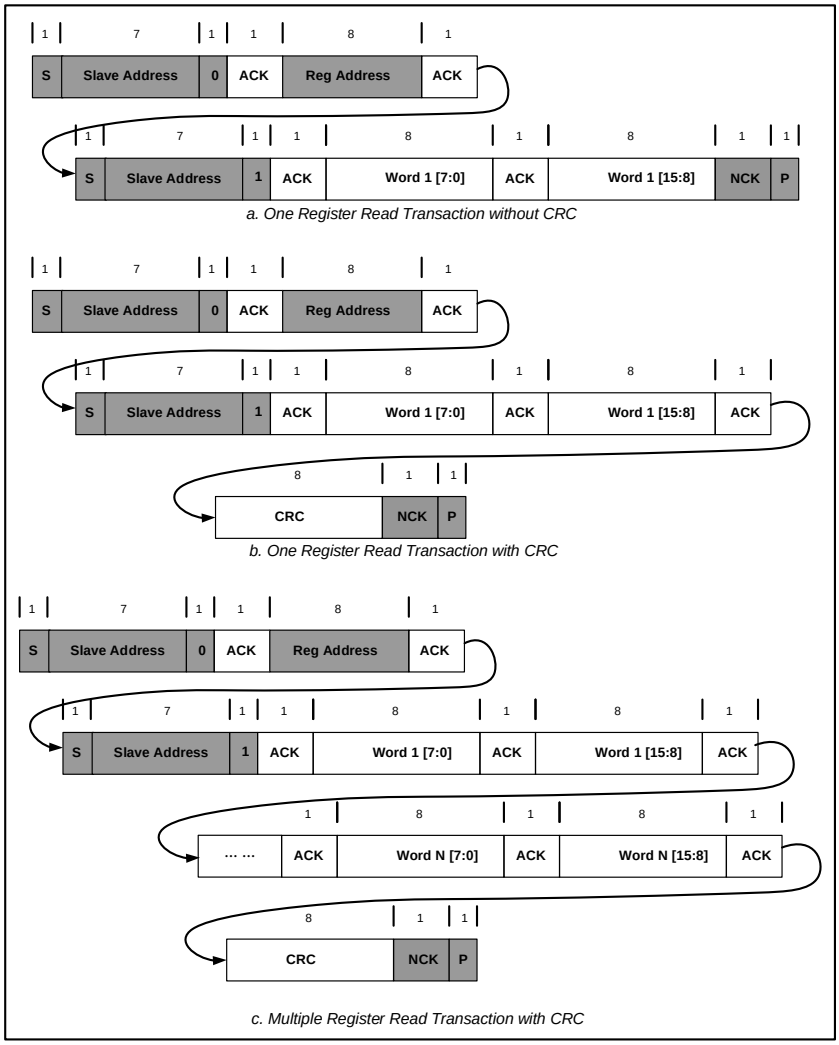


Figure 18: I²C Read

I²C Write

Figure 19 shows how the byte is ordered in a write transaction. When CRC is enabled, the targeted register address is modified according to payload only if the CRC results match.

CRC in an I²C Write Transaction

The CRC-8 algorithm follows the polynomial ($1 + x^1 + x^2 + x^8$), and is applied byte-wise to the bytes following the order in which they are transmitted or received. If it were bit-wise, the MSB would first be processed in each byte. An example of this sequence is shown below:

1. Slave address byte + write (0x02)
2. Register address byte (0x00)
3. Word 1 - byte 1 / bits[7:0] (0x7C)
4. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x72, which the host MCU should append as the last CRC byte to ensure a successful transaction.

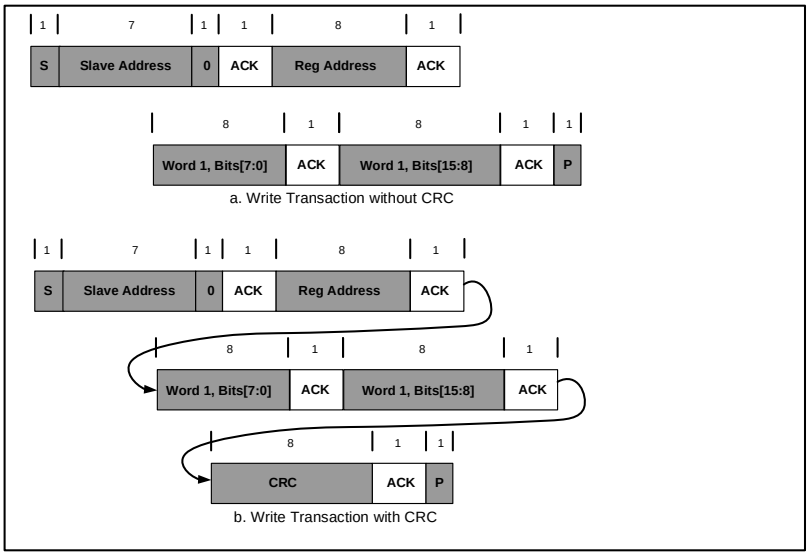


Figure 19: I²C Write Transaction

Serial Peripheral Interface (SPI)

The MP2790 has an interface that is compatible with serial peripheral interfaces (SPIs). This interface is configured to operate using clock phase (CPHA) = 1 and clock polarity (CPOL) = 1. Consequently, data on SDI must be stable during SCK's rising edge. Words are transferred with most significant bit (MSB) first.

During a write transaction, the data value on SDI is latched to the device on SCK's rising edge. During a read transaction, the bit stream is presented on SDO with the MSB first, and is valid during SCK's rising edge, while the SDO transitions on SCK's falling edge.

nCS must remain low for the entire command sequence duration, including the time between the command byte and subsequent data. During a write command, data is latched on nCS's rising edge (see Figure 20 on page 42).

SPI Data Protocol

For a successful SPI transaction, nCS must go low and there must be a successful match between the transaction slave address and the internally configured slave address (located in register DEVICE_ADD). The MP2790's SPI requires a specific transaction structure.

SPI Read

Read transactions should have the fields arranged with a matching order for the slave address, read bit, register address, and data payload (see Figure 21 on page 43).

When CRC is enabled, the payload is limited to two bytes by default. This value can be increased to 63 words (126 bytes) using the XFR_NUM_RD_WORDS register. XFR_NUM_RD_WORDS retains the new value only for the next transaction, so ensure that the next transaction uses the increased payload count.

CRC in an SPI Read Transaction

After completing the request for a read transaction, the host MCU must ensure that the CRC matches the value provided in the read transaction to confirm that no bits were corrupted during the transmission.

The CRC-8 algorithm follows the polynomial (1 + x^1 + x^2 + x^8), and it is applied byte-wise to the bytes, following the order in which bytes are transmitted or received. . When applied bit-wise, the MSB is first processed in each byte. An example of this sequence is shown below:

1. Slave address byte + read (0x03)
2. Register address byte (0x00)
3. Word 1 - byte 1 / bits[7:0] (0x7C)
4. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x64 being appended as the last CRC byte.

SPI Write

Write transactions should have the fields arranged with a slave address, write bit, register address, and data payload (see Figure 22 on page 43). When CRC is enabled, the SPI write payload is limited to 2 bytes and targeted register addresses are modified according to the payload only if the CRC matches.

CRC in an SPI Write Transaction

The CRC-8 algorithm follows the polynomial (1 + x^1 + x^2 + x^8), and it is applied byte-wise to the bytes following the order in which they are transmitted or received. When applied bit-wise, the MSB is first processed in each byte. An example of this sequence is shown below:

1. Slave address byte + write (0x02)
2. Register address byte (0x00)
3. Word 1 - byte 1 / bits[7:0] (0x7C)
4. Word 1 - byte 2 / bits[15:8] (0x00)

This sequence results in CRC = 0x72, which the host MCU should append as the last CRC byte to ensure a successful transaction.

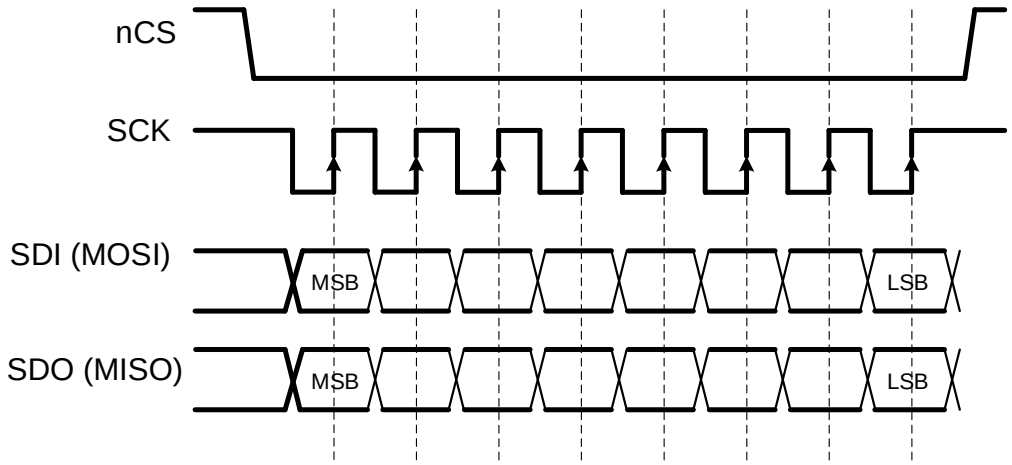
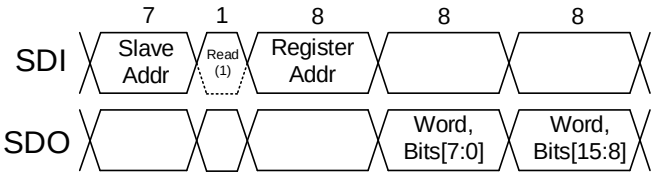
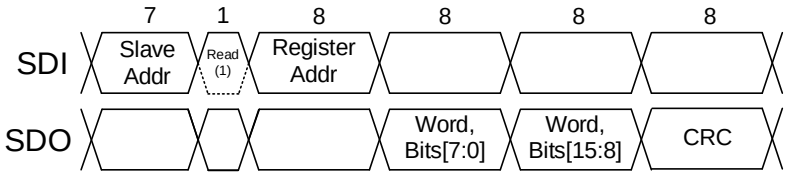


Figure 20: SPI Signal Sequencing

SPI Read without CRC: 1 Word (2 Bytes)



SPI Read with CRC: 1 Word (2 Bytes) Payload



SPI Read with CRC: 2 Words (4 Bytes) Payload

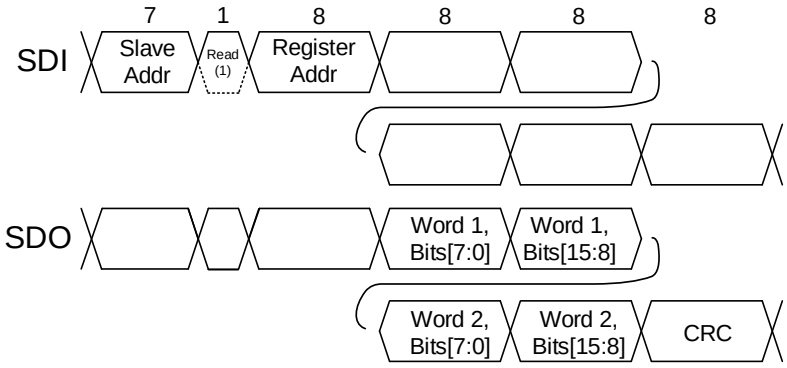
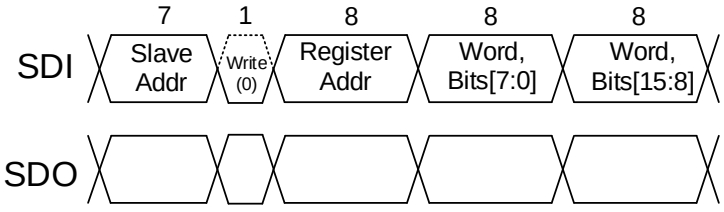


Figure 21: SPI Read Transaction

SPI Write without CRC: 1 Word (2 Bytes)



SPI Write with CRC: 1 Word (2 Bytes)

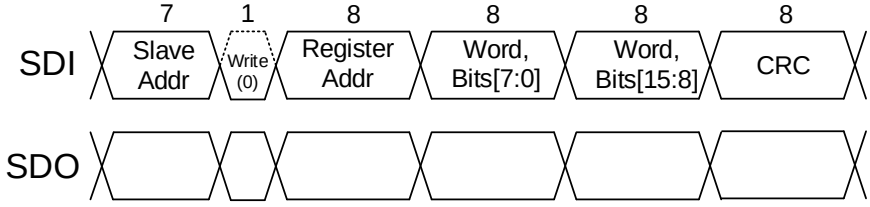


Figure 22: SPI Write Transaction

SUPPORTED COMMANDS

The default slave address is 01h. The address can be configured by modifying DEVICE_ADD (see the COMM_CFG (A3h) section on page 124 for more information). Once the value has been changed, the next communication should use the new address. Note that the default address may be different for chips with different -xxxx suffixes.

Command Code	Command Name	Type	Bytes
00h	CELLS_CTRL	RW	2
01h	PWR_STATUS	R	2
02h	STB_STATUS	R	2
03h	LOAD_CHARGER_STATUS	R	2
05h	ACT_CFG	RW	2
06h	STB_CFG	RW	2
07h	SAFE_CFG	RW	2
08h	RGL_CFG	RW	2
09h	LOAD_CHARGER_CFG	RW	2
0Ah	GPIO_STATUS	R	2
0Bh	GPIO_OUT	RW	2
0Ch	GPIO_CFG	RW	2
0Dh	PINS_CFG	RW	2
0Eh	WDT_STATUS	R	2
0Fh	WDT_RST	W	2
10h	WDT_CFG	RW	2
11h	FET_STATUS	R	2
12h	FET_CTRL	RW	2
13h	FET_MODE	RW	2
14h	FET_CFG	RW	2
15h	RD_INT0	R	2
16h	RD_INT1	R	2
17h	INT0_CLR	W	2
18h	INT1_CLR	W	2
19h	INT0_EN	RW	2
1Ah	INT1_EN	RW	2
1Bh	INT_TYPE0	RW	2
1Ch	INT_TYPE1	RW	2
1Dh	INT_TYPE2	RW	2
1Eh	MASK_INT0	RW	2
1Fh	MASK_INT1	RW	2
20h	OC_STATUS	R	2
23h	OCFT_CTRL	RW	2
24h	DSGOC_LIM	RW	2
25h	DSGOC_DEG	RW	2
26h	CHGOC_DEG	RW	2
27h	SC_STATUS	R	2
2Ah	SCFT_CTRL	RW	2
2Bh	DSGSC_CFG	RW	2
2Ch	CHGSC_CFG	RW	2
2Dh	RD_CELL_UV	R	2
2Eh	RD_CELL_OV	R	2
2Fh	RD_CELL_MSMT	R	2
30h	RD_CELL_DEAD	R	2
33h	CELL_MSMT_STS	R	2
34h	PACKFT_CTRL	RW	2
35h	CELLFT_CTRL	RW	2
36h	CELL_HYST	RW	2
37h	PACK_UV_OV	R	2

SUPPORTED COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes
38h	CELL_UV	RW	2
39h	CELL_OV	RW	2
3Ah	PACK_UV	RW	2
3Bh	PACK_OV	RW	2
3Ch	CELL_DEAD_THR	RW	2
3Dh	CELL_MSMT	RW	2
3Eh	RD_NTC_DIE	R	2
3Fh	RD_V_NTC4_LR	R	2
40h	RD_V_NTC3_LR	R	2
41h	RD_V_NTC2_LR	R	2
42h	RD_V_NTC1_LR	R	2
43h	RD_T_DIE	R	2
44h	NTC_CLR	W	2
46h	DIE_CFG	RW	2
47h	NTC_CFG	RW	2
48h	NTCC_OTHR_DSG	RW	2
49h	NTCC_UTHR_DSG	RW	2
4Ah	NTCC_OTHR_CHG	RW	2
4Bh	NTCC_UTHR_CHG	RW	2
4Ch	NTCM_OTHR	RW	2
4Dh	DIE_OT	RW	2
4Eh	SELF_STS	R	2
4Fh	RD_VA1P8	R	2
50h	RD_VA3P3	R	2
51h	RD_VA5	R	2
52h	RD_VASELF	R	2
53h	RD_OPENH	R	2
55h	SFT_GO	R	2
56h	SELF_CFG	RW	2
57h	OPEN_CFG	RW	2
58h	REGIN_UV	RW	2
59h	V3P3_UV	RW	2
5Ah	VDD_UV	RW	2
5Bh	SELF_THR	RW	2
5Dh	FT_STS1	R	2
5Eh	FT_STS2	R	2
5Fh	FT_CLR	W	2
60h	FT_REC	W	2
61h	FT0_CFG	RW	2
62h	FT1_CFG	RW	2
65h	RD_CCIRQL	R	2
66h	RD_CCIRQH	R	2
67h	RD_CCACCQL	R	2
68h	RD_CCACCQH	R	2
69h	RD_VPACKP	R	2
6Ah	RD_VTOP	R	2
6Bh	RD_ITOP	R	2
6Ch	RD_VCELL1	R	2
6Dh	RD_ICELL1	R	2
6Eh	RD_VCELL2	R	2
6Fh	RD_ICELL2	R	2
70h	RD_VCELL3	R	2
71h	RD_ICELL3	R	2
72h	RD_VCELL4	R	2
73h	RD_ICELL4	R	2

SUPPORTED COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes
74h	RD_VCELL5	R	2
75h	RD_ICELL5	R	2
76h	RD_VCELL6	R	2
77h	RD_ICELL6	R	2
78h	RD_VCELL7	R	2
79h	RD_ICELL7	R	2
7Ah	RD_VCELL8	R	2
7Bh	RD_ICELL8	R	2
7Ch	RD_VCELL9	R	2
7Dh	RD_ICELL9	R	2
7Eh	RD_VCELL10	R	2
7Fh	RD_ICELL10	R	2
8Ch	RD_VNTC4	R	2
8Dh	RD_VNTC3	R	2
8Eh	RD_VNTC2	R	2
8Fh	RD_VNTC1	R	2
90h	RD_VGPIO3	R	2
91h	RD_VGPIO2	R	2
92h	RD_VGPIO1	R	2
93h	RD_TDIE	R	2
94h	RD_V1P8	R	2
95h	RD_V3P3	R	2
96h	RD_V5	R	2
97h	CC_STS	R	2
98h	ADC_STS	R	2
99h	ADC_CTRL	RW	2
9Ah	CC_CFG	RW	2
9Bh	TRIMG_IPCB	RW	2
9Ch	HR_SCAN0	RW	2
9Dh	HR_SCAN1	RW	2
9Eh	HR_SCAN2	RW	2
A0h	SILC_INFO1	RW	2
A3h	COMM_CFG	RW	2
A4h	BAL_STS	R	2
A5h	BAL_LIST	RW	2
A6h	BAL_CTRL	RW	2
A7h	BAL_CFG	RW	2
A8h	BAL_THR	RW	2
B4h	MEM_STATUS	R	2
B8h	OTP_STORE_CMD	R	2
B9h	STORE_CMD_ACCESS_CODE	RW	2

REGISTER MAP

The value of these reserved bits may be 0 or 1. In the write operation to the command code with reserved bit, these reserved bits must be filled with 0. After the write operation, the value of these reserved bits is the same as their initial value.

CELLS_CTRL (00h)

Format: Unsigned binary

The CELLS_CTRL command controls the number of stacked cells in use.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3:0	R/W (can lock to read-only)	CELL_S_CTRL	4'b 1001	Sets the number of stacked cells in use. These bits allow MTP. 0x0: Not allowed 0x1: Not allowed 0x2: Not allowed 0x3: Cells 6~3 enabled 0x4: Cells 6~2 enabled 0x5: Cells 6~1 enabled 0x6: Cells 7~1 enabled 0x7: Cells 8~1 enabled 0x8: Cells 9~1 enabled 0x9: Cells 10~1 enabled 0xA: Cells 10~1 enabled 0xB: Cells 10~1 enabled 0xC: Cells 10~1 enabled 0xD: Cells 10~1 enabled 0xE: Cells 10~1 enabled 0xF: Cells 10~1 enabled

PWR_STATUS (01h)

Format: Unsigned binary

The PWR_STATUS command reports the pack current status and the power state status.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:7	R	PACK_CURRENT_STATUS	3'b 010	Returns the pack current status. 0x1: The battery pack current is discharging 0x2: The battery pack current is in the standby range, meaning it is within ±STBY_CUR_TH 0x4: The battery pack current is charging
6:5	R	RESERVED	N/A	Reserved. Do not change this register value.
4:0	R	PWR_STATE	5'b 00001	Returns the power state status. 0x01: Safe 0x02: Standby 0x04: Normal B 0x08: Normal C 0x10: Normal A

STB_STATUS (02h)

Format: Unsigned binary

The STB_STATUS command reports the voltage comparison result between PACKP and V_{TOP}. It also reports the SBYDSG driver status, and the on/off setting for standby mode.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10:8	R	PACKP_COMP_STS	3'b 000	Reports the voltage comparison result between PACKP and V_{TOP}. The exact voltage level for the transition can be slightly different based on the direction of the transition and the applied hysteresis. 0x4: $V_{PACKP} > V_{TOP}$ + 280mV 0x3: The PACKP comparator is invalid 0x2: V_{TOP} + 160mV > $V_{PACKP} > V_{TOP}$ - 1V 0x1: $V_{PACKP} < V_{TOP}$ - 1.77V 0x0: The comparison result is not available
7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R	DSG_PFET_SYNC	1'b 0	Reports whether the SBYDSG driver is on or off. 0: Off 1: On
5:1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R	STBY_STATE	1'b 0	Reports the on/off setting for standby mode. If off, the AFE does not transition to standby mode from normal B mode, regardless of whether the current level is in the standby mode range. 0: Off 1: On

LOAD_CHARGER_STATUS (03h)

Format: Unsigned binary

The LOAD_CHARGER_STATUS command reports the charger/load plug-in detection process and result.

Bits	Access	Bit Name	Default	Description
15	R	CHG_IN	1'b 0	Reports whether a charger plug-in event was detected. This bit can be cleared by writing 0 to CHG_LD_CLR. 0: Not detected 1: Detected
14	R	LD_IN	1'b 0	Reports whether a load plug-in event was detected. This bit can be cleared by writing 0 to CHG_LD_CLR. 0: Not detected 1: Detected
13	R	CHGDET_FAIL	1'b 0	Reports the outcome of pre-bias PACKP detection. When true, charger plug-in detection could not pre-charge the PACKP voltage to the TOP voltage in the allocated time, so there is no engagement. When false, detection is in a different state. 0: False 1: True

12	R	LDDET_FAIL	1’b 0	Reports the outcome of pre-biased PACKP detection. When true, the load plug-in detection could not pre-charge the PACKP voltage to the TOP voltage in the allocated time, so there is no engagement. When false, detection is in a different state. 0: False 1: True
11:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5	R	CHGDET_ENGAGED	1’b 0	Reports the status of pre-biased PACKP detection. When true, the PACKP voltage has reached the TOP voltage and is waiting to detect a plug-in. The state machine for charger plug-in detection is enabled, and the current source/sink is enabled. When false, detection is ineffective. 0: False 1: True
4	R	LDDET_ENGAGED	1’b 0	Reports the status of pre-biased PACKP detection. When true, the PACKP voltage has reached the TOP voltage and is waiting to detect a plug-in. The state machine for load plug-in detection is enabled, and the current source/sink is enabled. When false, detection is ineffective. 0: False 1: True
3	R	CHG_SETTLING	1’b 0	Reports the status of PACKP detection for pre-charging. When true, the PACKP voltage is approaching the TOP voltage, but has not reached it. The state machine for charger plug-in detection is enabled, and the current source/sink is enabled. When false, a different state has been detected. 0: False 1: True
2	R	LD_SETTLING	1’b 0	Reports the status of PACKP detection for pre-charging. When true, the PACKP voltage is approaching the TOP voltage, but has not reached it. The state machine for load plug-in detection is enabled, and the current source/sink is enabled. When false, a different state has been detected. 0: False 1: True
1	R	CHCONN_EN	1’b 0	Reports whether charger plug-in detection is enabled. 0: Disabled 1: Enabled
0	R	LDDET_EN	1’b 0	Reports whether load plug-in detection is enabled. 0: Disabled 1: Enabled

ACT_CFG (05h)

Format: Unsigned binary

The ACT_CFG command configures the MOSFET transition method, turn-on/off command, control logic, and control method.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.

9	R/W (can lock to read-only)	FT_STATE_SEL	1’b 0	When this bit is set to 0, the MOSFETs transition to start-up via a control source (depending on FET_SRC); this source is disabled then enabled. When this bit is set to 1, the MOSFETs start up depending on the control source status. This bit allows OTP. 0: Rising edge 1: Level
8:5	R	RESERVED	N/A	Reserved. Do not change this register value.
4:3	R/W	ACTIVE_CTRL	2’b 00	This bit allows OTP. When FET_SRC = 0 and FET_CFG = 0: 0x0: All MOSFETs are off 0x1: CHG MOSFET and DSG MOSFET turn on 0x2: All MOSFETs are off 0x3: CHG MOSFET and DSG MOSFET turn on When FET_SRC = 0 and FET_CFG = 1: 0x0: All MOSFETs are off 0x1: DSG MOSFET turns on 0x2: CHG MOSFET turns on 0x3: CHG and DSG MOSFETs turn on
2	R	RESERVED	N/A	Reserved. Do not change this register value.
1	R/W (can lock to read-only)	FET_CFG	1’b 1	Selects the CHG and DSG MOSFET control logic. This bit allows OTP. 0: Simple mode. The internal logic automatically determines the turn-on/-off sequencing 1: Direct mode. In direct mode with pin control, GPIO1 controls the DSG MOSFET and GPIO2 controls the CHG MOSFET. When direct mode is selected and faults are enabled, the IC still uses the internal logic to turn off the MOSFETs
0	R/W (can lock to read-only)	FET_SRC	1’b 0	Defines the source that enables the MOSFETs and switches to enter normal mode. The CHG and DSG MOSFETs are controlled by the host MCU, via either register or pin. This bit allows OTP. 0: Register control 1: GPIO (GPIO1 or GPIO1 and GPIO2 depending on FET_CFG)

STB_CFG (06h)

Format: Unsigned binary

The STB_CFG command enables standby mode, the P-channel MOSFET in standby mode, and the standby current hysteresis. It also configures the standby current threshold and the refreshing interval for voltage protection reading in standby or safe mode.

Bits	Access	Bit Name	Default	Description
15:7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R/W (can lock to read-only)	STBY_PFET_EN	1’b 0	Enables the P-channel MOSFET in standby mode when ENABLE_REG_CFG is set to simple mode. To control the standby MOSFET in direct mode, use the P_FET_MANUAL setting together with P_FET_MAN_CTRL to turn the driver on and off. This bit allows OTP. 0: Disabled 1: Enabled

5:4	R/W (can lock to read-only)	STBY_MONITOR_CFG	2'b 10	Selects the interval used for voltage protection monitoring to refresh the ADC reading while in standby or safe mode. These bits allow OTP. 0x0: Voltage protection readings are refreshed every 254ms 0x1: Voltage protection readings are refreshed every 492ms 0x2: Voltage protection readings are refreshed every 968ms 0x3: Not allowed
3	R/W	STBY_HYS	1'b 0	Enables the digital hysteresis on the standby current comparator. This bit allows OTP. 0: Disabled 1: Enabled
2:1	R/W	STBY_CUR_TH	2'b 01	Sets the standby comparator current threshold. These bits allow OTP. 0x0: 250μV 0x1: 375μV 0x2: 500μV 0x3: 625μV
0	R/W (can lock to read-only)	STBY_STATE_EN	1'b 0	Enables mode. When disabled, the device cannot enter standby mode. This bit allows OTP. 0: Disabled 1: Enabled

SAFE_CFG (07h)

Format: Unsigned binary

The SAFE_CFG command enables over-current (OC), short-circuit (SC), and voltage protection monitoring in safe mode. It also configures the refreshing interval for voltage protection reading in normal mode.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3	R/W	NORM_MONITOR_CFG	1'b 0	Selects the interval used for voltage protection monitoring to refresh the ADC reading in normal mode. 0x0: Voltage protection readings are refreshed every 254ms 0x1: Voltage protection readings are refreshed every 135ms
2	R	RESERVED	N/A	Reserved. Do not change this register value.
1	R/W	SAFE_SCOC_EN	1'b 0	Enables short-circuit (SC) and over-current (OC) monitoring, even in safe mode. This function is disabled by default, since the MOSFETs are disabled in safe mode. If enabled, current consumption increases. 0: Disabled 1: Enabled
0	R/W	PROTECT_IN_SAFE_CFG	1'b 0	Enable or disable voltage protection monitoring in safe mode. This bit allows OTP. 0: Disables voltage protection monitoring in safe mode 1: Enables voltage protection monitoring in safe mode

RGL_CFG (08h)

Format: Unsigned binary

The RGL_CFG command enables 3V3 in shutdown mode and reports its status.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change this register value.

3	R	V3P3_SHOFF_STS	1’b 1	Reports the internal enable or disable control for the 3.3V regulator during shutdown mode. When enabled, the 3.3V rails stay on even in shutdown mode. 0: Off 1: On
2	R/W (can lock to read-only)	V3D3_SHDN_EN	1’b 1	Enables the 3.3V regulator during shutdown mode. This bit allows OTP. 0: Disabled 1: Enabled
1:0	R	RESERVED	N/A	Reserved. Do not change this register value.

LOAD_CHARGER_CFG (09h)

Format: Unsigned binary

The LOAD_CHARGER_CFG command enables charger and load plug-in detection, the PACKP and TOP voltage comparator, and charger detection in standby mode. It also configures the PACKP pre-charging time and reports the load/charger plug-in detection. In addition, it clears the charger/load detection status, and reports whether load/charger detection is complete.

Bits	Access	Bit Name	Default	Description
15	R/W	PACKP_CMP_EN	1’b 0	Enables the PACKP vs. TOP voltage comparator. When disabled, the comparator can still be internally enabled for other functions, such as plug-in detection. This bit allows OTP. 0: Disabled 1: Enabled
14:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10:8	R/W	T_PLUGIN_PRECHARGE_MAX	3’b 101	Selects the PACKP pre-charging expiration timer. These bits allow OTP. 0x0: 0.2s 0x1: 0.4s 0x2: 0.8s 0x3: 1.6s 0x4: 3.2s 0x5: 6.4s 0x6: 12s 0x7: 24s
7:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5	R/W (can lock to read-only)	CH_CONN_P_SBY	1’b 0	Enables charger detection in standby mode. This bit allows OTP. 0: Disabled 1: Enabled
4	R	LD_DET_DONE_STS	1’b 0	Indicates whether load plug-in detection is complete. 0: Not completed 1: Completed
3	R	CHG_DET_DONE_STS	1’b 0	Indicates whether charger plug-in detection is complete. 0: Not completed 1: Completed
2	R/W (can lock to read-only)	LD_PLUGIN_DET_EN	1’b 0	Enables load plug-in detection. If this detection is re-enabled, this bit must be written to 0 and then written to 1 again. This bit allows OTP. 0: Disabled 1: Enabled

1	R/W (can lock to read-only)	CH_PLUGIN_DET_EN	1’b 0	Enables charger plug-in detection. If this detection is re-enabled, this bit must be written to 0 and then written to 1 again. This bit allows OTP. 0: Disabled 1: Enabled
0	W	CHG_LD_CLR	1’b 0	Write to this bit to clear the detection function status bits. This bit clears itself. This command does not clear the interrupt function, so use CONN_DET_CLEAR used.

GPIO_STATUS (0Ah)

Format: Unsigned binary

The GPIO_STATUS command reports the GPIO status (high/low).

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3	R	GPIO1HV	1’b 0	Reports the GPIOHV1 pin status. 0: Low 1: High
2	R	GPIO3	1’b 0	Reports the GPIO3 pin status. 0: Low 1: High
1	R	GPIO2	1’b 0	Reports the GPIO2 pin status. 0: Low 1: High
0	R	GPIO1	1’b 0	Reports the GPIO1 pin status. 0: Low 1: High

GPIO_OUT (0Bh)

Format: Unsigned binary

The GPIO_OUT command controls the output level for GPIO.

Bits	Access	Bit Name	Default	Description
15:5	R	RESERVED	N/A	Reserved. Do not change this register value.
4	R/W	GPIO1HV_HZ	1’b 0	Sets the GPIOHV1 to Hi-Z mode. This bit allows OTP. 0: GPIOHV1 is controlled in output mode, following GPIOHV1_O 1: GPIOHV1 is in Hi-Z, and GPIOHV1_O is ignored
3	R/W	GPIO1HV_O	1’b 0	Sets the target level for GPIOHV1 (high or low). This bit is effective only when GPIOHV1 is used as a digital output (GPIO1_HV_CFG is set to output) and GPIOHV1_HZ = 0. Otherwise, GPIOHV1 is in Hi-Z. This bit allows OTP. 0: Low 1: High
2	R/W (can lock to read-only)	GPIO3_O	1’b 0	Sets the target output level for GPIO3 (high or low). This bit is effective only when GPIO3 is used as a digital output (GPIO3_IO is set to output). This bit allows OTP. 0: Low 1: High

1	R/W	GPIO2_O	1’b 0	Sets the target output level for GPIO2 (high or low). This bit is effective only when GPIO2 is used as a digital output (GPIO2_IO is set to output). This bit allows OTP. 0: Low 1: High
0	R/W	GPIO1_O	1’b 0	Sets the target output level for GPIO1 (high or low). This bit is effective only when GPIO1 is used as a digital output (GPIO1_IO is set to output). This bit allows OTP. 0: Low 1: High

GPIO_CFG (0Ch)

Format: Unsigned binary

The GPIO_CFG command enables the pull-up capability of GPIO1~3, and defines the direction and the type of input for GPIO1~3.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10	R/W (can lock to read-only)	GPIO3_PUP	1’b 0	Enables the GPIO3 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO3. This bit allows OTP. 0: Disabled 1: Enabled
9	R/W (can lock to read-only)	GPIO3_TYPE	1’b 0	Defines the type of input for GPIO3. This bit allows OTP. 0: Digital input 1: Buffered ADC input, 3.3V range
8	R/W (can lock to read-only)	GPIO3_IO	1’b 0	Defines the direction for GPIO3. This bit allows OTP. 0: Output 1: Input
7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R/W (can lock to read-only)	GPIO2_PUP	1’b 0	Enables the GPIO2 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO2. This bit allows OTP. 0: Disabled 1: Enabled
5	R/W (can lock to read-only)	GPIO2_TYPE	1’b 0	Defines the type of input for GPIO2. This bit allows OTP. 0: Digital input 1: Buffered ADC input, 3.3V range
4	R/W (can lock to read-only)	GPIO2_IO	1’b 0	Defines the direction for GPIO2. This bit allows OTP. 0: Output 1: Input
3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R/W (can lock to read-only)	GPIO1_PUP	1’b 0	Enables the GPIO1 pull-up capability. When enabled, a 20kΩ pull-up resistor is applied to GPIO1. This bit allows OTP. 0: Disabled 1: Enabled

1	R/W (can lock to read-only)	GPIO1_TYPE	1’b 0	Defines the type of input for GPIO1. This bit allows OTP. 0: Digital input 1: Buffered ADC input, 3.3V range
0	R/W (can lock to read-only)	GPIO1_IO	1’b 0	Defines the direction for GPIO1. This bit allows OTP. 0: Output 1: Input

PINS_CFG (0Dh)

Format: Unsigned binary

The PINS_CFG command defines the direction of GPIOHV1, and the pull-up voltage of GPIO1~3. It also sets the behavior of the WDT pins and xALERT pin.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10	R/W	GPIO1_HV_CFG	1’b 0	Defines the direction of GPIOHV1. This bit allows OTP. 0: Output 1: Input
9	R	RESERVED	N/A	Reserved. Do not change this register value.
8	R/W (can lock to read-only)	GPIO_LV_CFG	1’b 0	Sets the GPIO1~3 pull-up voltage. This bit allows OTP. 0: 3V3 1: REGIN
7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R/W (can lock to read-only)	WDT_RST_EN	1’b 1	Enables the WDT pin to reset the MP2790 back to its factory settings. When disabled, a WDT pulse caused by a watchdog bite does not trigger a reset. This bit allows OTP. 0: Disabled 1: Enabled
5	R/W (can lock to read-only)	WDT_RPT	1’b 1	Enables a watchdog bite event to trigger the WDT pin to toggle a high pulse. This bit allows OTP. 0: Disabled 1: Enabled
4:1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R/W (can lock to read-only)	ALERT_POL	1’b 1	Sets the polarity of the XALERT pin when the interrupt is pending. This bit allows OTP. 0: Active low. The XALERT pin goes low when an interrupt is pending 1: Active high. The XALERT pin goes high when an interrupt is pending

WDT_STATUS (0Eh)

Format: Unsigned binary

The WDT_STATUS command reports the WDT status.

Bits	Access	Bit Name	Default	Description
15:2	R	RESERVED	N/A	Reserved. Do not change this register value.

1	R	WDT_BITE	1’b 0	Indicates whether the bite timer has expired and a bite event has occurred. This event toggles the WDT pin, if WDT_RPT is set to enable. 0: False 1: True
0	R	WDT_BARKED	1’b 0	Indicates whether the bark timer has expired and a bark event has occurred. 0: False 1: True

WDT_RST (0Fh)

Format: Unsigned binary

The WDT_RST command controls the reset of the WDT.

Bits	Access	Bit Name	Default	Description
15:1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	W	WDT_RST	1’b 0	Writing 1 to this bit resets the watchdog timer counter, and clears WDT_BITE and WDT_BARKED. This is a self-clearing register.

WDT_CFG (10h)

Format: Unsigned binary

The WDT_CFG command enables WDT communication and configures the WDT bite and bark timeout.

Bits	Access	Bit Name	Default	Description
15:9	R/W (can lock to read-only)	WDT_BITE_CFG	7’b 1011110	Configures the watchdog bite timeout. The bite setting defines the delay from the bark to the bite. These bits allow OTP. LSB: 25ms Offset: 25ms Range: 25ms to 3200ms Value (ms) = Setting x 25 + 25
8:2	R/W (can lock to read-only)	WDT_BARK_CFG	7’b 0110110	Configures the watchdog bark timeout. The bark setting defines the delay from the last watchdog reset to the bark. These bits allow OTP. LSB: 25ms Offset: 25ms Range: 25ms to 3200ms Value (ms) = Setting x 25 + 25
1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R/W (can lock to read-only)	WDT_COM_CTRL	1’b 0	Enables watchdog communication. This bit allows OTP. 0: Disabled 1: Enabled

FET_STATUS (11h)

Format: Unsigned binary

The FET_STATUS reports the status of the DSG, CHG, and SBYDSG drivers and charge pump.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11	R	CP_STS	1’b 0	Indicates the charge pump’s status. 0: Off 1: On

10	R	SBYDSG_DRV_ TRANS	1’b 0	Reports whether the SBYDSG driver is changing. 0: The SBYDSG driver is settled (off or at its target voltage) 1: The SBYDSG driver is changing states
9	R	DSG_DRV_TRANS	1’b 0	Reports whether the DSG driver is changing. 0: The DSG driver is settled (off or at its target voltage) 1: The DSG driver is changing states
8	R	CHG_DRV_TRANS	1’b 0	Reports whether the CHG driver is changing. 0: The CHG driver is settled (off or at its target voltage) 1: The CHG driver is changing states
7:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3	R	FET_TIMEOUT	1’b 0	When true, an issue was detected during the latest turn-on attempt. 0: False 1: True
2	R	SBYDSG_DRV	1’b 0	Reports whether the SBYDSG driver is on or off. 0: Off 1: On
1	R	DSG_DRV	1’b 0	Reports whether the DSG driver is on or off. 0: Off 1: On
0	R	CHG_DRV	1’b 0	Reports whether the CHG driver is on or off. 0: Off 1: On

FET_CTRL (12h)

Format: Unsigned binary

The FET_CTRL turns the SBYDSG drivers on/off.

Bits	Access	Bit Name	Default	Description
15:1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R/W	P_FET_MAN_CTRL	1’b 0	Turns the SBYDSG MOSFET driver on and off. To use this bit, P_FET_MANUAL must be enabled, and the IC must be in direct mode. This bit allows OTP. 0: Off 1: On

FET_MODE (13h)

Format: Unsigned binary

The FET_MODE configures soft start for the CHG and DSG MOSFETs, and it enables manual control of the SBYDSG MOSFET.

Bits	Access	Bit Name	Default	Description
15:13	R	RESERVED	N/A	Reserved. Do not change this register value.
12	R/W (can lock to read-only)	P_FET_MANUAL	1’b 0	Enables the manual control of the P-channel MOSFET, only effective when the direct mode is enabled (FET_CFG = 1). When this bit is enabled, P_FET_MAN_CTRL can be used to control the SBYDSG driver. This bit allows OTP. 0: Disabled 1: Enabled

11	R/W (can lock to read-only)	CHG_SOFTON_OC_LIM	1’b 0	Sets the over-current (OC) threshold that is only applicable when the CHG MOSFET undergoes soft start (SS). This bit allows OTP. 0: 3.6mV 1: 4.8mV
10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R/W (can lock to read-only)	TURNON_TIMEOUT_FAULT	1’b 0	Enables the driver fault report for the turn-on timeout. This bit allows OTP. 0: Disabled 1: Enabled
8	R/W (can lock to read-only)	CHG_TURNON_TIMER	1’b 1	Sets the CHG MOSFET soft start timeout. This bit allows OTP. 0: 25ms 1: 50ms
7:5	R/W	TURNON_TIMEOUT	3’b 000	Sets the MOSFET turn-on timeout delay. Applies to both the CHG and DSG MOSFETs. This function is paused during SS. These bits allow OTP. LSB: 20ms Offset: 40ms Range: 40ms to 180ms Value (ms) = Setting x 20 + 40
4	R/W (can lock to read-only)	CHG_SOFTON_EN	1’b 1	Enables SS for the CHG MOSFET driver. This bit allows OTP. 0: Disabled 1: Enabled
3	R/W (can lock to read-only)	DSGFET_ON_RUN_SC_DET_EN	1’b 1	Enables the short-circuit detection sequence prior to the MOSFET turning on. If detection is enabled and the device detects that PACKP is shorted to ground, then a MOSFET driver fault is generated. The associated MOSFET driver bit can be manually cleared with DRIVER_FAULT_CLR. This bit allows OTP. 0: Disabled 1: Enabled
2	R	RESERVED	N/A	Reserved. Do not change this register value.
1	R/W (can lock to read-only)	DSG_SOFTON_SBY_EN	1’b 1	Enables a standby comparator check, with its dedicated threshold level selection, during soft start for the DSG MOSFET. If excessive discharge current is detected, a FET driver fault is generated. The FET driver fault can only be manually cleared. Disabling this check exposes the DSG MOSFET to damage risk during soft start in case of unexpected loading of the pack output. This bit allows OTP. 0: Disabled 1: Enabled
0	R/W (can lock to read-only)	DSG_SOFTON_EN	1’b 1	Enables soft start for the DSG MOSFET driver. This bit allows OTP. 0: Disabled 1: Enabled

FET_CFG (14h)

Format: Unsigned binary

The FET_CFG configures the driver voltages of CHG and DSG MOSFETs, and it configures soft start for the CHG and DSG MOSFETs.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:12	R/W (can lock to read-only)	FET_DRV_LVL	3'b 110	Defines VGS for the CHG and DSG MOSFETs. These bits allow OTP. 0x0: 5V with a lower CP voltage 0x1: 6V with a lower CP voltage 0x2: 7V with a lower CP voltage 0x3: 7V with a normal CP voltage 0x4: 8V with a normal CP voltage 0x5: 9V with a normal CP voltage 0x6: 10V with a normal CP voltage 0x7: 12V with a normal CP voltage
11:9	R/W (can lock to read-only)	CHG_SOFTON_PUP	3'b 100	Sets the pull-up current values during CHG MOSFET soft start. These bits allow MTP. LSB: 1μA Offset: 3μA Range: 3μA to 10μA Value (μA) = Setting + 3
8:6	R/W	RAMP_UP_SC_GF	3'b 011	Sets the deglitch filter for the standby comparator current threshold when DSG N-channel MOSFET is ramping up during SS. These bits allow OTP. 3'b000: 100μs 3'b001: 200μs 3'b010: 400μs 3'b011: 800μs 3'b100: 1200μs 3'b101: 2400μs 3'b110: 2400μs 3'b111: 2400μs
5:4	R/W	STBY_SC_CUR_TH	2'b 11	Sets the standby comparator current threshold, which acts as a protection again excessive current while the DSG N-channel MOSFET ramps up during SS. These bits allow OTP. 0x0: 250μV 0x1: 375μV 0x2: 500μV 0x3: 625μV
3	R	RESERVED	N/A	Reserved. Do not change this register value.
2:0	R/W (can lock to read-only)	DSG_SOFTON_DV	3'b 000	Sets the DSG MOSFET's turn-on slope. These bits allow MTP. 3'b000: 0.1V/ms 3'b001: 0.2V/ms 3'b010: 0.4V/ms 3'b011: 0.6V/ms 3'b100: 0.8V/ms 3'b101: 1.0V/ms 3'b110: 1.2V/ms 3'b111: 1.6V/ms

RD_INT0 (15h)

Format: Unsigned binary

The RD_INT0 command reports interrupts, such as current status changes, charger/load detection, CC, ADC, AFE status changes, fault recovery, watchdog, cell NTC charging hot/cold, cell NTC discharging hot/cold, short-circuit (SC), over-current (OC), pack over-voltage (OV), pack under-voltage (UV), cell OV, cell UV event.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	R	PACK_CURRENT_INT_STS	1'b 0	Reports whether an interrupt related to a battery pack current change has been detected. The pack current changes when switching between discharge, standby, and charge mode, which is reported via PACK_CURRENT_STATUS. 0: Not detected 1: Detected
13	R	CONN_DET_INT_STS	1'b 0	Reports whether an interrupt related to charger or load plug-in detection has been detected. 0: Not detected 1: Detected
12	R	CC_ACC_INT_STS	1'b 0	Reports whether an interrupt related a new Coulomb counting accumulation value has occurred, and updates CC_ACC_LSBS and CC_ACC_MSBS. 0: Not detected 1: Detected
11	R	VSCAN_DONE_INT_STS	1'b 0	Reports whether an interrupt related to a high-resolution voltage scan has been detected. 0: Not detected 1: Detected
10	R	AFE_MODE_CHANGE_INT_STS	1'b 0	Reports whether an interrupt related to an AFE mode change has been detected. A mode change is a change between any of the operating modes (e.g. safe, normal A/B/C state, and standby). 0: Not detected 1: Detected
9	R	RECOVERED_INT_STS	1'b 0	Reports whether an interrupt related to fault recovery event from normal C state has been detected. 0: Not detected 1: Detected
8	R	WDT_INT_STS	1'b 0	Reports whether an interrupt related to watchdog communication has been detected. A watchdog bark and a watchdog bite event can both trigger a watchdog event interruption. 0: Not detected 1: Detected
7	R	NTC_CHG_INT_STS	1'b 0	Reports whether an interrupt related to a cell NTC charging hot/cold event has been detected. This signal is generated by combining the interrupt detection for all 4 NTC channels. NTC1_VALUE, NTC2_VALUE, NTC3_VALUE, and NTC4_VALUE can be read to identify the source of the interrupt. 0: Not detected 1: Detected

6	R	NTC_DSG_INT_STS	1’b 0	Reports whether an interrupt related to a cell NTC discharging hot/cold event has been detected. This signal is generated by combining the interrupt detection for all 4 NTC channels. NTC1_VALUE, NTC2_VALUE, NTC3_VALUE, and NTC4_VALUE can be read to identify the source of the interrupt. 0: Not detected 1: Detected
5	R	SHORT_CURR_INT_STS	1’b 0	Reports whether an interrupt related to an SC event has been detected. This signal is generated by combining the interrupt detection for discharge short-circuit and charge short-circuit. Check SC_CHG_STS and SC_DCHG_STS identify the source of the interrupt. 0: Not detected 1: Detected
4	R	OVER_CURR_INT_STS	1’b 0	Reports whether an interrupt related to an OC event has been detected. This signal is generated by combining the interrupt detection for discharge OC and charge OC. Check OC1_DCHG_STS, OC2_DCHG_STS, and OC_CHG_STS to identify the source of the interrupt. 0: Not detected 1: Detected
3	R	VTOP_OV_INT_STS	1’b 0	Reports whether an OV interrupt related to the battery stack positive terminal (C10 to AGND) has been detected. 0: Not detected 1: Detected
2	R	VTOP_UV_INT_STS	1’b 0	Reports whether a UV interrupt related to the battery stack positive terminal (C10 to AGND) has been detected. 0: Not detected 1: Detected
1	R	CELL_UV_INT_STS	1’b 0	Reports whether an interrupt related to a cell under-voltage (UV) event has been detected. Check the flags located in RD_CELL_UV to identify which cell caused the interrupt. 0: Not detected 1: Detected
0	R	CELL_OV_INT_STS	1’b 0	Reports whether an interrupt related to a cell over-voltage (OV) event has been detected. Check the flags located in RD_CELL_OV to identify which cell caused the interrupt. 0: Not detected 1: Detected

RD_INT1 (16h)

Format: Unsigned binary

The RD_INT1 reports interrupts, such as driver error, pack voltage changes, balancing done, ADC self-diagnostics, scheduler errors, NTC hot PCB monitoring, a digital die temperature, cell mismatch, dead cell, open-wire detection, V_{DD} under-voltage (UV), 3V3 UV, REGIN UV, and an OTP CRC event.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change this register value.

13	R	FET_DRIVER_INT_STS	1'b 0	Reports whether an interrupt related to a MOSFET driver error has been detected. MOSFET driver errors cover the following conditions: ● MOSFET timeout ● An issue during CHG or DSG soft start, such as a SC or an OC condition 0: Not detected 1: Detected
12	R	PACKP_V_INT_STS	1'b 0	Reports whether an interrupt related to a PACKP voltage change event has been detected. 0: Not detected 1: Detected
11	R	BAL_DONE_INT_STS	1'b 0	Reports whether an interrupt related to a cell-balancing done event has been detected. 0: Not detected 1: Detected
10	R	SELF_TEST_INT_STS	1'b 0	Reports whether an interrupt related to an ADC self-diagnostic event has been detected. The SELF_TEST_STS_OV and SELF_TEST_STS_UV flags should be checked to identify the cause of the interrupt. 0: Not detected 1: Detected
9	R	FSM_ERROR_INT_STS	1'b 0	Reports whether an interrupt related to a scheduler error event has been detected. 0: Not detected 1: Detected
8	R	PCB_MNTR_HOT_INT_STS	1'b 0	Reports whether an interrupt related to the NTC hot PCB monitor has been detected. Check NTC1_PCB_MNTR_HOT_STS, NTC2_PCB_MNTR_HOT_STS, NTC3_PCB_MNTR_HOT_STS, and NTC4_PCB_MNTR_HOT_STS to identify which NTC caused the interrupt. 0: Not detected 1: Detected
7	R	DIE_TEMP_INT_STS	1'b 0	Reports whether an interrupt related to a digital die temperature event has been detected. 0: Not detected 1: Detected
6	R	CELL_MISMATCH_INT_STS	1'b 0	Reports whether an interrupt related to a cell mismatch has been detected. Flags in the RD_CELL_MSMT and CELL_MSMT_LOWER registers should be read to identify the cells triggering the event. 0: Not detected 1: Detected
5	R	CELL_DEAD_INT_STS	1'b 0	Reports whether an interrupt related to a dead cell has been detected. 0: Not detected 1: Detected

4	R	OPEN_WIRE_INT_STS	1’b 0	Reports whether an interrupt related to an open-wire event has been detected. The open wire status registers (located at the RD_OPENH and RD_OPENL addresses) must be checked to determine whether there are disconnected wires. 0: Not detected 1: Detected
3	R	VDD_INT_STS	1’b 0	Reports whether an interrupt related to a UV condition on VDD has been detected. A VDD UV event can be triggered by either ADC voltage monitoring or the VDD UV comparator. The VDD analog comparator is always enabled, so when VDD_INT_EN is enabled, it can trigger an interrupt even if VDD_EN is disabled. 0: Not detected 1: Detected
2	R	3V3_INT_STS	1’b 0	Reports whether an interrupt related to a UV condition on 3V3 has been detected. This is triggered by monitoring the 3V3 ADC or the 3.3V analog comparator. The 3.3V UV analog comparator is always enabled, so when 3V3_INT_EN is enabled, it can trigger an interrupt even if 3V3_EN is disabled. 0: Not detected 1: Detected
1	R	REGIN_INT_STS	1’b 0	Reports whether an interrupt related to a UV condition on REGIN has been detected. 0: Not detected 1: Detected
0	R	OTP_CRC_EVENT_INT_STS	1’b 0	Reports whether an interrupt related to a one-time-programmable (OTP) memory CRC fault has been detected. When enabled, this interrupt can be triggered by the following conditions: the OTP CRC calculation fails while restoring the OTP. OTP CRC is manually triggered using OTP_CRC_DO. In this scenario, an interrupt event is generated when a CRC check is completed (for either passing or failing). 0: Not detected 1: Detected

INT0_CLR (17h)

Format: Unsigned binary

The INT0_CLR command clears the interrupts, such as pack current change, charger/load connection, CC done, ADC done, AFE mode change, fault recovery, watchdog, cell NTC charging hot/cold, cell NTC discharging hot/cold, short-circuit, over-current, pack over-voltage (OV), pack under-voltage (UV), cell OV, cell UV event.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	W	PACK_CURRENT_INT_CLEAR	1’b 0	Write 1 to this bit to clear a battery pack current change interrupt. This is a self-clearing register.
13	W	CONN_DET_INT_CLEAR	1’b 0	Write 1 to this bit to clear a charger/load connection interrupt. This is a self-clearing register.
12	W	CC_ACC_STS_INT_CLEAR	1’b 0	Write 1 to this bit to clear a CC completed interrupt. This is a self-clearing register.
11	W	VSCAN_DONE_INT_CLEAR	1’b 0	Write 1 to this bit to clear a completed high-resolution voltage scan interrupt. This is a self-clearing register.

10	W	AFE_MODE_ CHANGE_INT_ CLEAR	1’b 0	Write 1 to this bit to clear an AFE mode change interrupt. This is a self-clearing register.
9	W	RECOVERED_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a fault recovery interrupt. This is a self-clearing register.
8	W	WDT_INT_CLEAR	1’b 0	Write 1 to this bit to clear a watchdog event interrupt. This is a self-clearing register.
7	W	NTC_CHG_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a cell NTC charging hot/cold monitor interrupt. This is a self-clearing register.
6	W	NTC_DSG_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a cell NTC discharging hot/cold monitor interrupt. This is a self-clearing register.
5	W	SHORT_CURR_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a short-circuit interrupt. This is a self-clearing register.
4	W	OVER_CURR_INT_ CLEAR	1’b 0	Write 1 to this bit to clear an OC interrupt. This is a self-clearing register.
3	W	VTOP_OV_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a battery pack OV interrupt. This is a self-clearing register.
2	W	VTOP_UV_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a battery pack UV interrupt. This is a self-clearing register.
1	W	CELL_UV_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a cell UV interrupt. This is a self-clearing register.
0	W	CELL_OV_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a cell OV interrupt. This is a self-clearing register.

INT1_CLR (18h)

Format: Unsigned binary

The INT1_ CLR command clears the interrupts, such as driver error, pack voltage change, balancing done, ADC self-diagnostic, scheduler error, NTC hot PCB monitor, cell mismatch, dead cell, OW detection, VDD UV, 3V3 UV, REGIN UV, and OTP CRC events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change this register value.
13	W	FET_DRIVER_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a MOSFET driver event interruption. This is a self-clearing register.
12	W	PACKP_V_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a PACKP voltage change interruption. This is a self-clearing register.
11	W	BAL_DONE_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a balancing complete interruption. This is a self-clearing register.
10	W	SELF_TEST_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a self-diagnostic interruption. This is a self-clearing register.
9	W	FSM_ERROR_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a schedule error interruption. This is a self-clearing register.
8	W	PCB_MNTR_TEMP_ INT_CLEAR	1’b 0	Write 1 to this bit to clear an NTC hot PCB monitor interruption. This is a self-clearing register.
7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	W	CELL_MISMATCH_ INT_CLEAR	1’b 0	Write 1 to this bit to clear a mismatched cell interruption. This is a self-clearing register.
5	W	CELL_DEAD_INT_ CLEAR	1’b 0	Write 1 to this bit to clear a dead cell interruption. This is a self-clearing register.
4	W	OPEN_WIRE_INT_ CLEAR	1’b 0	Write 1 to this bit to clear an open wire interruption. This is a self-clearing register.

3	W	VDD_INT_CLEAR	1’b 0	Write 1 to this bit to clear a VDD UV interruption. This is a self-clearing register.
2	W	3V3_INT_CLEAR	1’b 0	Write 1 to this bit to clear a 3V3 UV interruption. This is a self-clearing register.
1	W	REGIN_INT_CLEAR	1’b 0	Write 1 to this bit to clear a REGIN UV interruption. This is a self-clearing register.
0	W	OTP_CRC_EVENT_ INT_CLEAR	1’b 0	Write 1 to this bit to clear an OTP CRC interruption. This is a self-clearing register.

INT0_EN (19h)

Format: Unsigned binary

The INT0_EN command enables the interrupts, such as interrupt reports to xALERT, pack current direction changes, charger/load connection, Coulomb counting accumulation, voltage ADC scan completion, AFE mode change, fault recovery, watchdog communication, cell NTC charging/discharging hot/cold monitoring, short-circuit (SC), over-current (OC), pack over-voltage (OV), pack under-voltage (UV), cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	R/W (can lock to read-only)	INT_ALERT_CTRL	1’b 1	Enables interrupt reporting to the xALERT pin. This bit allows OTP. 0: Disabled 1: Enabled
14	R/W	PACK_CURRENT_ INT_EN	1’b 0	Enables interrupt reporting for battery pack current direction changes. 0: Disabled 1: Enabled
13	R/W	CONN_DET_INT_EN	1’b 0	Enables interrupt reporting for charger/load connection. 0: Disabled 1: Enabled
12	R/W	CC_ACC_INT_EN	1’b 0	Enables interrupt reporting for Coulomb counting accumulation. 0: Disabled 1: Enabled
11	R/W	VSCAN_DONE_INT_ EN	1’b 0	Enables interrupt reporting for high-resolution voltage ADC scan completion. 0: Disabled 1: Enabled
10	R/W	AFE_MODE_ CHANGE_INT_EN	1’b 0	Enables interrupt reporting for an AFE mode change. 0: Disabled 1: Enabled
9	R/W	RECOVERED_INT_ EN	1’b 0	Enables interrupt reporting for fault recovery. 0: Disabled 1: Enabled
8	R/W	WDT_INT_EN	1’b 0	Enables interrupt reporting for watchdog communication. 0: Disabled 1: Enabled
7	R/W	NTC_CHG_INT_EN	1’b 0	Enables interrupt reporting for cell NTC charging hot/cold monitoring conditions. 0: Disabled 1: Enabled

6	R/W	NTC_DSG_INT_EN	1’b 0	Enables interrupt reporting for cell NTC discharging hot/cold monitoring conditions. 0: Disabled 1: Enabled
5	R/W	SHORT_CURR_INT_EN	1’b 0	Enables interrupt reporting for short-circuit conditions. Note that there are individual enable bits: SC_CHG_INT_EN and SC_DCHG_INT_EN. SHORT_CURR_INT_EN acts as a master enabler, so it must be enabled for the charge and discharge interruption to work. 0: Disabled 1: Enabled
4	R/W	OVER_CURR_INT_EN	1’b 0	Enables interrupt reporting for OC conditions. Note that there are individual enable bits: OC_CHG_INT_EN, OC2_DCHG_INT_EN, and OC1_DCHG_INT_EN. OVER_CURR_INT_EN acts as a master enabler, so it must be enabled for the charger and discharge interrupt to work. 0: Disabled 1: Enabled
3	R/W	VTOP_OV_INT_EN	1’b 0	Enables interrupt reporting for battery pack OV conditions. 0: Disabled 1: Enabled
2	R/W	VTOP_UV_INT_EN	1’b 0	Enables interrupt reporting for battery pack UV conditions. 0: Disabled 1: Enabled
1	R/W	CELL_UV_INT_EN	1’b 0	Enables interrupt reporting for cell UV conditions. 0: Disabled 1: Enabled
0	R/W	CELL_OV_INT_EN	1’b 0	Enables interrupt reporting for cell OV conditions. 0: Disabled 1: Enabled

INT1_EN (1Ah)

Format: Unsigned binary

The INT1_EN command enables the interrupts, such as MOSFET driver issues, PACKP voltage changes, completed cell-balancing, ADC self-diagnostics for over-voltage (OV)/under-voltage (UV) conditions, scheduled errors, NTC hot PCB, die over-temperature, cell mismatch, dead cell, open-wire detection, V_{DD} UV, 3V3 UV, REGIN UV, and an OTP CRC events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change this register value.
13	R/W	FET_DRIVER_INT_EN	1’b 0	Enables interrupt reporting for MOSFET driver issues. 0: Disabled 1: Enabled
12	R/W	PACKP_V_INT_EN	1’b 0	Enables interrupt reporting for PACKP voltage changes. 0: Disabled 1: Enabled
11	R/W	BAL_DONE_INT_EN	1’b 0	Enables interrupt reporting for completed cell-balancing. 0: Disabled 1: Enabled

10	R/W	SELF_TEST_INT_EN	1’b 0	Enables interrupt reporting for an ADC self-diagnostic OV/UV conditions. 0: Disabled 1: Enabled
9	R/W	FSM_ERROR_INT_EN	1’b 0	Enables interrupt reporting for a scheduled error. 0: Disabled 1: Enabled
8	R/W	PCB_MNTR_TEMP_INT_EN	1’b 0	Enables interrupt reporting for an NTC hot PCB condition. 0: Disabled 1: Enabled
7	R/W	DIE_TEMP_INT_EN	1’b 0	Enables interrupt reporting for a die over-temperature (OT) event. 0: Disabled 1: Enabled
6	R/W	CELL_MISMATCH_INT_EN	1’b 0	Enables interrupt reporting for a cell mismatch condition. 0: Disabled 1: Enabled
5	R/W	CELL_DEAD_INT_EN	1’b 0	Enables interrupt reporting for a dead cell condition. 0: Disabled 1: Enabled
4	R/W	OPEN_WIRE_INT_EN	1’b 0	Enables interrupt reporting for completed open-wire detection. 0: Disabled 1: Enabled
3	R/W	VDD_INT_EN	1’b 0	Enables interrupt reporting for a V_{DD} UV event. 0: Disabled 1: Enabled
2	R/W	3V3_INT_EN	1’b 0	Enables interrupt reporting for a 3V3 UV event. 0: Disabled 1: Enabled
1	R/W	REGIN_INT_EN	1’b 0	Enables interrupt reporting for a REGIN UV event. 0: Disabled 1: Enabled
0	R/W	OTP_CRC_EVENT_INT_EN	1’b 1	Enables interrupt reporting for an OTP CRC event. 0: Disabled 1: Enabled

INT_TYPE0 (1Bh)

Format: Unsigned binary

The INT_TYPE0 command controls the triggering logic for the interrupts, such as cell NTC charging hot/cold, cell NTC discharging hot/cold interruption, pack over-voltage (OV), and pack under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change this register value.

7:6	R/W	NTC_CHG_INT_TYPE	2'b 00	Controls the triggering logic for a cell NTC charging hot/cold interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
5:4	R/W	NTC_DSG_INT_TYPE	2'b 00	Controls the triggering logic for a cell NTC discharging hot/cold interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
3:2	R/W	VTOP_OV_INT_TYPE	2'b 00	Controls the triggering logic for battery pack OV interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
1:0	R/W	VTOP_UV_INT_TYPE	2'b 00	Controls the triggering logic for battery pack UV interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

INT_TYPE1 (1Ch)

Format: Unsigned binary

The INT_TYPE1 command controls the triggering logic for the interrupts, such as V_{DD} under-voltage (UV), 3V3 UV, and REGIN UV interruption.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change this register value.
13:12	R/W	VDD_INT_TYPE	2'b 00	Controls the triggering logic for V_{DD} UV interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

11:10	R/W	3V3_INT_TYPE	2’b 00	Controls the triggering logic for 3V3 UV interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
9:8	R/W	REGIN_INT_TYPE	2’b 00	Controls the triggering logic for REGIN UV interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
7:0	R	RESERVED	N/A	Reserved. Do not change this register value.

INT_TYPE2 (1Dh)

Format: Unsigned binary

The INT_TYPE2 command controls the triggering logic for the interrupts, such as self-diagnostic, NTC hot PCB monitor, die temperature, cell mismatch, and dead cell events.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11:10	R/W	SELF_TEST_INT_ TYPE	2’b 00	Controls the triggering logic for a self-diagnostic interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
9:8	R	RESERVED	N/A	Reserved. Do not change this register value.
7:6	R/W	PCB_MNTR_TEMP_ INT_TYPE	2’b 00	Controls the triggering logic for an NTC hot PCB monitor interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
5:4	R/W	DIE_TEMP_INT_ TYPE	2’b 00	Controls the triggering logic for a die temperature interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

3:2	R/W	CELL_MISMATCH_INT_TYPE	2'b 00	Controls the triggering logic for a mismatched cell interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
1:0	R/W	CELL_DEAD_INT_TYPE	2'b 00	Controls the triggering logic for a dead cell interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal

MASK_INT0 (1Eh)

Format: Unsigned binary

The MASK_INT0 command masks the triggering interrupts, such as cell NTC charging/discharging hot/cold, short-circuit (SC), over-current (OC), TOP over-voltage (OV), TOP under-voltage (UV), cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change this register value.
7	R/W	NTC_CELL_CHG_MASK	1'b 0	Enables clearing the cell NTC charging hot/cold interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
6	R/W	NTC_CELL_DSG_MASK	1'b 0	Enables clearing the cell NTC discharging hot/cold interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
5	R/W	SC_MASK	1'b 0	Enables clearing the short-circuit interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
4	R/W	OVER_CURR_MASK	1'b 0	Enables clearing the OC interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
3	R/W	VTOP_OV_MASK	1'b 0	Enables clearing the TOP OV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled

2	R/W	VTOP_UV_MASK	1’b 0	Enables clearing the TOP UV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
1	R/W	CELL_UV_MASK	1’b 0	Enables clearing the cell UV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
0	R/W	CELL_OV_MASK	1’b 0	Enables clearing the cell OV interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled

MASK_INT1 (1Fh)

Format: Unsigned binary

The MASK_INT1 command masks the triggering interrupts, such as NTC hot PCB monitor, die hot temperature, cell mismatch, V_{DD} under-voltage (UV), 3V3 UV, REGIN UV, and self-test events.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change this register value.
8	R/W	PCB_MNTR_HOT_ MASK	1’b 0	Enables clearing the NTC hot PCB monitor interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
7	R/W	DIE_TEMP_DIG_ MASK	1’b 0	Enables clearing the die temperature interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
6	R/W	CELL_MSMT_MASK	1’b 0	Enables clearing the mismatched cell interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
5:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3	R/W	VDD_MASK	1’b 0	Enables clearing the VDD interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
2	R/W	3V3_MASK	1’b 0	Enables clearing the 3V3 interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled

1	R/W	REGIN_MASK	1’b 0	Enables clearing the REGIN interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled
0	R/W	SELF_TEST_MASK	1’b 0	Enables clearing the self-test interrupt flag and pulls the interrupt pin low, unless there are other interrupts pending. When disabled, the interrupt process can set the interrupt flag again. 0: Disabled 1: Enabled

OC_STATUS (20h)

Format: Unsigned binary

The OC_STATUS command reports both the real-time and latched status of charge over-current (OC), discharge OC1, and discharge OC2 events.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10	R	OC_CHG_RT_STS	1’b 0	Reports in real time whether a charge OC limit is detected. 0: Not detected 1: Detected
9	R	OC2_DCHG_RT_STS	1’b 0	Reports in real time whether a discharge OC limit 2 is detected. 0: Not detected 1: Detected
8	R	OC1_DCHG_RT_STS	1’b 0	Reports in real time whether a discharge OC limit 1 is detected. 0: Not detected 1: Detected
7:3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R	OC_CHG_STS	1’b 0	Indicates the latched charge OC limit interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. The type is determined by OC_CHG_INT_TYPE. This status bit can be cleared with OVER_CURR_INT_CLEAR. 0: Not detected 1: Detected

1	R	OC2_DCHG_STS	1’b 0	Indicates the latched discharge OC limit 2 interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. The type is determined by OC_DCHG_INT_TYPE, with the type selection being common for both limit 1 and limit 2 interrupts. This status bit can be cleared with OVER_CURR_INT_CLEAR. 0: Not detected 1: Detected
0	R	OC1_DCHG_STS	1’b 0	Indicates the latched discharge OC limit 1 interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. The type is determined by OC_DCHG_INT_TYPE, with the type selection being common for both limit 1 and limit 2 interrupts. This status bit can be cleared with OVER_CURR_INT_CLEAR. 0: Not detected 1: Detected

OCFT_CTRL (23h)

Format: Unsigned binary

The OCFT_CTRL command controls the triggering logic for the interrupt of charge over-current (OC), discharge OC1, and discharge OC2 events. It also enables the interrupts, faults, and monitoring for charge OC, discharge OC1, discharge OC2 events.

Bits	Access	Bit Name	Default	Description
15:14	R/W	OC_CHG_INT_TYPE	2’b 00	Controls the triggering logic for a charge OC interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
13:12	R/W	OC_DCHG_INT_ TYPE	2’b 00	Controls the triggering logic for a discharge OC interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
11:9	R	RESERVED	N/A	Reserved. Do not change this register value.

8	R/W (can lock to read-only)	OC_CHG_FAULT_EN	1’b 1	Enables a charge OC event to turn off the CHG driver. When enabled, a CHG OC event turns off the CHG MOSFET. This bit allows OTP. 0: Disabled 1: Enabled
7	R/W (can lock to read-only)	OC2_DCHG_FAULT_EN	1’b 1	Enables a discharge OC2 event to turn off the DSG driver. When enabled, a DSG OC2 event turns off the DSG MOSFET. This bit allows OTP. 0: Disabled 1: Enabled
6	R/W (can lock to read-only)	OC1_DCHG_FAULT_EN	1’b 1	Enables a discharge OC1 event to turn off the DSG driver. When enabled, a DSG OC1 event turns off the DSG MOSFET. This bit allows OTP. 0: Disabled 1: Enabled
5	R/W	OC_CHG_INT_EN	1’b 0	Enables bit-level control for a charge OC interruption. OVER_CURR_INT_EN must be enabled for this bit to be effective. 0: Disabled 1: Enabled
4	R/W	OC2_DCHG_INT_EN	1’b 0	Enables bit-level control for a discharge OC2 interruption. OVER_CURR_INT_EN must be enabled for this bit to be effective. 0: Disabled 1: Enabled
3	R/W	OC1_DCHG_INT_EN	1’b 0	Enables bit-level control for a discharge OC1 interruption. OVER_CURR_INT_EN must be enabled for this bit to be effective. 0: Disabled 1: Enabled
2	R/W (can lock to read-only)	OC_CHG_EN_CTRL	1’b 1	Enables charge OC limit monitoring. When disabled, a charge OC limit event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled. This bit allows MTP. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	OC2_DCHG_EN_CTRL	1’b 1	Enables discharge OC limit 2 monitoring. When disabled, a discharge OC2 event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled. This bit allows MTP. 0: Disabled 1: Enabled
0	R/W (can lock to read-only)	OC1_DCHG_EN_CTRL	1’b 1	Enables discharge OC limit 1 monitoring. When disabled, a discharge OC1 event does not trigger a fault or interrupt, regardless of whether the fault and interrupt bits are enabled. This bit allows MTP. 0: Disabled 1: Enabled

DSGOC_LIM (24h)

Format: Unsigned binary

The DSGOC_LIM command configures the threshold and threshold range for discharge over-current (OC1) and discharge OC2 events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change this register value.
13	R/W (can lock to read-only)	OC2_DCHG_RNG	1'b 1	Selects the range and LSB for the discharge OC level 2 (OC2) threshold. This bit allows MTP. 0: 2.5mV/LSB, 80mV FSR 1: 7.5mV/LSB, 240mV FSR
12:8	R/W (can lock to read-only)	OC2_DCHG_LIM	5'b 01001	Sets the discharge OC2 threshold. These bits allow MTP. With a 1x range (OC2_DCHG_RNG = 0): LSB: 2.5mV Offset: 2.5mV Range: 2.5mV to 80mV Value (mV) = Setting x 2.5 + 2.5 With a 3x range (OC2_DCHG_RNG = 1): LSB: 7.5mV Offset: 7.5mV Range: 7.5mV to 240mV Value (mV) = Setting x 7.5 + 7.5
7:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5	R/W (can lock to read-only)	OC1_DCHG_RNG	1'b 0	Selects the range and LSB for the discharge OC level 1 (OC1) threshold. This bit allows MTP. 0: 2.5mV/LSB, 80mV FSR 1: 7.5mV/LSB, 240mV FSR
4:0	R/W (can lock to read-only)	OC1_DCHG_LIM	5'b 10000	Sets the discharge OC1 threshold. These bits allow MTP. With a 1x range (OC1_DCHG_RNG = 0): LSB: 2.5mV Offset: 2.5mV Range: 2.5mV to 80mV Value (mV) = Setting x 2.5 + 2.5 With a 3x range (OC1_DCHG_RNG = 1): LSB: 7.5mV Offset: 7.5mV Range: 7.5mV to 240mV Value (mV) = Setting x 7.5 + 7.5

DSGOC_DEG (25h)

Format: Unsigned binary

The DSGOC_DEG command configures the deglitch and deglitch range for discharge over-current (OC1) and discharge OC2 events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	R/W (can lock to read-only)	OC2_DCHG_DGL_RNG	1'b 0	Sets the discharge OC2 deglitch bit weight and selects the range for OC2_DCHG_DGL. This bit allows MTP. 0: 5ms/LSB, 315ms FSR 1: 40ms/LSB, 2520ms FSR

13:8	R/W (can lock to read-only)	OC2_DCHG_DGL	6’b 000100	Sets the discharge OC2 deglitch value. When OC2_DCHG_DGL = 0x00, there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 60µs. These bits allow MTP. When OC2_DCHG_DGL_RNG = 0x0: LSB: 5ms Range: 0ms to 315ms Value (ms) = Setting x 5 When OC2_DCHG_DGL_RNG = 0x1: LSB: 40ms Range: 0ms to 2520ms Value (ms) = Setting x 40
7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R/W (can lock to read-only)	OC1_DCHG_DGL_RNG	1’b 0	Sets the discharge OC1 deglitch bit weight and selects the range for OC1_DCHG_DGL. This bit allows MTP. 0: 5ms/LSB, 315ms FSR 1: 40ms/LSB, 2520ms FSR
5:0	R/W (can lock to read-only)	OC1_DCHG_DGL	6’b 010100	Sets the discharge OC1 deglitch value. When OC1_DCHG_DGL = 0x00, there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 60µs. These bits allow MTP. When OC1_DCHG_DGL_RNG = 0x0: LSB: 5ms Range: 0ms to 315ms Value (ms) = Setting x 5 When OC1_DCHG_DGL_RNG = 0x1: LSB: 40ms Range: 0ms to 2520ms Value (ms) = Setting x 40

CHGOC_DEG (26h)

Format: Unsigned binary

The CHGOC_DEG command configures the deglitch, deglitch range, threshold, and threshold range for charge over-current (OC) events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	R/W (can lock to read-only)	OC_CHG_DGL_RNG	1’b 0	Sets the charge OC deglitch bit weight and selects the range for OC_CHG_DG. These bits allow MTP. 0: 5ms/LSB, 315ms FSR 1: 40ms/LSB, 2520ms FSR
13:8	R/W (can lock to read-only)	OC_CHG_DG	6’b 000100	Sets the charge OC deglitch value. When OC_CHG_DG = 0x00, there is no deglitch, regardless of the LSB. This means an OC event is flagged as soon as it is detected. The response time is about 60µs. These bits allow MTP. When OC_CHG_DGL_RNG = 0x0: LSB: 5ms Range: 0ms to 315ms Value (ms) = Setting x 5 When OC2_DCHG_DGL_RNG = 0x1: LSB: 40ms Range: 0ms to 2520ms Value (ms) = Setting x 40

7:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5	R/W (can lock to read-only)	OC_CHG_RNG	1’b 0	Selects the range and LSB for the charge OC threshold (OC_CHG_LIM). These bits allow MTP. 0: 1.6mV/LSB, 51.2mV FSR 1: 4.8mV/LSB, 153.6mV FSR
4:0	R/W (can lock to read-only)	OC_CHG_LIM	5’b 10000	Sets the charge OC threshold. These bits allow MTP. With a 1x range (OC_CHG_RNG = 0): LSB: 1.6mV Offset: 1.6mV Range: 1.6mV to 51.2mV Value (mV) = Setting x 1.6 + 1.6 With a 3x range (OC_CHG_RNG = 1): LSB: 4.8mV Offset: 4.8mV Range: 4.8mV to 153.6mV Value (mV) = Setting x 4.8 + 4.8

SC_STATUS (27h)

Format: Unsigned binary

The SC_STATUS command reports both the real-time and latched status of charge short-circuit (SC) and discharge SC events.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R	SC_CHG_RT_STS	1’b 0	Reports whether a charge SC event has been detected in real time. 0: Not detected 1: Detected
8	R	SC_DCHG_RT_STS	1’b 0	Reports whether a discharge SC event has been detected in real time. 0: Not detected 1: Detected
7:2	R	RESERVED	N/A	Reserved. Do not change this register value.
1	R	SC_CHG_STS	1’b 0	Reports whether a latched charge SC event has been detected. This status bit can be cleared with SHORT_CURR_INT_CLEAR. 0: Not detected 1: Detected
0	R	SC_DCHG_STS	1’b 0	Reports whether a latched discharge SC event has been detected. The latched value depends on the interrupt type (e.g. rising, falling, or rising and falling), which is determined by SC_DCHG_INT_TYPE. For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. This status bit can be cleared with SHORT_CURR_INT_CLEAR. 0: Not detected 1: Detected

SCFT_CTRL (2Ah)

Format: Unsigned binary

The SCFT_CTRL command enables the fault protection, interrupt, and monitoring of charge short-circuit (SC) and discharge SC events.

Bits	Access	Bit Name	Default	Description
15:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5	R/W (can lock to read-only)	SC_CHG_FAULT_EN	1’b 1	Enables a charge SC event to provide a fault protection by turning off the CHG MOSFET. For this bit to be effective, SC_CHG_EN_CTRL must be enabled. This bit allows OTP. 0: Disabled 1: Enabled
4	R/W (can lock to read-only)	SC_DCHG_FAULT_EN	1’b 1	Enables a discharge SC event to provide a fault protection by turning off the CHG MOSFET. For this bit to be effective, SC_DCHG_EN_CTRL must be enabled. This bit allows OTP. 0: Disabled 1: Enabled
3	R/W	SC_CHG_INT_EN	1’b 0	Enables the interrupt for a charge SC current. For this bit to be effective, SC_CHG_EN_CTRL must be enabled. 0: Disabled 1: Enabled
2	R/W	SC_DCHG_INT_EN	1’b 0	Enables the interrupt for a discharge SC current. For this bit to be effective, SC_DCHG_EN_CTRL must be enabled. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	SC_CHG_EN_CTRL	1’b 1	Enables charge SC monitoring. When disabled, this fault does not trigger an interrupt or a fault, regardless of whether those bits are enabled. This bit allows MTP. 0: Disabled 1: Enabled
0	R/W (can lock to read-only)	SC_DCHG_EN_CTRL	1’b 1	Enables discharge SC monitoring. When disabled, this fault does not trigger an interrupt or a fault, regardless of whether those bits are enabled. This bit allows MTP. 0: Disabled 1: Enabled

DSGSC_CFG (2Bh)

Format: Unsigned binary

The DSGSC_CFG command configures the deglitch, threshold, and threshold range for discharge short-circuit (SC) events.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:8	R/W (can lock to read-only)	SC_DCHG_DG	7’b 0000001	Configures the discharge SC deglitch time. When SC_DCHG_DG = 0x00, there is no deglitch, so a short-circuit event is flagged as soon as it is detected. The response time is about 60µs. These bits allow MTP. LSB: 0.2ms Range: 0ms to 25.4ms Value (ms) = Setting x 0.2
7:6	R	RESERVED	N/A	Reserved. Do not change this register value.

5	R/W (can lock to read-only)	SC_DCHG_RNG	1’b 0	Selects the range and LSB for the discharge SC threshold (SC_DCHG_LIM). This bit allows MTP. 0: 5.5mV/LSB, 176mV FSR 1: 16.5mV/LSB, 528mV FSR
4:0	R/W (can lock to read-only)	SC_DCHG_LIM	5’b 10001	Configures the SC discharge threshold. These bits allow MTP. With a 1x range (SC_DCHG_RNG = 0): LSB: 5.5mV Offset: 5.5mV Range: 5.5mV to 176mV Value (mV) = Setting x 5.5 + 5.5 With a 3x range (SC_DCHG_RNG = 1): LSB: 16.5mV Offset: 16.5mV Range: 16.5mV to 528mV Value (mV) = Setting x 16.5 + 16.5

CHGSC_CFG (2Ch)

Format: Unsigned binary

The CHGSC_CFG command configures the deglitch, threshold, and threshold range for charge short-circuit (SC).

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:8	R/W (can lock to read-only)	SC_CHG_DG	7’b 0001000	Configures the charge short-circuit deglitch time. When SC_CHG_DG = 0x00, there is no deglitch, so a short-circuit event is flagged as soon as it is detected. The response time is about 60µs. These bits allow MTP. LSB: 0.2ms Range: 0ms to 25.4ms Value (ms) = Setting x 0.2
7:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5	R/W (can lock to read-only)	SC_CHG_RNG	1’b 0	Selects the range and LSB for the charge short-circuit threshold (SC_CHG_LIM). This bit allows MTP. 0: 2.5mV/LSB, 80mV FSR 1: 7.5mV/LSB, 240mV FSR
4:0	R/W (can lock to read-only)	SC_CHG_LIM	5’b 10001	Configures the charge short-circuit threshold. These bits allow MTP. With a 1x range (SC_CHG_RNG = 0): LSB: 2.5mV Offset: 2.5mV Range: 2.5mV to 80mV Value (mV) = Setting x 2.5 + 2.5 With a 3x range (SC_CHG_RNG = 1): LSB: 7.5mV Offset: 7.5mV Range: 7.5mV to 240mV Value (mV) = Setting x 7.5 + 7.5

RD_CELL_UV (2Dh)

Format: Unsigned binary

The RD_CELL_UV command reports whether under-voltage (UV) conditions have been detected on cell 1~10.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R	CELL_10_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 10. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
8	R	CELL_9_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 9. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
7	R	CELL_8_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 8. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
6	R	CELL_7_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 7. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
5	R	CELL_6_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 6. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
4	R	CELL_5_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 5. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
3	R	CELL_4_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 4. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
2	R	CELL_3_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 3. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell
1	R	CELL_2_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 2. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell

0	R	CELL_1_UV_STS	1'b 0	Reports whether a UV condition has been detected on cell 1. If CELL_UV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_UV_STS_SEL = 1, this bit indicates the real-time status. 0: No UV condition has been detected on this cell 1: A UV condition has been detected on this cell

RD_CELL_OV (2Eh)

Format: Unsigned binary

The RD_CELL_OV command reports whether over-voltage (OV) conditions have been detected on cell 1~10.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R	CELL_10_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 10. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
8	R	CELL_9_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 9. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
7	R	CELL_8_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 8. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
6	R	CELL_7_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 7. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
5	R	CELL_6_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 6. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
4	R	CELL_5_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 5. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
3	R	CELL_4_OV_STS	1'b 0	Reports whether an OV condition has been detected on cell 4. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell

2	R	CELL_3_OV_STS	1’b 0	Reports whether an OV condition has been detected on cell 3. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
1	R	CELL_2_OV_STS	1’b 0	Reports whether an OV condition has been detected on cell 2. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell
0	R	CELL_1_OV_STS	1’b 0	Reports whether an OV condition has been detected on cell 1. Send an interrupt OV clear to clear this bit. If CELL_OV_STS_SEL = 0, this bit indicates the interrupt status; if CELL_OV_STS_SEL = 1, this bit indicates the real-time status. 0: No OV condition has been detected on this cell 1: An OV condition has been detected on this cell

RD_CELL_MSMT (2Fh)

Format: Unsigned binary

The RD_CELL_MSMT command reports cell 1~10 mismatch (MSMT) interrupt status.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R	CELL_10_MSMT_STS	1’b 0	Reports cell 10’s mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
8	R	CELL_9_MSMT_STS	1’b 0	Reports cell 9’s mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
7	R	CELL_8_MSMT_STS	1’b 0	Reports cell 8’s mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
6	R	CELL_7_MSMT_STS	1’b 0	Reports cell 7’s mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
5	R	CELL_6_MSMT_STS	1’b 0	Reports cell 6’s mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
4	R	CELL_5_MSMT_STS	1’b 0	Reports cell 5’s mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
3	R	CELL_4_MSMT_STS	1’b 0	Reports cell 4’s mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected

2	R	CELL_3_MSMT_STS	1'b 0	Reports cell 3's mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
1	R	CELL_2_MSMT_STS	1'b 0	Reports cell 2's mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected
0	R	CELL_1_MSMT_STS	1'b 0	Reports cell 1's mismatch interrupt status. Clear a mismatch with CELL_MISMATCH_INT_CLEAR. 0: No mismatch has been detected 1: A mismatch has been detected

RD_CELL_DEAD (30h)

Format: Unsigned binary

The RD_CELL_DEAD command reports whether dead cell conditions have been detected on cell 1~10.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R	CELL_10_DEAD_STS	1'b 0	Reports cell 10's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
8	R	CELL_9_DEAD_STS	1'b 0	Reports cell 9's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
7	R	CELL_8_DEAD_STS	1'b 0	Reports cell 8's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
6	R	CELL_7_DEAD_STS	1'b 0	Reports cell 7's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
5	R	CELL_6_DEAD_STS	1'b 0	Reports cell 6's dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead

4	R	CELL_5_DEAD_STS	1’b 0	Reports cell 5’s dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
3	R	CELL_4_DEAD_STS	1’b 0	Reports cell 4’s dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
2	R	CELL_3_DEAD_STS	1’b 0	Reports cell 3’s dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
1	R	CELL_2_DEAD_STS	1’b 0	Reports cell 2’s dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead
0	R	CELL_1_DEAD_STS	1’b 0	Reports cell 1’s dead interrupt status. If CELL_DEAD_STS_SEL = 0, this bit indicates the interrupt status; if CELL_DEAD_STS_SEL = 1, this bit indicates the real-time status. 0: This cell is not dead 1: This cell is dead

CELL_MSMT_STS (33h)

Format: Unsigned binary

The CELL_MSMT_STS command reports the real-time cell mismatch status, the cell with the lowest voltage, and the voltage difference between the cell with the lowest voltage and the cell with the highest voltage.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	R	CELL_MSMT_RT_ STS	1’b 0	Reports the real-time cell mismatch status. 0: There is no mismatch 1: A mismatch has been detected
13:10	R	CELL_MSMT_ LOWER	4’b 0000	Reports the cell with the lowest voltage. If the interrupt is disabled, this bit indicates the real-time status; otherwise, this bit is latched at the interrupt and returns to the real-time status after being cleared. 0x0: Cell 1 0x1: Cell 2 ... 0x9: Cell 10

9:0	R	CELL_MSMT_DELTA	10’b 0000000000	Reports the voltage difference between the cell with the lowest voltage and the cell with the highest voltage. If the interrupt is disabled, this bit indicates the real-time status; otherwise, this bit is latched at the interrupt and returns to the real-time status after being cleared. LSB: 4.8828mV Range: 0mV to 4995.1044mV Value (mV) = Setting x 4.8828

PACKFT_CTRL (34h)

Format: Unsigned binary

The PACKFT_CTRL command enables the monitoring and fault protection of cell mismatch (MSMT), cell dead, and VTOP over-voltage (OV)/under-voltage (UV) events. It also reports the real-time or latched interrupt dead cell status and whether a dead cell event has been detected.

Bits	Access	Bit Name	Default	Description
15	W	CELL_DEAD_DET_CLEAR	1’b 0	Write this bit to 1 to clear the dead cell status. This is a self-clearing bit.
14	R	CELL_DEAD_LOG_STS	1’b 0	Reports whether a dead cell event has been detected. This status is not cleared by shutting down. It can be cleared by the CELL_DEAD_DET_CLEAR command, WDT reset, or the fully powering down. 0: Not detected 1: Detected
13	R	RESERVED	N/A	Reserved. Do not change this register value.
12	R/W (can lock to read-only)	CELL_MSMT_FAULT_EN	1’b 0	Enables a cell mismatch event to provide a fault protection. When enabled, this cell mismatch event provides a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
11	R/W	CELL_MSMT_EN	1’b 0	Enables cell mismatch monitoring protection. This bit must be enabled to trigger cell mismatch faults or interrupts (which both have their own enable controls as well). This bit allows OTP. 0: Disabled 1: Enabled
10	R/W	CELL_DEAD_STS_SEL	1’b 0	Selects what each of the CELL_x_DEAD_STS bits report. 0: Report the latched cell x’s status going to the interrupt controller 1: Report the latest outcome of cell x’s dead check
9	R/W (can lock to read-only)	CELL_DEAD_FAULT_EN	1’b 0	Enables a dead cell event to provide a fault protection. When enabled, this cell dead event provides a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
8	R/W (can lock to read-only)	CELL_DEAD_EN	1’b 0	Enables dead cell protection. This bit must be enabled to trigger dead cell faults or interrupts (which both have their own enable controls as well). This bit allows OTP. 0: Disabled 1: Enabled
7:6	R	RESERVED	N/A	Reserved. Do not change this register value.

5	R/W (can lock to read-only)	VTOP_OV_FAULT_EN_CTRL	1’b 0	Enables battery pack (C10 to AGND) over-voltage protection (OVP). This bit allows OTP. 0: Disabled 1: Enabled
4	R/W	VTOP_OV_EN_CTRL	1’b 0	Enables monitoring the battery pack (C10 to AGND). This bit allows OTP. 0: Disabled 1: Enabled
3:2	R	RESERVED	N/A	Reserved. Do not change this register value.
1	R/W (can lock to read-only)	VTOP_UV_FAULT_EN_CTRL	1’b 0	Enables battery pack (C10 to AGND) under-voltage protection (UVP). This bit allows OTP. 0: Disabled 1: Enabled
0	R/W	VTOP_UV_EN_CTRL	1’b 0	Enables monitoring for battery pack (C10 to AGND) UVP. This bit allows OTP. 0: Disabled 1: Enabled

CELLFT_CTRL (35h)

Format: Unsigned binary

The CELLFT_CTRL command enables monitoring and fault protection for cell over-voltage (OV)/under-voltage (UV) events. It also controls the triggering logic for cell OV and cell UV events.

Bits	Access	Bit Name	Default	Description
15:13	R	RESERVED	N/A	Reserved. Do not change this register value.
12	R/W	CELL_OV_STS_SEL	1’b 0	Selects what each of the CELL_x_OV_STS bits report. 0: Report the latched cell x’s status going to the interrupt controller 1: Report the latest outcome of the cell x’s OV check
11	R/W	CELL_UV_STS_SEL	1’b 0	Selects what each of the CELL_x_UV_STS bits report. 0: Report the latched cell x’s status going to the interrupt controller 1: Report the latest outcome of the cell x’s UV check
10:9	R/W	CELL_OV_INT_TYPE	2’b 01	Controls the triggering logic for cell OV interruption. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
8:7	R/W	CELL_UV_INT_TYPE	2’b 01	Controls the triggering logic for cell UV interrupt. 0x0: An interrupt is generated on the input status signal high 0x1: An interrupt is generated on the rising edge of the input status signal 0x2: An interrupt is generated on the falling edge of the input status signal 0x3: An interrupt is generated on the rising and falling edges of the input status signal
6	R	RESERVED	N/A	Reserved. Do not change this register value.

5	R/W (can lock to read-only)	CELL_OV_FAULT_EN	1’b 0	Enables a cell OV event to provide a fault protection. When enabled, this cell OV event provides a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
4	R/W (can lock to read-only)	CELL_OV_EN_CTRL	1’b 0	Enables cell OVP. This bit must be enabled for OV faults or interrupts to be triggered. This bit allows OTP. 0: Disabled 1: Enabled
3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R/W (can lock to read-only)	CELL_UV_FAULT_EN	1’b 0	Enables a cell UV event to provide a fault protection. When enabled, this cell UV event provides a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	CELL_UV_EN_CTRL	1’b 0	Enables cell UVP. This bit must be enabled for UV faults or interrupts to be triggered. This bit allows OTP. 0: Disabled 1: Enabled
0	R/W	SYNC_RT_STATUS	1’b 0	When this bit is set to on, it synchronizes the status bit to allow the voltage ADC monitoring input status to be cleared after it has been disabled. 0: Off 1: On

CELL_HYST (36h)

Format: Unsigned binary

The CELL_HYST command configures the cell over-voltage (OV) and cell under-voltage (UV) threshold hysteresis.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11:8	R/W	CELL_OV_HYST	4’b 1010	Sets the cell OV threshold hysteresis. These bits allow OTP. LSB: 19.5mV Range: 0mV to 292.5mV Value (mV) = Setting x 19.5
7:4	R/W	CELL_UV_HYST	4’b 1010	Sets the cell UV threshold hysteresis. These bits allow OTP. LSB: 19.5mV Range: 0mV to 292.5mV Value (mV) = Setting x 19.5
3:0	R	RESERVED	N/A	Reserved. Do not change this register value.

PACK_UV_OV (37h)

Format: Unsigned binary

The PACK_UV_OV command configures the V_{TOP} over-voltage (OV) and under-voltage (UV) threshold hysteresis. It also reports the real-time V_{TOP} OV and UV statuses.

Bits	Access	Bit Name	Default	Description
15:10	R/W	VTOP_OV_HYST	6'b 100000	Sets the battery pack OV threshold hysteresis. These bits allow MTP. LSB: 78.125mV Range: 0mV to 4921.875mV Value (mV) = Setting x 78.125
9	R	RESERVED	N/A	Reserved. Do not change this register value.
8	R	VTOP_OV_RT_STS	1'b 0	Reports the real-time result of the stack top voltage vs. OV threshold comparison. Depending on the settings, a hysteresis may be applied to the threshold for comparison. 0: $V_{C10\_AGND} \leq$ OV threshold 1: $V_{C10\_AGND} >$ OV threshold
7:2	R/W	VTOP_UV_HYST	6'b 100000	Sets the battery pack UV threshold hysteresis. These bits allow MTP. LSB: 78.125mV Range: 0mV to 4921.875mV Value (mV) = Setting x 78.125
1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R	VTOP_UV_RT_STS	1'b 0	Reports the real-time result of the stack top voltage vs. UV threshold comparison. Depending on the settings, a hysteresis may be applied to the threshold for comparison. 0: $V_{C10\_AGND} \geq$ UV threshold 1: $V_{C10\_AGND} <$ UV threshold

CELL_UV (38h)

Format: Unsigned binary

The CELL_UV command configures the cell under-voltage (UV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11:8	R/W (can lock to read-only)	CELL_UV_DG	4'b 0000	Sets the cell UV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. These bits allow OTP. 0x0: A UV condition is reported as soon as the UV threshold is reached 0x1: A UV condition is reported when the current and previous protection readings violate the cell UV threshold ... 0xF: A UV condition is reported when a total of 16 protection cycles violate the cell UV threshold
7:0	R/W (can lock to read-only)	CELL_UV	8'b 10011000	Configures the cell UV threshold. These bits allow MTP. LSB: 19.53mV Range: 0mV to 4980.15mV Value (mV) = Setting x 19.53

CELL_OV (39h)

Format: Unsigned binary

The CELL_OV command configures the cell over-voltage (OV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11:8	R/W (can lock to read-only)	CELL_OV_DG	4'b 0000	Sets the cell OV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. These bits allow OTP. 0x0: An OV condition is reported as soon as the OV threshold is reached 0x1: An OV condition is reported when the current and previous protection readings violate the cell OV threshold ... 0xF: An OV condition is reported when a total of 16 protection cycles violate the cell OV threshold
7:0	R/W (can lock to read-only)	CELL_OV	8'b 11010111	Configures the cell OV threshold. These bits allow MTP. LSB: 19.53mV Range: 0mV to 4980.15mV Value (mV) = Setting x 19.53

PACK_UV (3Ah)

Format: Unsigned binary

The PACK_UV command configures the V_{TOP} under-voltage (UV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R/W	VTOP_UV_DG	4'b 0000	Sets the TOP UV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. These bits allow OTP. 0x0: A UV condition is reported as soon as the UV threshold is reached 0x1: A UV condition is reported when the current and previous protection readings violate the TOP UV threshold ... 0xF: A UV condition is reported when a total of 16 protection cycles violate the TOP UV threshold
11:0	R/W	VTOP_UV_LIMIT	12'b 010110011010	Configures the battery pack UV threshold. These bits allow MTP. LSB: 19.531mV Range: 0mV to 79979.445mV Value (mV) = Setting x 19.531

PACK_OV (3Bh)

Format: Unsigned binary

The PACK_OV command configures the V_{TOP} over-voltage (OV) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:12	R/W	VTOP_OV_DG	4'b 0000	Sets the TOP OV deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. These bits allow OTP. 0x0: An OV condition is reported as soon as the OV threshold is reached 0x1: An OV condition is reported when the current and previous protection readings violate the TOP OV threshold ... 0xF: An OV condition is reported when a total of 16 protection cycles violate the TOP OV threshold

11:0	R/W	VTOP_OV_LIMIT	12'b 100001100 110	Configures the battery pack OV threshold. These bits allow MTP. LSB: 19.531mV Range: 0mV to 79979.445mV Value (mV) = Setting x 19.531

CELL_DEAD_THR (3Ch)

Format: Unsigned binary

The CELL_DEAD_THR command configures the dead cell threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10:7	R/W	CELL_DEAD_DGL_N	4'b 0000	Sets the dead cell deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. These bits allow OTP. 0x0: A dead cell condition is reported as soon as the dead cell threshold is reached 0x1: A dead cell condition is reported when the current and previous protection readings violate the dead cell threshold ... 0xF: A dead cell condition is reported when a total of 16 protection cycles violate the dead cell threshold
6:0	R/W	CELL_DEAD_LIMIT	7'b 1101000	Configures the dead cell threshold. These bits allow MTP. LSB: 19.53mV Range: 0mV to 2480.31mV Value (mV) = Setting x 19.53

CELL_MSMT (3Dh)

Format: Unsigned binary

The CELL_MSMT command configures the cell mismatch (MSMT) threshold and deglitch delay.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change this register value.
8:5	R/W	CELL_MSMT_DGL_N	4'b 0000	Sets the mismatched cell deglitch delay, which can be set between 1 reading (no deglitch) and 16 readings. These bits allow OTP. 0x0: A mismatched cell condition is reported as soon as the mismatched cell threshold is reached 0x1: A mismatched cell condition is reported when the current and previous protection readings violate the mismatched cell threshold ... 0xF: A mismatched cell condition is reported when a total of 16 protection cycles violate the mismatched cell threshold
4:0	R/W	MSMT_TH	5'b 00010	Sets the mismatched cell threshold. These bits allow OTP. LSB: 39.06mV Range: 0mV to 1210.86mV Value (mV) = Setting x 39.06

RD_NTC_DIE (3Eh)

Format: Unsigned binary

The RD_NTC_DIE command reports the NTC PCB hot and NTC cell charging/discharging hot/cold status. It also reports the die's temperature in real time, as well as its interrupt status.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	R	DIE_TEMP_DIG_STS	1'b 0	Reports the die temperature interrupt status. The latched value depends on the interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. This bit is cleared by DIE_TEMP_DIG_CLEAR. 0: No digital die temperature event has been detected 1: The digital die temperature event has been detected
13	R	DIE_TEMP_DIG_RT_STS	1'b 0	Reports the real-time digital die temperature status, based on the result of the latest comparison between the digital die temperature reading and the associated hot threshold. 0: The die temperature is within its normal range 1: The digital die temperature is too hot
12	R	RESERVED	N/A	Reserved. Do not change this register value.
11	R	NTC4_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC4 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC4 PCB temperature is within its normal range 1: The NTC4 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected

10	R	NTC3_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC3 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC3 PCB temperature is within its normal range 1: The NTC3 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected
9	R	NTC2_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC2 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC2 PCB temperature is within its normal range 1: The NTC2 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected
8	R	NTC1_PCB_MNTR_HOT_STS	1'b 0	Reports the NTC1 hot PCB interrupt status. Depending on PCB_MNTR_STS_SEL, this bit may report the latched status or the real-time status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. If PCB_MNTR_STS_SEL reports the real-time status: 0: The NTC1 PCB temperature is within its normal range 1: The NTC1 PCB temperature is too hot If PCB_MNTR_STS_SEL reports the latched status: 0: No interrupt has been detected 1: An interrupt has been detected

7	R	NTC4_CELL_DSG_STS	1'b 0	Reports the NTC4 cell's discharging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected
6	R	NTC3_CELL_DSG_STS	1'b 0	Reports the NTC3 cell's discharging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected
5	R	NTC2_CELL_DSG_STS	1'b 0	Reports the NTC2 cell's discharging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected
4	R	NTC1_CELL_DSG_STS	1'b 0	Reports the NTC1 cell's discharging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected
3	R	NTC4_CELL_CHG_STS	1'b 0	Reports the NTC4 cell's charging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected

2	R	NTC3_CELL_CHG_STS	1'b 0	Reports the NTC3 cell's charging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected
1	R	NTC2_CELL_CHG_STS	1'b 0	Reports the NTC2 cell's charging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected
0	R	NTC1_CELL_CHG_STS	1'b 0	Reports the NTC1 cell's charging hot/cold interrupt status. The latched value depends on the selected interrupt type (e.g. rising, falling, or rising and falling). For a rising edge type, the bit is set to 1 if a rising edge is detected. For a falling edge type, the bit is set to 1 if a falling edge is detected. For a rising and falling edge type, the bit is set to 1 if either edge is detected. For a level type, the bit is set to 1 if the source signal is high. 0: No interrupt detected 1: An interrupt was detected

RD_V_NTC4_LR (3Fh)

Format: Unsigned binary

The RD_V_NTC4_LR command reports the NTC1~4 cell's discharging hot/cold real-time status. It also reports NTC4's ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	NTC4_CELL_DSG_RT_STS	1'b 0	Reports the NTC4 cell's discharging hot/cold real-time status. 0: The NTC4 is within its normal temperature range 1: The NTC4 exceeds the discharging temperature range
14	R	NTC3_CELL_DSG_RT_STS	1'b 0	Reports the NTC3 cell's discharging hot/cold real-time status. 0: The NTC3 is within its normal temperature range 1: The NTC3 exceeds the discharging temperature range
13	R	NTC2_CELL_DSG_RT_STS	1'b 0	Reports the NTC2 cell's discharging hot/cold real-time status. 0: The NTC2 is within its normal temperature range 1: The NTC2 exceeds the discharging temperature range
12	R	NTC1_CELL_DSG_RT_STS	1'b 0	Reports the NTC1 cell's discharging hot/cold real-time status. 0: The NTC1 is within its normal temperature range 1: The NTC1 exceeds the discharging temperature range
11:10	R	RESERVED	N/A	Reserved. Do not change this register value.

9:0	R	NTC4_VALUE	10’b 0000000000	Reports the NTC4 protection ADC reading. NTC4 monitoring is controlled by NTC4_EN, so this register updates when protection monitoring is requested and NTC4_EN is enabled. The value can be calculated with the following equation: Value = Reading x 0.09766%

RD_V_NTC3_LR (40h)

Format: Unsigned binary

The RD_V_NTC3_LR command reports the NTC1~4 cell charging hot/cold real-time status. It also reports NTC3’s ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	NTC4_CELL_CHG_RT_STS	1’b 0	Reports the NTC4 cell charging hot/cold real-time status. 0: The NTC4 is within its normal temperature range 1: The NTC4 exceeds the charging temperature range
14	R	NTC3_CELL_CHG_RT_STS	1’b 0	Reports the NTC3 cell charging hot/cold real-time status. 0: The NTC3 is within its normal temperature range 1: The NTC3 exceeds the charging temperature range
13	R	NTC2_CELL_CHG_RT_STS	1’b 0	Reports the NTC2 cell charging hot/cold real-time status. 0: The NTC2 is within its normal temperature range 1: The NTC2 exceeds the charging temperature range
12	R	NTC1_CELL_CHG_RT_STS	1’b 0	Reports the NTC1 cell charging hot/cold real-time status. 0: The NTC1 is within its normal temperature range 1: The NTC1 exceeds the charging temperature range
11:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	NTC3_VALUE	10’b 0000000000	Reports the NTC3 protection ADC reading. NTC3 monitoring is controlled by NTC3_EN, so this register updates when protection monitoring is requested and NTC3_EN is enabled. The value can be calculated with the following equation: Value = Reading x 0.09766%

RD_V_NTC2_LR (41h)

Format: Unsigned binary

The RD_V_NTC2_LR command reports NTC2’s ADC reading.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	NTC2_VALUE	10’b 0000000000	Reports the NTC2 protection ADC reading. NTC2 monitoring is controlled by NTC2_EN, so this register updates when protection monitoring is requested and NTC2_EN is enabled. The value can be calculated with the following equation: Value = Reading x 0.09766%

RD_V_NTC1_LR (42h)

Format: Unsigned binary

The RD_V_NTC1_LR command reports NTC1’s ADC reading.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.

9:0	R	NTC1_VALUE	10’b 0000000000	Reports the NTC1 protection ADC reading. NTC1 monitoring is controlled by NTC1_EN, so this register updates when protection monitoring is requested and NTC1_EN is enabled. The value can be calculated with the following equation: Value = Reading x 0.09766%

RD_T_DIE (43h)

Format: Unsigned binary

The RD_T_DIE command reports the die’s temperature ADC reading.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	DIE_TEMP_V	10’b 0000000000	Reports the die temperature, which can be calculated with the following equation: T = Reading x 0.474 - 269.12°C

NTC_CLR (44h)

Format: Unsigned binary

The NTC_CLR command controls the clearing of an event when the digital die is too hot. It also controls reporting the real-time or latched NTC PCB status.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	W	DIE_TEMP_DIG_ CLEAR	1’b 0	Write 1 to clear a digital die hot event. This bit is a self-clearing register.
13:3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R/W	PCB_MNTR_STS_ SEL	1’b 0	Controls the NTCx_PCB_MNTR_HOT_STS register. 0: Show the latched status going to the interrupt controller 1: Show the real-time status
1:0	R	RESERVED	N/A	Reserved. Do not change this register value.

DIE_CFG (46h)

Format: Unsigned binary

The DIE_CFG command enables digital die temperature monitoring and fault protection.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3	R/W (can lock to read-only)	DIE_TEMP_DIG_ FAULT_EN	1’b 0	Enables a die temperature hot event to provide a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
2	R	RESERVED	N/A	Reserved. Do not change this register value.
1	R/W (can lock to read-only)	DIE_TEMP_DIG_EN	1’b 1	Enables digital die temperature monitoring. This bit must be enabled for die temperature hot faults or interrupts to be triggered. This bit allows OTP. 0: Disabled 1: Enabled
0	R	RESERVED	N/A	Reserved. Do not change this register value.

NTC_CFG (47h)

Format: Unsigned binary

The NTC_CFG command configures NTC fault protection and monitoring.

Bits	Access	Bit Name	Default	Description
15	R/W (can lock to read-only)	PCB_MNTR_FAULT_EN	1'b 0	Enables a PCB NTC hot event to provide a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
14	R/W (can lock to read-only)	NTC_CELL_DSG_FAULT_EN	1'b 0	Enables an NTC cell discharge hot/cold event to provide a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
13	R/W (can lock to read-only)	NTC_CELL_CHG_FAULT_EN	1'b 0	Enables an NTC cell charging hot/cold event to provide a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
12:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10	R/W (can lock to read-only)	NTCB_DYNAMIC_ON	1'b 1	Enables a dynamic bias on NTCB during ADC conversions of the NTC channels. When disabled, NTCB is always enabled, which increases current consumption. This bit allows OTP. 0: Always stay on 1. Dynamic on
9	R/W (can lock to read-only)	NTC4_PD_EN	1'b 0	Enables the internal pull-down function on NTC3. This bit allows OTP. 0: Disabled 1: Enabled
8	R/W (can lock to read-only)	NTC3_PD_EN	1'b 0	Enables the internal pull-down function on NTC4. This bit allows OTP. 0: Disabled 1: Enabled
7	R/W (can lock to read-only)	NTC4_TYPE_SEL	1'b 1	Configures the NTC4 monitor type. This bit allows OTP. 0: Cell monitor 1: PCB monitor
6	R/W (can lock to read-only)	NTC4_EN	1'b 0	Enables protection monitoring for NTC4 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG. This bit allows OTP. 0: Disabled 1: Enabled
5	R/W (can lock to read-only)	NTC3_TYPE_SEL	1'b 0	Configures the NTC3 monitor type. This bit allows OTP. 0: Cell monitor 1: PCB monitor
4	R/W (can lock to read-only)	NTC3_EN	1'b 0	Enables protection monitoring for NTC3 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG. This bit allows OTP. 0: Disabled 1: Enabled

3	R/W (can lock to read-only)	NTC2_TYPE_SEL	1’b 0	Configures the NTC2 monitor type. This bit allows OTP. 0: Cell monitor 1: PCB monitor
2	R/W (can lock to read-only)	NTC2_EN	1’b 0	Enables protection monitoring for NTC2 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG. This bit allows OTP. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	NTC1_TYPE_SEL	1’b 0	Configures the NTC1 monitor type. This bit allows OTP. 0: Cell monitor 1: PCB monitor
0	R/W (can lock to read-only)	NTC1_EN	1’b 0	Enables protection monitoring for NTC1 if monitoring is required. Monitoring is automatically required when the IC is not in safe mode, but this function can be enabled in safe mode with PROTECT_IN_SAFE_CFG. This bit allows OTP. 0: Disabled 1: Enabled

NTCC_OTHR_DSG (48h)

Format: Unsigned binary

The NTCC_OTHR_DSG command configures the discharge NTC hot cell monitor voltage threshold.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R/W (can lock to read-only)	NTC_CELL_HOT_DSG	10’b 0100101110	Sets the discharge NTC hot cell monitor voltage threshold. The limit is triggered if the value is equal to or below the set threshold. These bits allow MTP. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766

NTCC_UTHR_DSG (49h)

Format: Unsigned binary

The NTCC_UTHR_DSG command configures the discharge NTC cold cell monitor voltage threshold.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R/W (can lock to read-only)	NTC_CELL_COLD_DSG	10’b 1010010100	Sets the discharge NTC cold cell monitor voltage threshold. The limit is triggered if the value exceeds the set threshold. These bits allow MTP. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766

NTCC_OTHR_CHG (4Ah)

Format: Unsigned binary

The NTCC_OTHR_CHG command configures the charge NTC hot cell monitor voltage threshold.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.

9:0	R/W (can lock to read-only)	NTC_CELL_HOT_CHG	10'b 0100101110	Sets the charge NTC hot cell monitor voltage threshold. The limit is triggered if the value is equal to or below the set threshold. These bits allow MTP. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766

NTCC_UTHR_CHG (4Bh)

Format: Unsigned binary

The NTCC_UTHR_CHG command configures the charge NTC cold cell monitor voltage threshold and NTC cell monitor hysteresis.

Bits	Access	Bit Name	Default	Description
15:11	R/W (can lock to read-only)	NTC_CELL_HYST	5'b 10001	Sets the NTC cell monitor hysteresis. These bits allow OTP. LSB: 0.1953% Range: 0% to 6.0543% Value (%) = Setting x 0.1953
10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R/W (can lock to read-only)	NTC_CELL_COLD_CHG	10'b 1010010100	Sets the charge NTC cold cell monitor voltage threshold. The limit is triggered if the value exceeds the set threshold. These bits allow MTP. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766

NTCM_OTHR (4Ch)

Format: Unsigned binary

The NTCM_OTHR command configures the NTC hot PCB monitor threshold and hysteresis.

Bits	Access	Bit Name	Default	Description
15:11	R/W	PCB_MNTR_HYST	5'b 10000	Sets the NTC hot PCB monitor hysteresis. These bits allow OTP. LSB: 0.1953% Range: 0% to 6.0543% Value (%) = Setting x 0.1953
10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R/W	PCB_MNTR_HOT	10'b 0011101011	Sets the NTC hot PCB monitor voltage threshold. The limit is triggered if the NTC reading is equal to or below the set threshold. These bits allow OTP. LSB: 0.09766% Range: 0% to 99.906% Value (%) = Setting x 0.09766

DIE_OT (4Dh)

Format: Unsigned binary

The DIE_OT command configures the digital die temperature threshold and hysteresis.

Bits	Access	Bit Name	Default	Description
15:11	R/W	DIE_TEMP_HYST	5'b 10101	Sets the digital die temperature hysteresis. These bits allow OTP. LSB: 0.474°C Range: 0°C to 14.694°C Value (°C) = Setting x 0.474
10	R	RESERVED	N/A	Reserved. Do not change this register value.

9:0	R/W	DIE_TEMP_HOT	10’b 1011101100	Sets the digital die temperature threshold. These bits allow OTP. LSB: 0.474°C Offset: - 269.12°C Range: - 269.12°C to +215.782°C Value (°C) = Setting x 0.474 - 269.12

SELF_STS (4Eh)

Format: Unsigned binary

The SELF_STS command reports the NVM CRC check outcome, V_{DD} under-voltage (UV), 3V3 UV, and REGIN UV detection results, as well as the ADC self-test over-voltage (OV)/UV detection results.

Bits	Access	Bit Name	Default	Description
15:7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R	NVM_CRC_ OUTCOME	1’b 0	Reports the errors in the outcome NVM CRC check. The result of the previous check is retained until NVM_CRC_DO is set to 1 (from 0). Then NVM_CRC_OUTCOME remains at 0 until the check is completed and a new result is available. 0: No errors detected 1: One or more error(s) detected
5	R	NVMCHK_DONE_ STS	1’b 0	When true, the NVM CRC check is complete. This bit can be cleared by setting NVM_CRC_DO = 0. 0: False 1: True
4	R	VDD_STS	1’b 0	Reports whether a V_{DD} UV event has been detected. 0: Not detected 1: Detected
3	R	3V3_STS	1’b 0	Reports whether a 3V3 UV event has been detected. 0: Not detected 1: Detected
2	R	REGIN_STS	1’b 0	Reports whether a REGIN UV event has been detected. 0: Not detected 1: Detected
1	R	SELF_TEST_STS_ OV	1’b 0	Reports whether an ADC self-test OV has been detected. 0: Not detected 1: Detected
0	R	SELF_TEST_STS_ UV	1’b 0	Reports whether an ADC self-test UV has been detected. 0: Not detected 1: Detected

RD_VA1P8 (4Fh)

Format: Unsigned binary

The RD_VA1P8 command reports the VDD regulator ADC reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	VDD_VALUE	10’b 0000000000	Reports the latest ADC reading for the VDD regulator, calculated with the following equation: Value = Reading x 3.2227mV

RD_VA3P3 (50h)

Format: Unsigned binary

The RD_VA3P3 command reports the 3V3 regulator ADC reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	3V3_VALUE	10'b 0000000000	Reports the latest ADC reading for the 3V3 regulator, calculated with the following equation: Value = Reading x 6.4453mV

RD_VA5 (51h)

Format: Unsigned binary

The RD_VA5 command reports the REGIN ADC reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	REGIN_VALUE	10'b 0000000000	Reports the latest ADC reading for REGIN, calculated with the following equation: Value = Setting x 6.4453mV

RD_VASELF (52h)

Format: Unsigned binary

The RD_VASELF command reports the ADC self-test reading result.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	SELF_TEST_VALUE	10'b 0000000000	Reports the latest 10-bit ADC reading for the internal fixed voltage reference, which acts as an ADC self-test. The value can be calculated with the following equation: Value = Setting x 3.2227mV

RD_OPENH (53h)

Format: Unsigned binary

The RD_OPENH command reports the C0~C10 open wire detection results.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10	R	CELL_10_OPW_STS	1'b 0	Reports whether C10 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
9	R	CELL_9_OPW_STS	1'b 0	Reports whether C9 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected

8	R	CELL_8_OPW_STS	1’b 0	Reports whether C8 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
7	R	CELL_7_OPW_STS	1’b 0	Reports whether C7 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
6	R	CELL_6_OPW_STS	1’b 0	Reports whether C6 has as an open wire after a detection has been executed. 0: Not detected 1: Detected
5	R	CELL_5_OPW_STS	1’b 0	Reports whether C5 has as an open wire after a detection has been executed. 0: Not detected 1: Detected
4	R	CELL_4_OPW_STS	1’b 0	Reports whether C4 has as an open wire after a detection has been executed. 0: Not detected 1: Detected
3	R	CELL_3_OPW_STS	1’b 0	Reports whether C3 has as an open wire after a detection has been executed. 0: Not detected 1: Detected
2	R	CELL_2_OPW_STS	1’b 0	Reports whether C2 has as an open wire after a detection has been executed. 0: Not detected 1: Detected
1	R	CELL_1_OPW_STS	1’b 0	Reports whether C1 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected
0	R	CELL_0_OPW_STS	1’b 0	Reports whether C0 has as an open wire after a detection has been executed. The cell must be enabled from CELL_S_CTRL for this flag to function. 0: Not detected 1: Detected

SFT_GO (55h)

Format: Unsigned binary

The SFT_GO command reports the open wire detection error and completion. It also controls the start of open wire and the clearing of NVM CRC.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.

10	R	OPEN_WIRE_ERR_STS	1’b 0	Reports whether an error has occurred during open-wire detection (e.g. cell-balancing is already operating). 0: False 1: True
9	R	OPEN_WIRE_DONE_STS	1’b 0	Reports whether open-wire detection is complete. When true, open-wire detection is complete. Write 0 to OPEN_WIRE_GO to clear this flag. 0: False 1: True
8	R/W	OPEN_WIRE_GO	1’b 0	Write 1 to this bit to schedule an open-wire check. Write 0 to this bit to clear the results of a completed open-wire detection.
7:1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R/W	NVM_CRC_DO	1’b 0	Write 0 to this bit to clear the results. Write 1 to this bit to schedule an NVM CRC.

SELF_CFG (56h)

Format: Unsigned binary

The SELT_CFG command enables NVM CRC, 3V3 under-voltage (UV), and V_{DD} UV fault protection. It also enable open-wire detection when the device is powered on as well as open-wire fault protection and NVM CRC, ADC self-test check, 3V3, VDD, and REGIN UV monitoring.

Bits	Access	Bit Name	Default	Description
15	R/W (can lock to read-only)	NVM_FAULT_EN	1’b 0	Enables the NVM CRC error event to provide a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
14	R/W (can lock to read-only)	3V3_VDD_FAULT_EN	1’b 0	Enables the 3.3V UV or VDD UV event (analog comparator and ADC monitoring) to provide a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
13:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10	R/W (can lock to read-only)	OPEN_WIRE_PON	1’b 0	Enables open-wire detection when the device is powered on (leaving shutdown mode). This bit allows OTP. 0: Disabled 1: Enabled
9	R/W (can lock to read-only)	OPEN_WIRE_FAULT_EN	1’b 0	Enables the open wire event to provide a fault protection. This bit allows OTP. 0: Disabled 1: Enabled
8:7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R/W (can lock to read-only)	NVM_CRC_EN	1’b 1	Enables the NVM CRC. This bit allows OTP. 0: Disabled 1: Enabled
5:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3	R/W (can lock to read-only)	ADC_SELF_TEST_EN	1’b 1	Enables the ADC self-test check that indicates whether the applied voltage is within the allowed range. This bit allows OTP. 0: Disabled 1: Enabled

2	R/W (can lock to read-only)	VDD_EN	1’b 1	Enables the ADC VDD monitoring check to ensure that the digital 1.8V supply is above the defined UV level. This bit allows OTP. 0: Disable VDD check 1: Enable VDD check
1	R/W (can lock to read-only)	3V3_EN	1’b 1	Enables ADC 3V3 UV monitoring to ensure that the 3.3V supply is above the defined UV level. This bit allows OTP. 0: Disabled 1: Enabled
0	R/W (can lock to read-only)	REGIN_EN	1’b 1	Enables ADC REGIN monitoring to ensure that the REGIN supply is above the defined UV level. This bit allows OTP. 0: Disable REGIN check 1: Enable REGIN check

OPEN_CFG (57h)

Format: Unsigned binary

The OPEN_CFG command configures the open-wire threshold and the length of each pull-up and pull-down phase.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11:8	R/W	OPW_CHECK_TH	4’b 0100	Sets the open-wire threshold used during the detection sequence. These bits allow OTP. LSB: 39.06mV Range: 39.06mV to 624.96mV Value (mV) = Setting x 39.06
7:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3:0	R/W	OPW_CHECK_LEN	4’b 0111	Sets the length of each pull-up and pull-down phase. These bits allow OTP. LSB: 1ms Offset: 1ms Range: 1ms to 16ms Value (ms) = Setting + 1

REGIN_UV (58h)

Format: Unsigned binary

The REGIN_UV command configures the threshold for REGIN under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change this register value.
8:0	R	REGIN_UV_LIMIT	9’b 101101101	Sets the threshold for REGIN UV conditions, which is applied to the ADC readings reported in REGIN_VALUE. LSB: 12.89mV Range: 0mV to 6586.79mV Value (mV) = Setting x 12.89

V3P3_UV (59h)

Format: Unsigned binary

The V3P3_UV command configures the threshold for 3V3 under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change this register value.

7:0	R/W	3V3_UV_LIMIT	8'b 11110000	Sets the threshold for 3V3 UV conditions, which is applied to the ADC reading reported in 3V3_VALUE. These bits allow OTP. LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89

VDD_UV (5Ah)

Format: Unsigned binary

The VDD_UV command configures the threshold for V_{DD} under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change this register value.
7:0	R	VDD_UV_LIMIT	8'b 10000100	Sets the threshold for VDD 1.8V UV conditions, which is applied to the ADC reading reported in VDD_VALUE. LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89

SELF_THR (5Bh)

Format: Unsigned binary

The SELF_THR command configures the thresholds for self-test over-voltage (OV) and under-voltage (UV) events.

Bits	Access	Bit Name	Default	Description
15:8	R	SELF_TEST_OV_ LIMIT	8'b 01100101	Sets the threshold for self-test OV conditions, which is applied to SELF_TEST_VALUE ADC readings. LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89
7:0	R	SELF_TEST_UV_ LIMIT	8'b 01010101	Sets the threshold for self-test UV conditions, which is applied to the SELF_TEST_VALUE ADC readings. LSB: 12.89mV Range: 0mV to 3286.95mV Value (mV) = Setting x 12.89

FT_STS1 (5Dh)

Format: Unsigned binary

The FT_STS1 command reports the fault status, including die temperature, charge short-circuit (SC), discharge SC, charge over-current (OC), discharge OC1, discharge OC2, NTC cell hot/cold discharging, NTC cell hot/cold charging, NTC PCB hot, TOP over-voltage (OV), TOP under-voltage (UV), open-wire, cell mismatch, dead cell, cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	R	DIE_TEMP_FAULT_ STS	1'b 0	Reports whether a die temperature condition is triggering a fault. 0: False 1: True
14	R	SC_CHG_FAULT_ STS	1'b 0	Reports whether a charge SC condition is triggering a fault. 0: False 1: True
13	R	SC_DCHG_FAULT_ STS	1'b 0	Reports whether a discharge SC condition is triggering a fault. 0: False 1: True

12	R	OC_CHG_FAULT_STS	1'b 0	Reports whether a charge OC condition is triggering a fault. 0: False 1: True
11	R	OC2_DCHG_FAULT_STS	1'b 0	Reports whether a discharge OC2 condition is triggering a fault. 0: False 1: True
10	R	OC1_DCHG_FAULT_STS	1'b 0	Reports whether a discharge OC1 condition is triggering a fault. 0: False 1: True
9	R	NTC_CELL_DSG_FAULT_STS	1'b 0	Reports whether an NTC cell monitoring fault triggered due to the NTC temperature exceeding the hot/cold discharging limit. 0: False 1: True
8	R	NTC_CELL_CHG_FAULT_STS	1'b 0	Reports whether an NTC cell monitoring fault triggered due to the NTC temperature exceeding the hot/cold charging limit. 0: False 1: True
7	R	PCB_MNTR_FAULT_STS	1'b 0	Reports whether an NTC PCB monitor condition is triggering a fault. 0: False 1: True
6	R	VTOP_OV_FAULT_STS	1'b 0	Reports whether a TOP OV condition is triggering a fault. 0: False 1: True
5	R	VTOP_UV_FAULT_STS	1'b 0	Reports whether a TOP UV condition is triggering a fault. 0: False 1: True
4	R	OPEN_WIRE_FAULT_STS	1'b 0	Reports whether an open-wire condition is triggering a fault. 0: False 1: True
3	R	CELL_MSMT_FAULT_STS	1'b 0	Reports whether a cell mismatch condition is triggering a fault. 0: False 1: True
2	R	CELL_DEAD_FAULT_STS	1'b 0	Reports whether a dead cell condition is triggering a fault. 0: False 1: True
1	R	CELL_OV_FAULT_STS	1'b 0	Reports whether a cell OV condition is triggering a fault. 0: False 1: True
0	R	CELL_UV_FAULT_STS	1'b 0	Reports whether a cell UV condition is triggering a fault. 0: False 1: True

FT_STS2 (5Eh)

Format: Unsigned binary

The FT_STS2 command reports fault statuses, including short-circuit (SC) removal detection, driver turn-on failures, V_{DD} under-voltage (UV), 3V3 UV, and OTP CRC fault events.

Bits	Access	Bit Name	Default	Description
15:14	R	RESERVED	N/A	Reserved. Do not change this register value.
13	R	RMVL_BUSY	1'b 0	When true, SC removal detection is busy. 0: False 1: True
12:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3	R	DRIVER_FAULT_STS	1'b 0	Reports whether a driver turn-on condition is triggering a fault. 0: False 1: True
2	R	VDD_FAULT_STS	1'b 0	Reports whether a V_{DD} UV event is triggering a fault. A V_{DD} fault can be triggered by ADC V_{DD} UV monitoring or the V_{DD} analog UV comparator. The V_{DD} analog comparator is always enabled, so when 3V3_VDD_FAULT_EN is enabled, it can trigger a fault even when ADC V_{DD} UV monitoring (VDD_EN) is disabled. 0: False 1: True
1	R	3V3_FAULT_STS	1'b 0	Reports whether a 3V3 UV event is triggering a fault. A 3V3 fault can be triggered by ADC 3V3 UV monitoring or the 3.3V analog UV comparator. The 3.3V analog comparator is always enabled, so when 3V3_VDD_FAULT_EN is enabled, it can trigger a fault even when ADC 3V3 UV monitoring (3V3_EN) is disabled. 0: False 1: True
0	R	OTP_CRC_FAULT_STS	1'b 0	Reports whether an OTP CRC condition is triggering a fault. This bit can be cleared with OTP_CRC_CLR. 0: False 1: True

FT_CLR (5Fh)

Format: Unsigned binary

The FT_CLR command clears faults, including die temperature, charge short-circuit (SC), discharge SC, charge over-current (OC), discharge OC1, discharge OC2, cell NTC hot/cold discharge, cell NTC hot/cold charge, NTC PCB monitor, TOP over-voltage (OV), TOP under-voltage (UV), open wire, cell mismatch, dead cell, cell OV, and cell UV events.

Bits	Access	Bit Name	Default	Description
15	W	DIE_TEMP_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a die temperature fault. This is a self-clearing register.
14	W	SC_CHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a charge SC fault. This is a self-clearing register.
13	W	SC_DCHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a discharge SC fault. This is a self-clearing register.
12	W	OC_CHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a charge OC fault. This is a self-clearing register.
11	W	OC2_DCHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a discharge OC 2 fault. This is a self-clearing register.

10	W	OC1_DCHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a discharge OC 1 fault. This is a self-clearing register.
9	W	NTC_CELL_DSG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell NTC hot/cold discharge fault. This is a self-clearing register.
8	W	NTC_CELL_CHG_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell NTC hot/cold charge fault. This is a self-clearing register.
7	W	PCB_MNTR_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear an NTC PCB monitor fault. This is a self-clearing register.
6	W	VTOP_OV_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a battery pack OV fault. This is a self-clearing register.
5	W	VTOP_UV_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a battery pack UV fault. This is a self-clearing register.
4	W	OPEN_WIRE_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell open wire fault. This is a self-clearing register.
3	W	CELL_MSMT_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a mismatched cell fault. This is a self-clearing register.
2	W	CELL_DEAD_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a dead cell fault. This is a self-clearing register.
1	W	CELL_OV_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell OV fault. This is a self-clearing register.
0	W	CELL_UV_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a cell UV fault. This is a self-clearing register.

FT_REC (60h)

Format: Unsigned binary

The FT_REC command controls the manual fault clearing function for 3.3V and 1.8V under-voltage (UV), OTP CRC, and MOSFET driver events. It also enables automatic recovery from an NTC PCB monitor, NTC cell charge, NTC cell discharge fault, and it defines the NTC cell hot/cold recovery mode.

Bits	Access	Bit Name	Default	Description
15	W	3V3_VDD_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear 3.3V and 1.8V UV faults. This is a self-clearing register.
14	W	OTP_CRC_CLR	1'b 0	Write 1 to this bit to manually clear an OTP CRC fault. This is a self-clearing register.
13	W	DRIVER_FAULT_CLR	1'b 0	Write 1 to this bit to manually clear a MOSFET driver fault. This is a self-clearing register.
12	R/W (can lock to read-only)	DIE_TEMP_FAULT_REC	1'b 0	Enables automatic recovery from die temperature conditions (when the temperature drops). This bit allows OTP. 0: Manual recovery 1: Automatic recovery attempt
11:5	R	RESERVED	N/A	Reserved. Do not change this register value.
4	R/W (can lock to read-only)	PCB_MNTR_REC	1'b 0	Enables automatic recovery from an NTC PCB monitor type fault. Set this bit to 0 for manual recovery. This bit allows OTP. 0: Disabled 1: Enabled

3	R/W	NTC_CHG_HYS_MODE	1’b 0	Defines the normal threshold from an NTC hot/cold condition in charge mode. This bit allows OTP. 0: NTC voltage [>/<] NTC_CELL_xxxx_CHG ± NTC_CELL_HYST 1: (NTC voltage [>/<] NTC_CELL_xxxx_CHG ± NTC_CELL_HYST) or if the charger is removed: (NTC voltage [>/<] NTC_CELL_xxxx_CHG)
2	R/W (can lock to read-only)	NTC_CELL_CHG_REC	1’b 0	Enables auto-recovery from an NTC cell type fault (the temperature is back within the nominal range) in charge mode. Set this bit to 0 for manual recovery. This bit allows OTP. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	NTC_CELL_DSG_REC	1’b 0	Enables auto-recovery from an NTC cell type fault (the temperature is back within the nominal range) in discharge mode or standby mode. Set this bit to 0 for manual recovery. This bit allows OTP. 0: Disabled 1: Enabled
0	R	RESERVED	N/A	Reserved. Do not change this register value.

FT0_CFG (61h)

Format: Unsigned binary

The FT0_CFG command enables automatic cell over-voltage (OV)/under-voltage (UV) fault recovery, configures MOSFET behavior when a cell OV/UV fault occurs, and sets the recovery logic from cell OV/UV faults. It also enables the additional recovery logic for CHG FETs recovery during cell OV/UV faults. It also configures MOSFET behavior when a cell NTC fault occurs, enables the additional recovery logic, and sets the standby current direction in response to an NTC charge or discharge fault.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11	R/W (can lock to read-only)	CELL_OV_REC	1’b 0	Enables automatic recovery for a cell OV fault. This bit allows OTP. 0: Manual recovery 1: Automatic recovery attempt
10	R/W (can lock to read-only)	CELL_OV_FAULT_ACTION	1’b 0	Sets the MOSFET behavior when a cell OV fault occurs. This bit allows OTP. 0: Only turn off the CHG MOSFET 1. Turn off the CHG and DSG MOSFETs
9	R/W (can lock to read-only)	CELL_OV_LOGIC_SEL	1’b 0	Selects which logic is used for status recovery from cell OV conditions. This bit allows OTP. 0: The status recovers by following either logic below: • The cell is below the OV threshold, CELL_OV_CHG_REC_MODE = 1, and the battery pack current status is in discharge • The cell is below (OV threshold - hysteresis) 1: The status recovers by following either logic below: • The cell is below the OV threshold and the PACKP voltage is below (V_{TOP} -1.77V) • The cell is below (OV threshold - hysteresis)

8	R/W (can lock to read-only)	CELL_OV_CHG_REC_MODE	1'b 1	Enables the additional recovery logic for the CHG FET's recovery action during a cell OV fault. When it is set to 1, if automatic recovery is enabled and set as a CHG FET off only, the CHG FET automatically turns on when a discharge condition is detected (V_{PACKP} < V_{TOP} or discharge current), while the fault state remains until the cell voltage returns to normal. This bit allows OTP. When this bit is set to 1, then CELL_OV_LOGIC_SEL must be set to 0. 0: Disabled 1: Enabled
7	R/W (can lock to read-only)	CELL_UV_REC	1'b 0	Enables automatic recovery for cell UV fault. This bit allows OTP. 0: Manual recovery 1: Automatic recovery attempt
6	R/W (can lock to read-only)	CELL_UV_FAULT_ACTION	1'b 0	Sets the MOSFET behavior when a cell UV fault occurs. This bit allows OTP. 0: Only turn off the DSG MOSFET 1. Turn off the CHG and DSG MOSFET
5	R/W (can lock to read-only)	CELL_UV_LOGIC_SEL	1'b 0	Selects which logic is used for status recovery from cell UV conditions. This bit allows OTP. 0: The status recovers by following either logic below: • The cell exceeds the UV threshold, CELL_UV_DSG_REC_MODE = 1, and the battery pack current exceeds the standby current • The cell exceeds (UV threshold + hysteresis) 1: The status recovers by following either logic below: • The cell exceeds the UV threshold and the PACKP voltage exceeds (V_{TOP} + 280mV) • The cell exceeds (UV threshold + hysteresis)
4	R/W (can lock to read-only)	CELL_UV_DSG_REC_MODE	1'b 1	Enables the additional recovery logic for the DSG FET's recovery action during a cell OV fault. When it is set to 1, if automatic recovery is enabled to turn off only the DSG FET, the DSG FET automatically turns on when a charge condition is detected (V_{PACKP} > V_{TOP} or discharge current), while the fault state remains until the cell voltage returns to normal. This bit allows OTP. When this bit is set to 1, then CELL_UV_LOGIC_SEL must be set to 0. 0: Disabled 1: Enabled
3	R/W	NTC_CELL_CHG_REC_MODE	1'b 0	Enables the additional recovery logic from an NTC hot/cold condition in charge mode, which allow the CHG FET fault to auto-recover if V_{PACKP} < V_{TOP}, or if the battery pack current state is in discharge. This setting is only valid when NTC_CELL_CHG_REC = 1 and NTC_CELL_CHG_ACTION = 0. 0: Disabled 1: Enabled
2	R/W	NTC_CELL_STBY_MODE	1'b 0	Determines if standby current is considered to be the charge current, or if it is the discharge current in response to an NTC charge or discharge fault. 0: Discharge 1: Charge

1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R/W (can lock to read-only)	NTC_CELL_CHG_ACTION	1’b 0	Sets the MOSFET behavior when NTC cell hot or cold fault happened during charging. This bit allows OTP. 0: Only turn off the CHG MOSFET 1. Turn off the CHG and DSG MOSFET

FT1_CFG (62h)

Format: Unsigned binary

The FT1_CFG command configures the battery pack pull-up current and time during short-circuit (SC) removal detection.

Bits	Access	Bit Name	Default	Description
15:4	R	RESERVED	N/A	Reserved. Do not change this register value.
3:2	R/W	SCOC_DET_TIME	2’b 00	Sets the time for SCOC_PUP. These bits allow MTP. 0x0: 125ms 0x1: 250ms 0x2: 500ms 0x3: 1s
1:0	R/W	SCOC_PUP	2’b 00	Sets the battery pack pull-up current during SC removal detection. These bits allow MTP. 0x0: 250μA 0x1: 500μA 0x2: 750μA 0x3: 250μA

RD_CCIRQL (65h)

Format: Two’s complement (combining with CC_ACC_MSBS)

The RD_CCIRQL command reports the accumulated Coulomb counter reading for the LSB.

Bits	Access	Bit Name	Default	Description
15:0	R	CC_ACC_LSBS	16’b 0000000000000000	Reports the accumulated Coulomb counter reading for the LSB. This content is latched from the CC_RT_ACC registers when a Coulomb counting accumulation has been completed. The reading is complement-signed and 26 bits long (combined with CC_ACC_MSBS). The value ranges from -33554432 to +33554431.

RD_CCIRQH (66h)

Format: Unsigned binary, two’s complement

The RD_CCIRQH command reports the accumulated Coulomb counter reading for the MSB.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	CC_ACC_MSBS	10’b 0000000000	Reports the accumulated Coulomb counter reading for the MSB. This content is latched from the CC_RT_ACC registers when a Coulomb counting accumulation has been completed. The reading is complement-signed and 26 bits long (combined with CC_ACC_LSBS). The value ranges from -33554432 to +33554431. The value can be calculated with the following equation: Value (mΩ x A x s) = Reading / 32768 / 5

RD_CCACCQL (67h)

Format: Two's complement (combining with CC_RT_ACC_MSBS)

The RD_CCACCQL command reports the real-time accumulated Coulomb counter reading for the LSB.

Bits	Access	Bit Name	Default	Description
15:0	R	CC_RT_ACC_LSBS	16'b 0000000000000000	Returns the real-time accumulated Coulomb counter reading for the LSB. This register is constantly updated when Coulomb counting is active. The reading is complement-signed and 26 bits long (combining with CC_RT_ACC_MSBS). The value ranges from -33554432 to +33554431.

RD_CCACCQH (68h)

Format: Unsigned binary, two's complement

The RD_CCACCQH command reports the real-time accumulated Coulomb counter reading for the MSB.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R	CC_RT_ACC_MSBS	10'b 0000000000	Returns the real-time accumulated Coulomb counter reading for the MSB. This register is constantly updated when Coulomb counting is active. The reading is complement-signed and 26 bits long (combining with CC_RT_ACC_LSBS). The value ranges from -33554432 to +33554431. The value can be calculated with the following equation: Value (mΩ x A x s) = Reading / 32768 / 5

RD_VPACKP (69h)

Format: Unsigned binary

The RD_VPACKP command reports the PACKP high-resolution voltage reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	VPACK_V	15'b 000000000000000	Returns the PACKP high-resolution voltage reading, calculated with the following equation: Voltage = Reading x 80000 / 32768 (mV)

RD_VTOP (6Ah)

Format: Unsigned binary

The RD_VTOP command reports the C10 to AGND high-resolution voltage reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	VTOP_V	15'b 000000000000000	Returns the C10 to AGND high-resolution voltage reading, calculated with the following equation: Voltage = Reading x 80000 / 32768 (mV)

RD_ITOP (6Bh)

Format: Two's complement

The RD_ITOP command reports the battery pack current reading (synchronous to VTOP_V).

Bits	Access	Bit Name	Default	Description
15:0	R	VTOP_I	16'b 0000000000000000	Returns the battery pack current reading (synchronous to VTOP_V). The reading is 16-bit, complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL1 (6Ch)

Format: Unsigned binary

The RD_VCELL1 command reports cell 1's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_1_V	15'b 000000000000000	Returns cell 1's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL1 (6Dh)

Format: Two's complement

The RD_ICELL1 command reports cell 1's battery pack current reading (synchronous with CELL_1_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_1_I_SYNC	16'b 0000000000000000	Returns cell 1's battery pack current reading (synchronous with CELL_1_V). The reading is 16-bit, complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL2 (6Eh)

Format: Unsigned binary

The RD_VCELL2 command reports cell 2's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_2_V	15'b 000000000000000	Returns cell 2's high resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL2 (6Fh)

Format: Two's complement

The RD_ICELL2 command reports cell 2's battery pack current reading (synchronous with CELL_2_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_2_I_SYNC	16'b 0000000000000000	Returns cell 2's battery pack current reading (synchronous with CELL_2_V). The reading is 16-bit, complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL3 (70h)

Format: Unsigned binary

The RD_VCELL3 command reports cell 3's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_3_V	15'b 000000000 000000	Returns cell 3's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL3 (71h)

Format: Two's complement

The RD_ICELL3 command reports cell 3's battery pack current reading (synchronous with CELL_3_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_3_I_SYNC	16'b 000000000 0000000	Returns cell 3's battery pack current reading (synchronous with CELL_3_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL4 (72h)

Format: Unsigned binary

The RD_VCELL4 command reports cell 4's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_4_V	15'b 000000000 000000	Returns cell 4's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL4 (73h)

Format: Two's complement

The RD_ICELL4 command reports cell 4's battery pack current reading (synchronous with CELL_4_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_4_I_SYNC	16'b 000000000 0000000	Returns cell 4's battery pack current reading (synchronous with CELL_4_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ).The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL5 (74h)

Format: Unsigned binary

The RD_VCELL5 command reports cell 5's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_5_V	15'b 000000000 000000	Returns cell 5's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL5 (75h)

Format: Two's complement

The RD_ICELL5 command reports cell 5's battery pack current reading (synchronous with CELL_5_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_5_I_SYNC	16'b 0000000000000000	Returns cell 5's battery pack current reading (synchronous with CELL_5_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL6 (76h)

Format: Unsigned binary

The RD_VCELL6 command reports cell 6's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_6_V	15'b 000000000000000	Returns cell 6's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL6 (77h)

Format: Two's complement

The RD_ICELL6 command reports cell 6's battery pack current reading (synchronous with CELL_6_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_6_I_SYNC	16'b 0000000000000000	Returns cell 6's battery pack current reading (synchronous with CELL_6_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL7 (78h)

Format: Unsigned binary

The RD_VCELL7 command reports cell 7's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_7_V	15'b 000000000000000	Returns cell 7's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL7 (79h)

Format: Two's complement

The RD_ICELL7 command reports cell 7's battery pack current reading (synchronous with CELL_7_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_7_I_SYNC	16'b 0000000000000000	Returns cell 7's battery pack current reading (synchronous with CELL_7_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL8 (7Ah)

Format: Unsigned binary

The RD_VCELL8 command reports cell 8's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_8_V	15'b 000000000 000000	Returns cell 8's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL8 (7Bh)

Format: Two's complement

The RD_ICELL8 command reports cell 8's battery pack current reading (synchronous with CELL_8_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_8_I_SYNC	16'b 000000000 0000000	Returns cell 8's battery pack current reading (synchronous with CELL_8_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL9 (7Ch)

Format: Unsigned binary

The RD_VCELL9 command reports cell 9's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_9_V	15'b 000000000 000000	Returns cell 9's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL9 (7Dh)

Format: Two's complement

The RD_ICELL9 command reports cell 9's battery pack current reading (synchronous with CELL_9_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_9_I_SYNC	16'b 000000000 0000000	Returns cell 9's battery pack current reading (synchronous with CELL_9_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VCELL10 (7Eh)

Format: Unsigned binary

The RD_VCELL10 command reports cell 10's high-resolution reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	CELL_10_V	15'b 000000000 000000	Returns cell 10's high-resolution reading, calculated with the following equation: Voltage = Reading x 5000 / 32768 (mV)

RD_ICELL10 (7Fh)

Format: Two's complement

The RD_ICELL10 command reports cell 10's battery pack current reading (synchronous with CELL_10_V).

Bits	Access	Bit Name	Default	Description
15:0	R	CELL_10_I_SYNC	16'b 0000000000000000	Returns cell 10's battery pack current reading (synchronous with CELL_10_V). The reading is 16-bit complement-signed. R_{SENSE} is the external current-sense resistor (in mΩ). The current can be calculated with the following equation: Current = Reading x 100 / 32768 / R_{SENSE} (A)

RD_VNTC4 (8Ch)

Format: Unsigned binary

The RD_VNTC4 command reports NTC4's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	NTC4_HIRES_V	15'b 000000000000000	Returns NTC4's high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value. The value can be calculated with the following equation: Value = Reading x 100 / 32768 (%NTCB)

RD_VNTC3 (8Dh)

Format: Unsigned binary

The RD_VNTC3 command reports NTC3's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	NTC3_HIRES_V	15'b 000000000000000	Returns NTC3's high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value. The value can be calculated with the following equation: Value = Reading x 100 / 32768 (%NTCB)

RD_VNTC2 (8Eh)

Format: Unsigned binary

The RD_VNTC2 command reports NTC2's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	NTC2_HIRES_V	15'b 000000000000000	Returns NTC2's high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value. The value can be calculated with the following equation: Value = Reading x 100 / 32768 (%NTCB)

RD_VNTC1 (8Fh)

Format: Unsigned binary

The RD_VNTC1 command reports NTC1's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.

14:0	R	NTC1_HIRES_V	15'b 000000000 000000	Returns NTC1's high-resolution voltage ADC reading. This reading is ratiometric to NTCB, which has a 3.3V nominal value. The value can be calculated with the following equation: Value = Reading x 100 / 32768 (%NTCB)

RD_VGPIO3 (90h)

Format: Unsigned binary

The RD_VGPIO3 command reports GPIO3's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	GPIO3_VOLTAGE	15'b 000000000 000000	Returns GPIO3's high-resolution voltage reading, calculated with the following equation: Voltage = Reading x 3300 / 32768 (mV)

RD_VGPIO2 (91h)

Format: Unsigned binary

The RD_VGPIO2 command reports GPIO2's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	GPIO2_VOLTAGE	15'b 000000000 000000	Returns GPIO2's high-resolution voltage reading, calculated with the following equation: Voltage = Reading x 3300 / 32768 (mV)

RD_VGPIO1 (92h)

Format: Unsigned binary

The RD_VGPIO1 command reports GPIO1's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	GPIO1_VOLTAGE	15'b 000000000 000000	Returns GPIO1's high-resolution voltage reading, calculated with the following equation: Voltage = Reading x 3300 / 32768 (mV)

RD_TDIE (93h)

Format: Unsigned binary

The RD_TDIE command reports the die temperature's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	DIE_T_VOLTAGE	15'b 000000000 000000	Returns the die temperature's high-resolution reading, which is proportional to the internal die temperature. The temperature can be calculated with the following equation: T = Reading x 0.01481 - 269.12 (°C)

RD_V1P8 (94h)

Format: Unsigned binary

The RD_V1P8 command reports the 1.8V regulator's high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.

14:0	R	VDD_VOLTAGE	15’b 000000000 000000	Returns the 1.8V regulator’s (VDD) high-resolution reading, calculated with the following equation: Voltage = Reading x 3300 / 32768 (mV)

RD_V3P3 (95h)

Format: Unsigned binary

The RD_V3P3 command reports the 3.3V regulator’s high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	3V3_VOLTAGE	15’b 000000000 000000	Returns the 3.3V regulator’s (3V3) high-resolution reading, calculated with the following equation: Voltage = Reading x 6600 / 32768 (mV)

RD_V5 (96h)

Format: Unsigned binary

The RD_V5 command reports REGIN’s high-resolution ADC reading.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:0	R	REGIN_VOLTAGE	15’b 000000000 000000	Reports REGIN’s high-resolution reading, calculated with the following equation: Voltage = Reading x 6600 / 32768 (mV)

CC_STS (97h)

Format: Unsigned binary

The CC_STS command reports the Coulomb counter status.

Bits	Access	Bit Name	Default	Description
15:1	R	RESERVED	N/A	Reserved. Do not change this register value.
0	R	CC_STATUS	1’b 0	Reports whether the Coulomb counter is running. 0: False 1: True

ADC_STS (98h)

Format: Unsigned binary

The ADC_STS command reports the status of the internal scheduler and the feature command scheduler.

Bits	Access	Bit Name	Default	Description
15:13	R	RESERVED	N/A	Reserved. Do not change this register value.
12:11	R	VADC_FSM	2’b 00	Reports the internal scheduler’s status. 0x0: Idle 0x1: Refreshing voltage protection reading 0x2: Ready for the feature command 0x3: Not allowed
10	R	RESERVED	N/A	Reserved. Do not change this register value.

9:8	R	VADC_SCHEDULER	2’b 00	This field reports the status of the feature command scheduler. 0x0: Free 0x1: Executing voltage ADC scan 0x2: Executing cell-balancing 0x3: Executing open-wire detection
7:0	R	RESERVED	N/A	Reserved. Do not change this register value.

ADC_CTRL (99h)

Format: Unsigned binary

The ADC_CTRL command reports whether an error has occurred when starting the high-resolution voltage scan. It also controls the start of a high-resolution scan for all the selected channels.

Bits	Access	Bit Name	Default	Description
15:3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R	SCAN_ERROR_STS	1’b 0	Reports whether an error has occurred when starting the high-resolution voltage scan (e.g. if open-wire detection is already running). 0: False 1: True
1	R	SCAN_DONE_STS	1’b 0	Reports whether the high-resolution voltage scan status is complete (true) or not (false). 0: False 1: True
0	R/W	ADC_SCAN_GO	1’b 0	Write 1 to this bit to start a high-resolution scan for all the selected channels.

CC_CFG (9Ah)

Format: Unsigned binary

The CC_CFG command configures Coulomb counting: it enables Coulomb counting accumulation, back-to-back accumulation mode, and operation in power-save mode. It also sets the Coulomb counter integration length and reports the Coulomb counting results, such as the state machine error and completion.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14	R/W	CC_B2B_ACC_CTRL	1’b 0	Controls back-to-back accumulation mode. When enabled, a new Coulomb counting conversion automatically restarts as soon as the current count is completed. With back-to-back conversions enabled, the CC_RT_ACC_LSBS and CC_RT_ACC_MSBS registers are automatically cleared and do not report the progress of the new accumulation. This bit allows OTP. 0: Disabled 1: Enabled
13:8	R/W	CC_INT_CNT	6’b 111111	Sets the Coulomb counter integration length. The length is set as the number of time slots (32ms each). These bits allow OTP. 0x00: 1 slot (32ms) 0x01: 2 slots (64ms) 0x3F: 64 slots (2048ms)
7:6	R	RESERVED	N/A	Reserved. Do not change this register value.

5	R	CC_ERROR_STS	1’b 0	Reports whether a Coulomb counting state machine error has been detected. 0: Not detected 1: Detected
4	R	CC_DONE	1’b 0	Reports whether Coulomb counting accumulation has completed (true) or not (false). 0: False 1: True
3	R/W	CC_PWR_SAVE	1’b 0	Enables the Coulomb counter to operate in power-save mode. When disabled, power-save mode is not used. This bit allows OTP. Power-save mode reduces overall current consumption at the expense of accuracy, since the current is effectively assumed to be constant during the interval of voltage protection monitoring scan. Power-save mode refreshes the IADC reading only during a refreshing voltage protection reading, and it accumulates the results of the last conversions without running the ADC to obtain a new reading during the feature command ready scheduler. 0: Disabled 1: Enabled
2	R	RESERVED	N/A	Reserved. Do not change this register value.
1	R/W	CC_EN_SAFE	1’b 0	Enables Coulomb counting conversions to occur in safe mode. This bit allows OTP. 0: Disabled 1: Enabled
0	R/W (can lock to read-only)	CC_EN	1’b 0	Enables Coulomb counting accumulation. If Coulomb counting is enabled, the device cannot be in standby mode. This bit allows OTP. 0: Disabled 1: Enabled

TRIMG_IPCB (9Bh)

Format: Two’s complement

The TRIMG_IPCB command configures the current-sense PCB gain correction for the compensation of sense resistors and SMT variation.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9:0	R/W (can lock to read-only)	I_PCB_GAIN_VALUE	10’b 0000000000	The current-sense PCB gain correction can compensate for sense resistors and SMT variation. The correction is applied to both Coulomb counting and synchronous current ADC readings. It is not applied for short-circuit or over-current detection. The setting is 10-bit, complement-signed. These bits allow MTP. The gain can be calculated with the following equation: Gain (%) = Setting x 0.0244 + 100

HR_SCAN0 (9Ch)

Format: Unsigned binary

The HR_SCAN0 command enables ADC cell measurement compensation for the voltage drop caused by the cell's input resistor. It also enables voltage and current ADC scanning for the synchronous TOP current, synchronous cell current, LDOs, die temperature, NTCs, GPIO, PACKP, TOP voltage, and cell voltage.

Bits	Access	Bit Name	Default	Description
15:12	R	RESERVED	N/A	Reserved. Do not change this register value.
11	R/W	CELL_1K_COMP	1'b 0	Enables ADC cell measurement compensation for the voltage drop caused by the cell's input resistor (R_CELL_FILTER). This configuration should be enabled when the input filter resistance exceeds 500Ω. For R_CELL_FILTER values below 500Ω, this should be disabled. This bit allows OTP. 0: Disabled 1: Enabled
10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R/W (can lock to read-only)	VTOP_SYNC_EN	1'b 1	Enables the battery pack current reading, which is synchronous to the VTOP_V reading, to be updated during the high-resolution voltage ADC scan. When disabled, the synchronous VTOP_I current reading cannot be updated. This bit allows OTP. 0: Disabled 1: Enabled
8	R/W (can lock to read-only)	CELL_SYNC_EN	1'b 1	Enables the battery pack current reading, which is synchronous to each cell, to be updated during the high-resolution voltage ADC scan following the enable setting of each individual cell. When disabled, no synchronous cell current reading can be updated. This bit allows OTP. 0: Disabled 1: Enabled
7	R	RESERVED	N/A	Reserved. Do not change this register value.
6	R/W (can lock to read-only)	SCAN_LDOS_EN	1'b 0	Enables VDD, REGIN, and 3.3V readings to be updated during the high-resolution voltage ADC scan. This bit allows OTP. 0: Disabled 1: Enabled
5	R/W (can lock to read-only)	SCAN_DIE_T	1'b 1	Enables the die temperature to be updated during the high-resolution voltage ADC scan. This bit allows OTP. 0: Disabled 1: Enabled
4	R/W (can lock to read-only)	SCAN_NTCS_EN	1'b 1	Enables the NTC scans to be updated during the high-resolution voltage ADC scan, according to the enable setting of each individual NTC channel. This bit allows OTP. 0: Disabled 1: Enabled
3	R/W (can lock to read-only)	SCAN_GPIO_EN	1'b 1	Enables GPIO readings to be updated during the high-resolution voltage ADC scan, according to each individual GPIO enable setting. This bit allows OTP. 0: Disabled 1: Enabled

2	R/W (can lock to read-only)	SCAN_PACKP_EN	1'b 1	Enables the PACKP reading to be updated during the high-resolution voltage ADC scan. This bit allows OTP. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	SCAN_VTOP_EN	1'b 1	Enables the stack top voltage (C10 to AGND) reading to be updated during the high-resolution voltage ADC scan. This bit allows OTP. 0: Disabled 1: Enabled
0	R/W (can lock to read-only)	SCAN_VCELLS_EN	1'b 1	Enables the cell readings to be updated during the high-resolution voltage ADC scan, according to the enable setting of each individual cell. When disabled, the cell readings are excluded from the high-resolution voltage ADC scan. This bit allows OTP. 0: Disabled 1: Enabled

HR_SCAN1 (9Dh)

Format: Unsigned binary

The HR_SCAN1 command enables the high-resolution ADC scans for cells 1~10.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R/W	CELL_10_VI_READ_EN	1'b 1	Enables cell 10's high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0x09. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 10 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
8	R/W	CELL_9_VI_READ_EN	1'b 1	Enables cell 9's high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0x08. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 9 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
7	R/W	CELL_8_VI_READ_EN	1'b 1	Enables cell 8's high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0x07. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 8 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
6	R/W	CELL_7_VI_READ_EN	1'b 1	Enables cell 7's high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled and CELL_S_CTRL ≥ 0x06. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 7 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
5	R/W	CELL_6_VI_READ_EN	1'b 1	Enables cell 6's high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 6 is also provided. This bit allows OTP. 0: Disabled 1: Enabled

4	R/W	CELL_5_VI_READ_EN	1’b 1	Enables cell 5’s high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 5 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
3	R/W	CELL_4_VI_READ_EN	1’b 1	Enables cell 4’s high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 4 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
2	R/W	CELL_3_VI_READ_EN	1’b 1	Enables cell 3’s high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 3 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
1	R/W	CELL_2_VI_READ_EN	1’b 1	Enables cell 2’s high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 2 is also provided. This bit allows OTP. 0: Disabled 1: Enabled
0	R/W	CELL_1_VI_READ_EN	1’b 1	Enables cell 1’s high-resolution voltage scan. Effective when SCAN_VCELLS_EN is enabled. If CELL_SYNC_EN is enabled, the current reading that is synchronous with cell 1 is also provided. This bit allows OTP. 0: Disabled 1: Enabled

HR_SCAN2 (9Eh)

Format: Unsigned binary

The HR_SCAN2 command enables the ADC voltage scans for NTC1~4 and the high-resolution voltage scans for GPIO1~3.

Bits	Access	Bit Name	Default	Description
15:9	R	RESERVED	N/A	Reserved. Do not change this register value.
8	R/W (can lock to read-only)	NTC4_READ_EN	1’b 0	Enables the NTC4 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled. This bit allows OTP. 0: Disabled 1: Enabled
7	R/W (can lock to read-only)	NTC3_READ_EN	1’b 0	Enables the NTC3 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled. This bit allows OTP. 0: Disabled 1: Enabled
6	R/W (can lock to read-only)	NTC2_READ_EN	1’b 0	Enables the NTC2 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled. This bit allows OTP. 0: Disabled 1: Enabled

5	R/W (can lock to read-only)	NTC1_READ_EN	1’b 0	Enables the NTC1 high-resolution voltage scan. Effective when SCAN_NTCS_EN is enabled. This bit allows OTP. 0: Disabled 1: Enabled
4:3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R/W (can lock to read-only)	GPIO3_READ_EN	1’b 0	Enables the GPIO3 high-resolution voltage scan. Effective when SCAN_GPIO_EN is enabled. This bit allows OTP. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	GPIO2_READ_EN	1’b 0	Enables the GPIO2 high-resolution voltage scan. Effective when SCAN_GPIO_EN is enabled. This bit allows OTP. 0: Disabled 1: Enabled
0	R/W (can lock to read-only)	GPIO1_READ_EN	1’b 0	Enables the GPIO1 high-resolution voltage scan. Effective when SCAN_GPIO_EN is enabled. This bit allows OTP. 0: Disabled 1: Enabled

SILC_INFO1 (A0h)

Format: Unsigned binary

The SILC_INFO1 command defines the size of the readback (in words) before appending a CRC.

Bits	Access	Bit Name	Default	Description
15:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5:0	R/W	XFR_NUM_RD_WORDS	6’b 000001	When CRC is enabled, this register defines the size of the readback (in words) before appending a CRC. After each read transaction, this bit self-resets back to 2 bytes. 6’b000001: 1 word / 2 bytes 6’b111111: 63 words / 126 bytes

COMM_CFG (A3h)

Format: Unsigned binary

The COMM_CFG command defines the configurable device address and enables using the CRC across the communication protocol.

Bits	Access	Bit Name	Default	Description
15	R	RESERVED	N/A	Reserved. Do not change this register value.
14:8	R/W (can lock to read-only)	DEVICE_ADD	7’b 0000001	Sets the configurable device address. These bits allow MTP.
7:3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R/W (can lock to read-only)	USE_COMM_CRC	1’b 0	Enables the use of CRC across the communication protocol. This bit allows OTP. 0: Disabled 1: Enabled
1:0	R	RESERVED	N/A	Reserved. Do not change this register value.

BAL_STS (A4h)

Format: Unsigned binary

The BAL_STS command reports whether auto-balancing cycles were skipped due to a hot die temperature, a detected discharge current, a detected standby current, or a detected charge current. It also shows the number of auto-balancing cycles that are actually performed and reports whether cell-balancing is currently ongoing.

Bits	Access	Bit Name	Default	Description
15:11	R	RESERVED	N/A	Reserved. Do not change this register value.
10	R	AUTO_BAL_ SKIPPED_HOT	1’b 0	When true, auto-balancing cycles were skipped due to the die temperature being too hot. 0: False 1: True
9	R	AUTO_BAL_ SKIPPED_ DISCHARGE	1’b 0	When true, auto-balancing cycles were skipped due to a detected discharge current. 0: False 1: True
8	R	AUTO_BAL_ SKIPPED_STANDBY	1’b 0	When true, auto-balancing cycles were skipped due to a detected standby current. 0: False 1: True
7	R	AUTO_BAL_ SKIPPED_CHARGE	1’b 0	When true, auto-balancing cycles were skipped due to a detected charge current. 0: False 1: True
6:1	R	AUTO_BALANCING_ COUNT_STS	6’b 000000	Shows the number of auto-balancing cycles that are actually performed. To be valid, BAL_DONE must be set to true. If any balancing cycle is skipped, the reason can be verified by reading AUTO_BAL_SKIPPED_HOT, AUTO_BAL_SKIPPED_DISCHARGE, AUTO_BAL_SKIPPED_STANDBY, or AUTO_BAL_SKIPPED_CHARGE. This register is not updated when AUTO_BAL_ALWAYS is enabled.
0	R	BALANCING_ACTIVE	1’b 0	Reports whether cell-balancing is currently ongoing. 0: False 1: True

BAL_LIST (A5h)

Format: Unsigned binary

The BAL_LIST command reports which cell will be balanced during the next balancing session.

Bits	Access	Bit Name	Default	Description
15:10	R	RESERVED	N/A	Reserved. Do not change this register value.
9	R/W	CELL_10_TO_ BALANCE	1’b 0	When true, cell 10 will be balanced during the next balancing session. If false, cell 10 is skipped. 0: False 1: True
8	R/W	CELL_9_TO_ BALANCE	1’b 0	When true, cell 9 will be balanced during the next balancing session. When false, cell 9 is skipped. 0: False 1: True

7	R/W	CELL_8_TO_ BALANCE	1’b 0	When true, cell 8 will be balanced during the next balancing session. When false, cell 8 is skipped. 0: False 1: True
6	R/W	CELL_7_TO_ BALANCE	1’b 0	When true, cell 7 will be balanced during the next balancing session. When false, cell 7 is skipped. 0: False 1: True
5	R/W	CELL_6_TO_ BALANCE	1’b 0	When true, cell 6 will be balanced during the next balancing session. When false, cell 6 is skipped. 0: False 1: True
4	R/W	CELL_5_TO_ BALANCE	1’b 0	When true, cell 5 will be balanced during the next balancing session. When false, cell 5 is skipped. 0: False 1: True
3	R/W	CELL_4_TO_ BALANCE	1’b 0	When true, cell 4 will be balanced during the next balancing session. When false, cell 4 is skipped. 0: False 1: True
2	R/W	CELL_3_TO_ BALANCE	1’b 0	When true, cell 3 will be balanced during the next balancing session. When false, cell 3 is skipped. 0: False 1: True
1	R/W	CELL_2_TO_ BALANCE	1’b 0	When true, cell 2 will be balanced during the next balancing session. When false, cell 2 is skipped. 0: False 1: True
0	R/W	CELL_1_TO_ BALANCE	1’b 0	When true, cell 1 will be balanced during the next balancing session. When false, cell 1 is skipped. 0: False 1: True

BAL_CTRL (A6h)

Format: Unsigned binary

The BAL_CTRL command reports whether an error occurs when balancing starts or cell-balancing is completed. It also controls the start for both manual and automatic cell-balancing.

Bits	Access	Bit Name	Default	Description
15:3	R	RESERVED	N/A	Reserved. Do not change this register value.
2	R	BAL_ERROR_STS	1’b 0	Reports whether an error occurs when balancing starts (e.g. if open-wire detection is already running). 0: False 1: True
1	R	BAL_DONE_STS	1’b 0	Reports whether cell-balancing is completed. 0: False 1: True

0	R/W	BALANCE_GO	1’b 0	Controls the start for both manual and automatic cell-balancing. When set to on, balancing begins. 0: Off 1: On

BAL_CFG (A7h)

Format: Unsigned binary

The BAL_CFG command configures the number of repetitions to execute the balancing list. It also enables continuous balancing and automatic balancing.

Bits	Access	Bit Name	Default	Description
15:8	R	RESERVED	N/A	Reserved. Do not change this register value.
7:3	R/W	BAL_REPETITION	5’b 11111	Sets the number of repetitions for each execution of the balancing list. When set to 31 repetitions, 32 balancing cycles are executed. This bit allows OTP. LSB: 1 repetition Range: 0 to 31 repetitions Value (repetitions) = Setting
2	R/W (can lock to read-only)	AUTO_BAL_ALWAYS	1’b 0	This register is used only when automatic cell-balancing is enabled. When disabled, automatic cell-balancing uses BAL_REPETITION to control how many iterations the device repeats. When enabled, balancing continues until the balancing list is empty. To stop constant automatic cell-balancing before the balancing list is empty, change this bit to disabled. This bit allows OTP. 0: Disabled 1: Enabled
1	R/W (can lock to read-only)	BALANCE_MODE_REG	1’b 0	Controls the cell-balancing mode. This bit allows OTP. 0: Manual cell-balancing 1: Automatic cell-balancing
0	R/W (can lock to read-only)	BALANCE_MODE_CTRL	1’b 0	This register is used only when automatic cell-balancing is enabled. This feature is only available on I^2C versions of the MP2790. This bit allows OTP. 0: Register control (BALANCE_GO) 1: GPIO3 control (the direction of GPIO3 is set as input, and the input type is set as digital input). When set to high, balancing begins

BAL_THR (A8h)

Format: Unsigned binary

The BAL_THR command configures the cell-balancing threshold and the minimum cell voltage to run automatic cell-balancing. It also enables suspending automatic balancing if the die temperature is too hot, and it enables automatic balancing at the standby/charging current.

Bits	Access	Bit Name	Default	Description
15:13	R	RESERVED	N/A	Reserved. Do not change this register value.
12:10	R/W	BAL_MSM_TH	3’b 010	The cell-balancing threshold used by the automatic cell-balancing algorithm. These bits have OTP. LSB: 9.765mV Offset: 19.5mV Range: 19.5mV to 87.855mV Value (mV) = Setting x 9.765 + 19.5

9	R/W	STOP_ON_HOT	1’b 0	This register is used only when automatic cell-balancing is enabled. 0: Do not suspend automatic cell-balancing if the silicon digital die temperature is too hot 1: Suspend automatic cell-balancing if the silicon digital die temperature is too hot
8	R	RESERVED	N/A	Reserved. Do not change this register value.
7	R/W	ABAL_ON_STBY	1’b 0	This register is used only when automatic cell-balancing is enabled. 0: Automatic balancing does not run when the current is between 0A and the standby threshold 1: Automatic balancing can run when the current is between 0A and the standby threshold
6	R/W	ABAL_ON_CHARGE	1’b 0	This register is used only when automatic cell-balancing is enabled. 0: Automatic balancing does not run when there is a charge current that exceeds the charge standby threshold 1: Automatic balancing can run when there is a charge current that exceeds the charge standby threshold
5:0	R/W	CELL_BAL_MIN	6’b 100001	Sets the qualifying minimum cell voltage to run automatic cell-balancing. When a cell is below this level, it is excluded from the balancing list, while other qualifying cells could be balanced if they meet applicable criteria. These bits allow OTP. LSB: 39.0625mV Range: 2500mV to 4960.9375mV Value (mV) = Setting x 39.0625

MEM_STATUS (B4h)

Format: Unsigned binary

The MEM_STATUS command reports the status of the MTP.

Bits	Access	Bit Name	Default	Description
15:6	R	RESERVED	N/A	Reserved. Do not change this register value.
5:3	R	MTP_STATUS	3’b 001	Returns the thermometer-coded confirmation status of the MTP: 3’bxx1: MTP Page 1 has been fully configured, and the MTP-backed registers can be loaded and use the NVM CRC if enabled 3’bx1x: MTP Page 2 has been fully configured, and the MTP-backed registers can be loaded and use the NVM CRC if enabled 3’b1xx: MTP Page 3 has been fully configured, and the MTP-backed registers can be loaded and use the NVM CRC if enabled
2:0	R	RESERVED	N/A	Reserved. Do not change this register value.

OTP_STORE_CMD (B8h)

Format: Unsigned binary

The OTP_STORE_CMD command reports whether the store function is in progress. It also enables storing all MTP registers and the MTP CRC code in the NVM.

Bits	Access	Bit Name	Default	Description
15	R	STORE_IN_ PROGRESS	1’b 0	Reports whether the store function is in progress. 0: Storage of register data to the MTP memory is not in progress 1: Storage of register data to the MTP memory is in progress
14:4	R	RESERVED	N/A	Reserved. Do not change this register value.

3	R/W	STORE_NVM_CMD	1’b 0	Store all MTP registers and the MTP CRC code in the NVM if STORE_CMD_ACCESS_CODE has been configured with the correct code. This is a self-clearing register
2:0	R	RESERVED	N/A	Reserved. Do not change this register value.

STORE_CMD_ACCESS_CODE (B9h)

Format: Unsigned binary

The STORE_CMD_ACCESS_CODE command controls the access to the store command.

Bits	Access	Bit Name	Default	Description
15:0	R/W	STORE_CMD_ACCESS_CODE	16’b 0000000000000000	Before enabling the STORE_NVM_CMD command, 0xA5B6 must be written to this register to allow for the store command. This bit should be cleared once storage is complete.

LOCK REGISTER MAP

The MP2790 supports the configuration register lock function. This prevents critical safety settings from changing due to unforeseen circumstances.

All of the bits in an address that are not populated by a register should be treated as reserved. The value of these reserved bits may be 0 or 1, and must be set to 0 when there are write operations changing other bits in the same address. Setting these reserved bits to 0 does not change the value of the reserved bits.

Once the lock bit is set to 1, it cannot be set to 0 unless the MP2790 is reset.

All the locking bits support the MTP and the default value is 0. If the lock bit is set by the MTP to 1, the corresponding setting register cannot be modified anymore. Before the MTP command, setting the locking bit to 1 should be considered carefully.

Register Location and Bit Position for Locking	Locked Address Name and Location	Locked Field Bit Position and Name
AAh: Bit[15]	FET_MODE: 13h	Bit[11]: CHG_SOFTON_OC_LIM Bit[9]: TURNON_TIMEOUT_FAULT Bit[8]: CHG_TURNON_TIMER
	FET_CFG: 14h	Bits[14:12]: FET_DRV_LVL Bits[11:9]: CHG_SOFTON_PUP Bits[2:0]: DSG_SOFTON_DV
AAh: Bit[14]	FET_MODE: 13h	Bit[12]: P_FET_MANUAL Bit[3]: FET_ON_RUN_SC_DET_EN
AAh: Bit[13]	WDT_CFG: 10h	Bits[15:9]: WDT_BITE_CFG Bits[8:2]: WDT_BARK_CFG Bit[0]: WDT_COM_CTRL
AAh: Bit[12]	PINS_CFG: 0Dh	Bit[8]: GPIO_LV_CFG Bit[6]: WDT_RST_EN Bit[5]: WDT_RPT Bit[0]: ALERT_POL
AAh: Bit[11]	GPIO_CFG: 0Ch	Bit[10]: GPIO3_PUP Bit[9]: GPIO3_TYPE Bit[8]: GPIO3_IO Bit[6]: GPIO2_PUP Bit[5]: GPIO2_TYPE Bit[4]: GPIO2_IO Bit[2]: GPIO1_PUP Bit[1]: GPIO1_TYPE Bit[0]: GPIO1_IO
AAh: Bit[10]	LOAD_CHARGER_CFG: 09h	Bit[5]: CH_CONN_P_SBY
AAh: Bit[9]	LOAD_CHARGER_CFG: 09h	Bit[2]: LD_PLUGIN_DET_EN Bit[1]: CH_PLUGIN_DET_EN
AAh: Bit[8]	RGL_CFG: 08h	Bit[2]: V3P3_SHDN_EN
AAh: Bit[6]	STB_CFG: 06h	Bits[5:4]: STBY_MONITOR_CFG
AAh: Bit[5]	STB_CFG: 06h	Bit[6]: STBY_PFET_EN
AAh: Bit[3]	ACT_CFG: 05h	Bit[9]: FT_STATE_SEL

AAh: Bit[2]	ACT_CFG: 05h	Bit[1]: FET_CFG
AAh: Bit[1]	ACT_CFG: 05h	Bit[0]: FET_SRC
ABh: Bit[11]	TRIMG_IPCB: 9Bh	Bits[9:0]: I_PCB_GAIN_VALUE
ABh: Bit[7]	DIE_CFG: 46h	Bit[3]: DIE_TEMP_DIG_FAULT_EN
ABh: Bit[6]	DIE_CFG: 46h	Bit[1]: DIE_TEMP_DIG_EN
ABh: Bit[4]	CELLFT_CTRL: 35h	Bit[5]: CELL_OV_FAULT_EN Bit[2]: CELL_UV_FAULT_EN
ABh: Bit[3]	PACKFT_CTRL: 34h	Bit[12]: CELL_MSMT_FAULT_EN Bit[9]: CELL_DEAD_FAULT_EN Bit[5]: VTOP_OV_FAULT_EN_CTRL Bit[1]: VTOP_UV_FAULT_EN_CTRL
ABh: Bit[2]	SCFT_CTRL: 2Ah	Bit[5]: SC_CHG_FAULT_EN Bit[4]: SC_DCHG_FAULT_EN Bit[1]: SC_CHG_EN_CTRL Bit[0]: SC_DCHG_EN_CTRL
ABh: Bit[1]	OCFT_CTRL: 23h	Bit[8]: OC_CHG_FAULT_EN Bit[7]: OC2_DCHG_FAULT_EN Bit[6]: OC1_DCHG_FAULT_EN Bit[2]: OC_CHG_EN_CTRL Bit[1]: OC2_DCHG_EN_CTRL Bit[0]: OC1_DCHG_EN_CTRL
ABh: Bit[0]	INT0_EN: 19h	Bit[15]: INT_ALERT_CTRL
ACh: Bit[15]	COMM_CFG: A3h	Bits[14:8]: DEVICE_ADD
ACh: Bit[14]	COMM_CFG: A3h	Bit[2]: USE_COMM_CRC
ACh: Bit[11]	FET_MODE: 13h	Bit[4]: CHG_SOFTON_EN Bit[0]: DSG_SOFTON_EN
ACh: Bit[10]	NTC_CFG: 47h	Bit[15]: PCB_MNTR_FAULT_EN
ACh: Bit[9]	NTC_CFG: 47h	Bit[14]: NTC_CELL_DSG_FAULT_EN Bit[13]: NTC_CELL_CHG_FAULT_EN
ACh: Bit[8]	NTC_CFG: 47h	Bit[10]: NTCB_DYNAMIC_ON
ACh: Bit[7]	NTC_CFG: 47h	Bit[7]: NTC4_TYPE_SEL
ACh: Bit[6]	NTC_CFG: 47h	Bit[6]: NTC4_EN
ACh: Bit[5]	NTC_CFG: 47h	Bit[5]: NTC3_TYPE_SEL
ACh: Bit[4]	NTC_CFG: 47h	Bit[4]: NTC3_EN
ACh: Bit[3]	NTC_CFG: 47h	Bit[3]: NTC2_TYPE_SEL
ACh: Bit[2]	NTC_CFG: 47h	Bit[2]: NTC2_EN
ACh: Bit[1]	NTC_CFG: 47h	Bit[1]: NTC1_TYPE_SEL
ACh: Bit[0]	NTC_CFG: 47h	Bit[0]: NTC1_EN
ADh: Bit[15]	CELL_UV: 38h	Bits[11:8]: CELL_UV_DG Bits[7:0]: CELL_UV
ADh: Bit[14]	CELL_OV: 39h	Bits[11:8]: CELL_OV_DG Bits[7:0]: CELL_OV

ADh: Bit[13]	NTCC_OTHR_DSG: 48h	Bits[9:0]: NTC_CELL_HOT_DSG
	NTCC_UTHR_DSG: 49h	Bits[9:0]: NTC_CELL_COLD_DSG
	NTCC_OTHR_CHG: 4Ah	Bits[9:0]: NTC_CELL_HOT_CHG
	NTCC_UTHR_CHG: 4Bh	Bits[15:11]: NTC_CELL_HYST Bits[9:0]: NTC_CELL_COLD_CHG
ADh: Bit[10]	CELLS_CTRL: 00h	Bits[3:0]: CELL_S_CTRL
ADh: Bit[9]	SELF_CFG: 56h	Bit[15]: OTP_FAULT_EN
ADh: Bit[8]	SELF_CFG: 56h	Bit[14]: 3V3_VDD_FAULT_EN
ADh: Bit[7]	SELF_CFG: 56h	Bit[10]: OPEN_WIRE_PON
ADh: Bit[6]	SELF_CFG: 56h	Bit[9]: OPEN_WIRE_FAULT_EN
ADh: Bit[4]	SELF_CFG: 56h	Bit[6]: OTP_CRC_EN
ADh: Bit[3]	SELF_CFG: 56h	Bit[3]: ADC_SELF_TEST_EN
ADh: Bit[2]	SELF_CFG: 56h	Bit[2]: VDD_EN
ADh: Bit[1]	SELF_CFG: 56h	Bit[1]: 3V3_EN
ADh: Bit[0]	SELF_CFG: 56h	Bit[0]: REGIN_EN
AEh: Bit[15]	DSGSC_CFG: 2Bh	Bits[14:8]: SC_DCHG_DG Bit[5]: SC_DCHG_RNG Bits[4:0]: SC_DCHG_LIM
AEh: Bit[14]	CHGSC_CFG: 2Ch	Bits[14:8]: SC_CHG_DG Bit[5]: SC_CHG_RNG Bits[4:0]: SC_CHG_LIM
AEh: Bit[13]	DSGOC_LIM: 24h	Bit[13]: OC2_DCHG_RNG Bits[12:8]: OC2_DCHG_LIM
	DSGOC_DEG: 25h	Bit[14]: OC2_DCHG_DGL_RNG Bits[13:8]: OC2_DCHG_DGL
AEh: Bit[12]	DSGOC_LIM: 24h	Bit[5]: OC1_DCHG_RNG Bits[4:0]: OC1_DCHG_LIM
	DSGOC_DEG: 25h	Bit[6]: OC1_DCHG_DGL_RNG Bits[5:0]: OC1_DCHG_DGL
AEh: Bit[11]	CHGOC_DEG: 26h	Bit[14]: OC_CHG_DGL_RNG Bits[13:8]: OC_CHG_DG Bit[5]: OC_CHG_RNG Bits[4:0]: OC_CHG_LIM
AEh: Bit[9]	FT_REC: 60h	Bit[12]: DIE_TEMP_FAULT_REC
AEh: Bit[2]	FT_REC: 60h	Bit[4]: PCB_MNTR_REC
AEh: Bit[1]	FT0_CFG: 61h	Bit[11]: CELL_OV_REC Bit[7]: CELL_UV_REC
AEh: Bit[0]	FT_REC: 60h	Bit[2]: NTC_CELL_CHG_REC Bit[1]: NTC_CELL_DSG_REC
AFh: Bit[7]	FT0_CFG: 61h	Bit[10]: CELL_OV_FAULT_ACTION
AFh: Bit[6]	FT0_CFG: 61h	Bit[9]: CELL_OV_LOGIC_SEL
AFh: Bit[5]	FT0_CFG: 61h	Bit[9]: CELL_OV_CHG_REC_MODE

AFh: Bit[4]	FT0_CFG: 61h	Bit[6]: CELL_UV_FAULT_ACTION
AFh: Bit[3]	FT0_CFG: 61h	Bit[5]: CELL_UV_LOGIC_SEL
AFh: Bit[2]	FT0_CFG: 61h	Bit[4]: CELL_UV_DSG_REC_MODE
AFh: Bit[0]	FT0_CFG: 61h	Bit[0]: NTC_CELL_CHG_ACTION
B0h: Bit[15]	PACKFT_CTRL: 34h	Bit[8]: CELL_DEAD_EN
B0h: Bit[13]	CELLFT_CTRL: 35h	Bit[4]: CELL_OV_EN_CTRL Bit[1]: CELL_UV_EN_CTRL
B0h: Bit[11]	BAL_CFG: A7h	Bit[2]: AUTO_BAL_ALWAYS
B0h: Bit[10]	BAL_CFG: A7h	Bit[1]: BALANCE_MODE_REG
B0h: Bit[9]	BAL_CFG: A7h	Bit[0]: BALANCE_MODE_CTRL (I^2C versions only)

APPLICATION INFORMATION

PCB Layout Guidelines

Proper PCB layout is critical to reduce noise, and to optimize the device's accuracy and reliability. For the best results, refer to Figure 23, Figure 24, and Figure 25, and follow the guidelines below:

1. Route the ground plane such that it reduces ground noise and prevents stray current (see Figure 23).

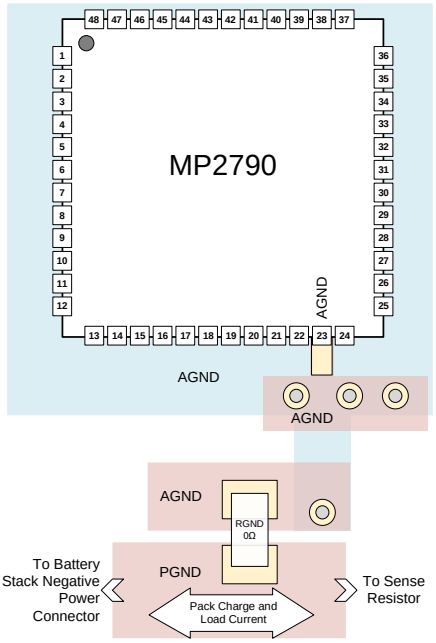


Figure 23: Recommended Layout for AGND

2. Connect the AGND pin to a dedicated ground plane. Then connect the AGND plane to the negative terminal of the battery stack via a 0Ω resistor.
3. Review the schematic and layout to ensure that each component is connected to the correct ground (power vs. signal). For example, the diodes protecting the different power terminals should be connected to PGND.
4. Consider the expected maximum peak load current, then check the PGND length, width, and thickness to ensure that there is an appropriate low-resistance path that prevents voltage drops.
5. The REGIN, VDD, VREF, 3V3, and NTCB pins require external decoupling capacitors, which should be placed as close as possible to each pin. Minimize the trace inductance from these pins to AGND (see Figure 24).

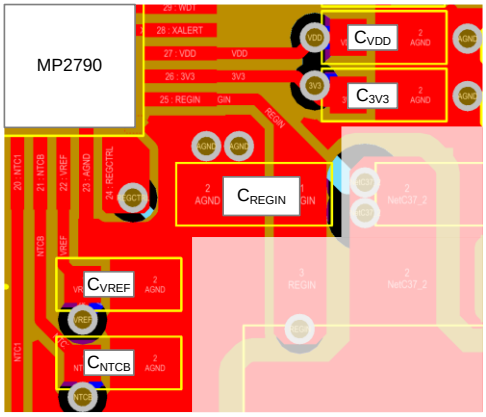


Figure 24: Recommended Layout for Decoupling Capacitors

6. Consider Kelvin connections at the sense resistor. A sense resistor with a dedicated sensing pad is ideal. A simple two-terminal sense resistor can be used in a 4-wire sensing configuration (see Figure 25).
7. Route the sensing signals to SRP and SRN in parallel to avoid coupling interfering signals.

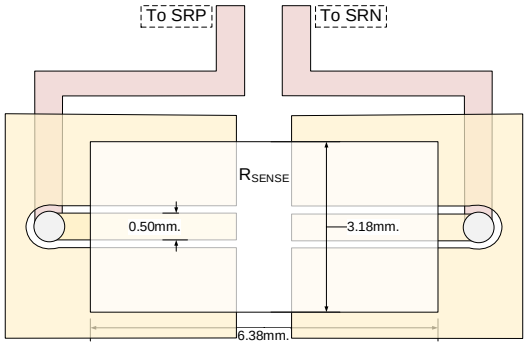


Figure 25: 2512 Sense Resistor using 4-Wire Footprint

8. Connect the temperature sensors (NTCx) to AGND using the star connection technique to avoid contaminating the voltage reading with the resistive voltage drop caused by the load or charging ground current.
9. Route the two wires connecting the NTCx pins together in twisted pairs to avoid coupling interfering signals. This is recommended if NTCx is located off-board.

TYPICAL APPLICATION CIRCUITS

Figure 26 shows the typical external components and connections required to interface the MP2790 to the battery pack and the one-port system.

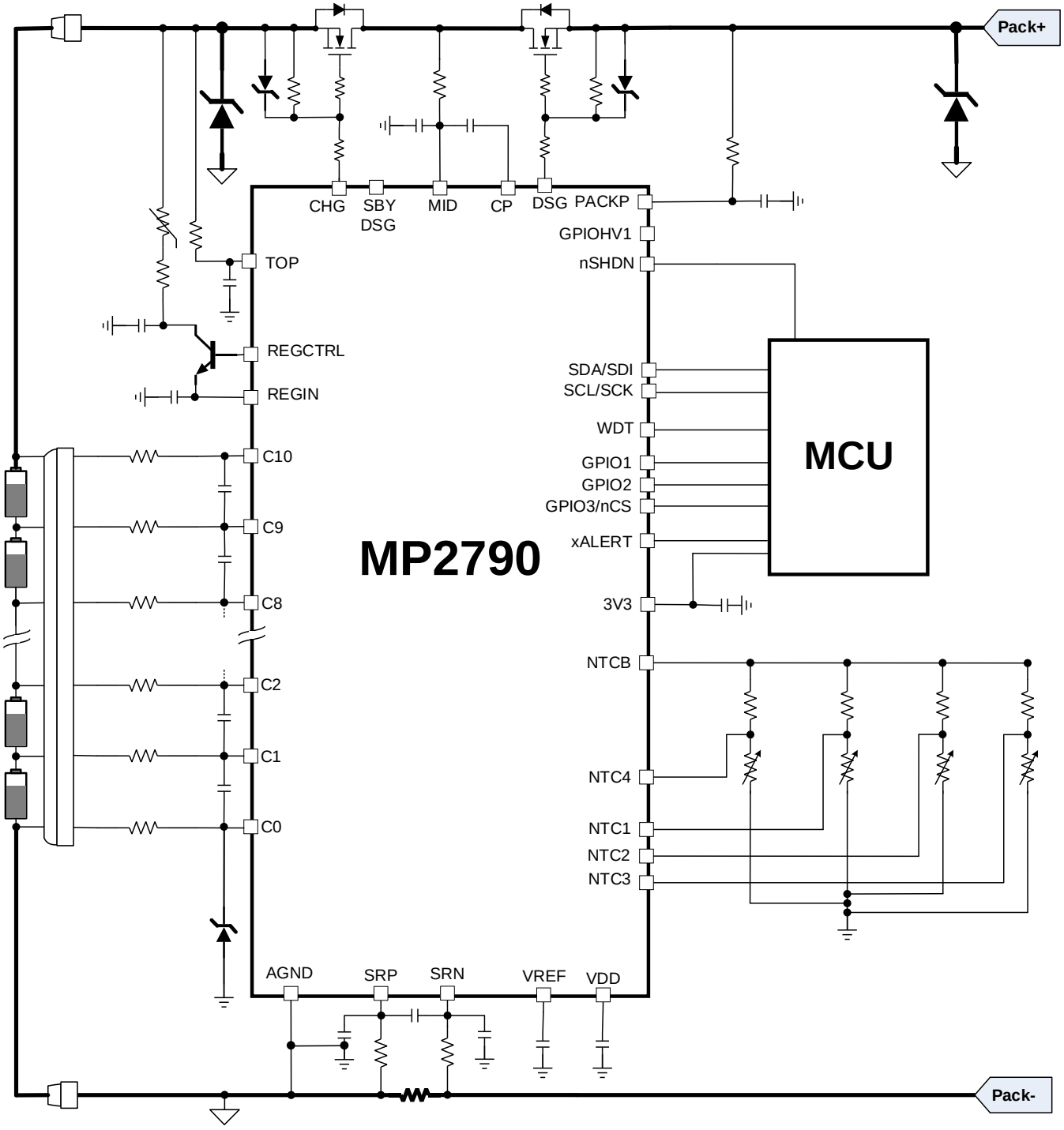


Figure 26: One-Port Application Circuit for the MP2790

Figure 27 shows the typical external components and connections required to interface the MP2790 to the battery pack and the separate port system.

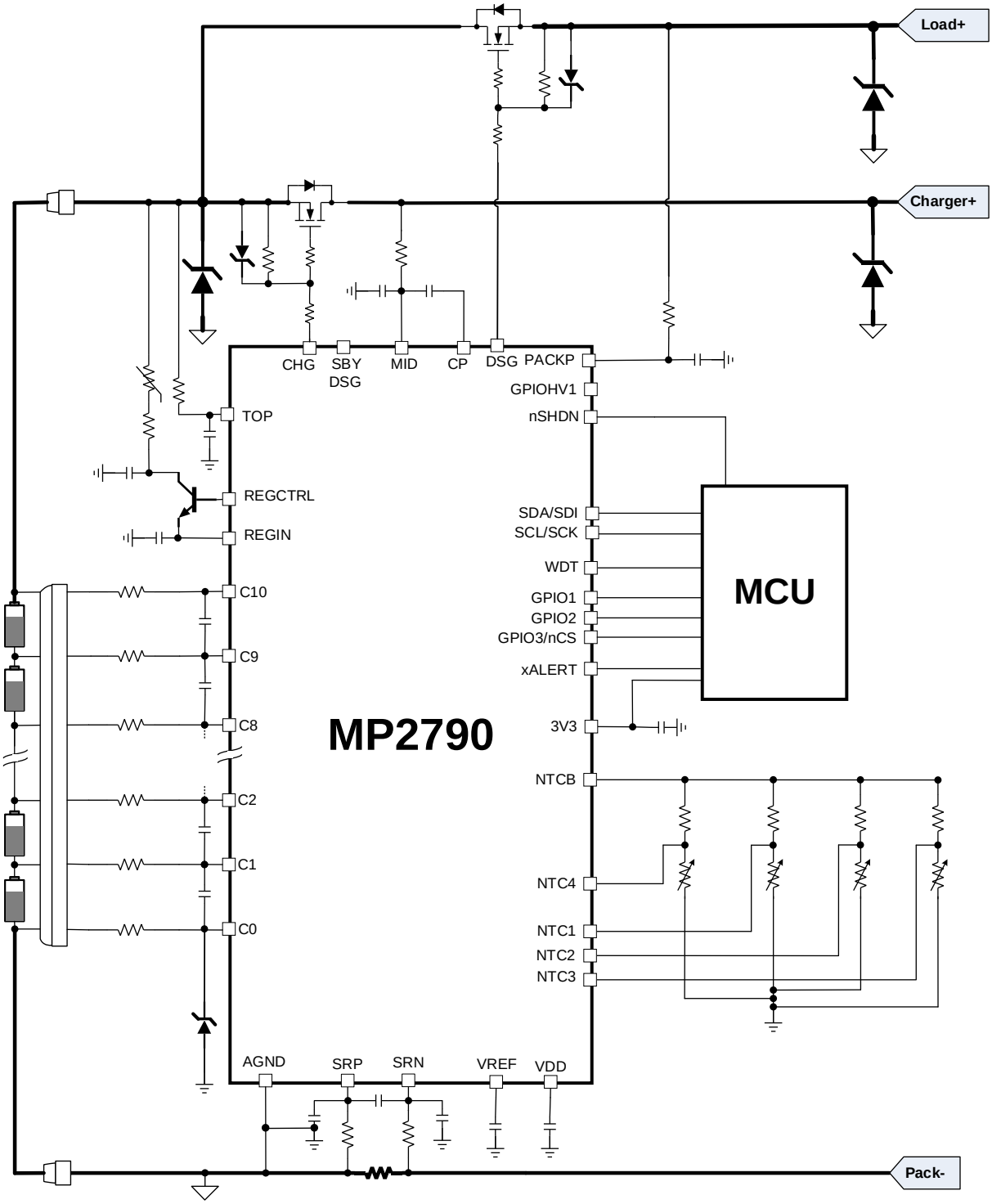


Figure 27: Separate Port Application Circuit for the MP2790

Recommended External Components

Figure 28 shows a detailed view of all of the typical recommended external components.

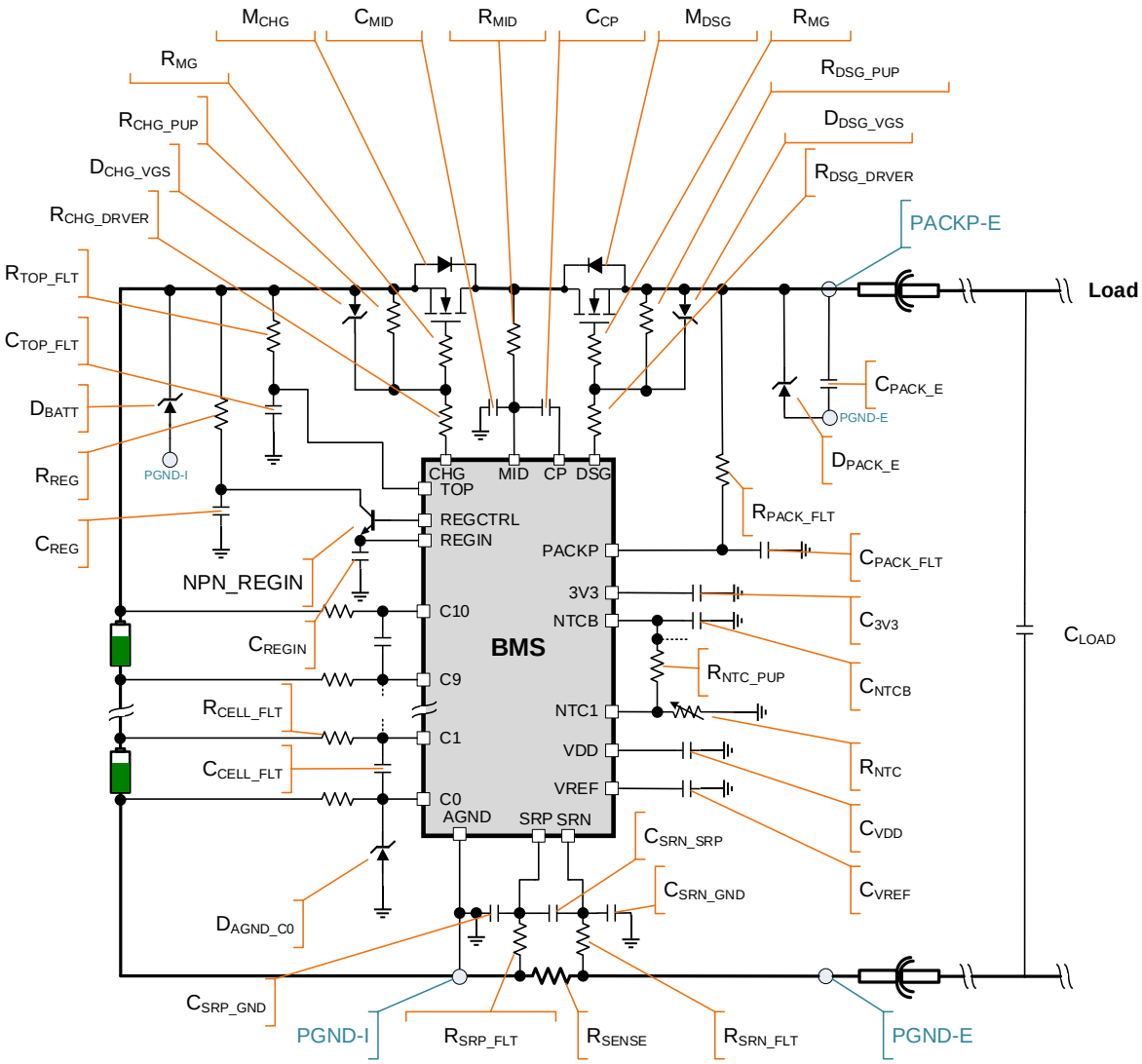


Figure 28: Recommended External Component Diagram

Table 15 on page 138 provides guidance regarding which parameters should be evaluated when selecting each BOM component (see the Configuration for External or Internal Cell-Balancing section on page 140 for more details on cell-balancing). Refer to the MP2790 evaluation board datasheet to see each BOM component.

Table 15: Recommended Components

Parameter Identifier	Parameter Description	Component Description	Parameter Comments	Min	Typ	Max	Unit
General							
$D_{AGND-C0}$	Recommended Zener diode voltage rating	AGND-C0 Zener diode voltage			3.3		V
C_{PACK_E}	Capacitance value	External pack capacitor			47	200	µF
Pin Filtering							
C_{TOP_FLT}	Required capacitance	TOP-filtering capacitor			470		nF
R_{TOP_FLT}	Required resistance	TOP-filtering resistor			20		Ω
C_{PACK_FLT}	Required capacitance	PACKP-filtering capacitor	If R_{PACK_FLT} increases, C_{PACK_FLT} should be proportionally decreased.		10		nF
R_{PACK_FLT}	Required resistance	PACKP-filtering resistor			100		Ω
R_{MID}	Required resistance	MID-filtering resistor			100		Ω
Cell Voltage Sensing							
C_{CELL_FLT}	Required capacitance	Cell-filtering capacitor			100		nF
R_{CELL_FLT}	Required resistance	Cell-filtering resistor		20	100		Ω
N-Channel MOSFET Driver							
$D_{CHG-VGS}$	Recommended Zener diode voltage rating	Diode CHG V_{GS} protection	For a CHG N-channel MOSFET with a ±20V maximum V_{GS}. If the CHG N-channel MOSFET has a smaller V_{GS}, decrease the Zener voltage value accordingly.		16		V
$D_{DSG-VGS}$	Recommended Zener voltage rating	Diode DSG V_{GS} protection	For a DSG N-channel MOSFET with a ±20V maximum V_{GS}. If the DSG N-channel MOSFET has a smaller V_{GS}, decrease the Zener voltage accordingly.		16		V
R_{CHG_PUP}	Recommended resistance	N charge MOSFET pull-up resistor			10		MΩ
R_{DSG_PUP}	Recommended resistance	N discharge MOSFET pull-up resistor			10		MΩ
R_{CHG_DRVER}	Required resistance	N-channel MOSFET charge driver protection resistor			100		Ω
R_{DSG_DRVER}	Required resistance	N-channel MOSFET discharge driver protection resistor			100		Ω
R_{MG}	Required resistance	N-channel MOSFET gate protection resistor			100		Ω
Current Sensing							
R_{SRN_FLT}	Recommended resistance	SRN filtering resistor			100		Ω
C_{SRN_GND}	Recommended capacitance	SRN-GND filtering capacitor			100		nF

C_{SRN_SRP}	Recommended capacitance	SRN/P differential filtering capacitor			100		nF
R_{SRP_FLT}	Recommended resistance	SRP filtering resistor			100		Ω
C_{SRP_GND}	Recommended capacitance	SRP-GND filtering capacitor			100		nF
R_{SENSE}	Recommended resistance	Pack current-sense resistor	The min and max values are recommended, and are based on the current-sense range.	0.1	2	5	mΩ
Regulators							
C_{3V3}	Required capacitance	3.3V capacitor		0.47	1	10	µF
C_{CP}	Required capacitance	CP to MID capacitor			47		nF
	Required voltage rating		The rating can be proportionally reduced if fewer than 10 stacked cells are used.	80			V
C_{VDD}	Required capacitance	VDD bypass capacitor			1		µF
C_{MID}	Required capacitance	MID bypass capacitor			100		nF
C_{VREF}	Required capacitance	VREF bypass capacitor			1		µF
C_{REGIN}	Required capacitance	REGIN capacitor			3.3		µF
C_{REG}	Required capacitance	Regulator capacitor			1		µF
R_{REG}	Regulator-limiting resistor value	Regulator-limiting resistor value			500		Ω
Temperature Sensing							
R_{NTC_PUP}	Typical resistance	NTC pull-up	This is a typical value. Generally, the NTC pull-up value should match the NTC thermistor value at 25°C.		10		kΩ
R_{NTC}	Typical resistance	NTC thermistor	If a smaller resistance is used, the NTCB current limit should be evaluated and compared to the total resistance connected to the NTCB in the worst-case scenario (hot temperatures).		10		kΩ
C_{NTCB}	NTCB capacitance	NTCB capacitor				10	nF

Configuration for External or Internal Cell-Balancing

Cell-balancing can be implemented via the internal balancing MOSFETs for up to 58mA. Higher cell-balancing current is possible with external MOSFETs or BJTs (see Figure 29).

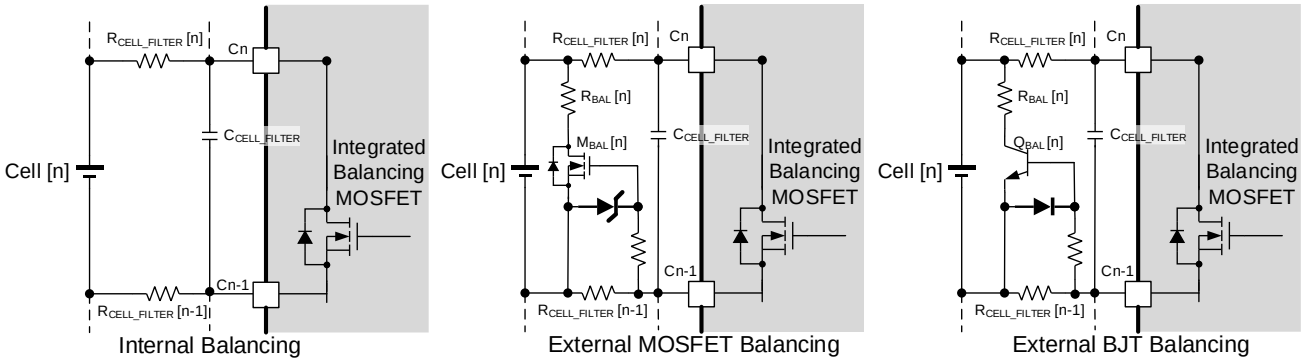


Figure 29: Typical Schematics Internal vs. External Balancing Configurations

Table 16 recommends specific components for internal MOSFET balancing.

Table 16: Recommended Component Selection for Internal MOSFET Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for internal balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		100		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for the internal balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	20	100	200	Ω

The amount of current provided in an internal balancing configuration is easily derived by following the R_{CELL_FILTER} resistor value and considering the integrated MOSFET balancing resistance ($R_{DS(ON)\_BAL\_FET}$). For example, for a lithium cell at 4V where R_{CELL_FILTER} = 20Ω, the resistive path allows for 58mA once the integrated balancing resistor MOSFET is enabled.

For higher balancing current, Table 17 and Table 18 on page 141 provide guidance on selecting the MOSFET or BJT circuit components.

Table 17 recommends specific components for external MOSFET balancing.

Table 17: Recommended Component Selection for External MOSFET Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		10		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	800	1000	1100	Ω
R_{BAL}	Required resistance	Cell-balancing current-limiting resistor	Adjust this value to set the balancing current, and verify the power dissipation compared to package limit.		43		Ω
V_{TH_MBAL}	MOSFET V_{GS} threshold	External balancing MOSFET M_{BAL}	A higher voltage threshold may prevent the MOSFET from turning on.		1.5	1.8	V

The external balancing MOSFETs should be selected using Table 17 on page 140. Choose a MOSFET with a sufficiently low V_{GS} threshold. For simplification, assume that the integrated MOSFET-balancing resistance can be ignored. The available V_{GS} that turns on the MOSFET is generated across R_{CELL_FILTER}, meaning its voltage is half of the lithium cell voltage (e.g. 4.2V/2 = 2.1V). In this scenario, the V_{GS} threshold for M_{BAL} should be below 2.1V with an appropriate safety margin. The safety margin should allow for voltage drops on the integrated MOSFET balancing resistor. This drop can be caused by the following:

- Changes in the operating conditions
- Shifts in the M_{BAL} V_{GS} threshold across operating conditions
- Drops that develop across the sensing wires due to the balancing current

Table 18 recommends specific components for external BJT balancing.

Table 18: Recommended Component Selection for External BJT Balancing

Parameter Identifier	Parameter Description	Component Description	Notes	Min	Typ	Max	Unit
C_{CELL_FILTER}	Required capacitance	Cell-filtering capacitor	Capacitance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.		100		nF
R_{CELL_FILTER}	Required resistance	Cell-filtering resistor	Resistance for external balancing configuration. If R_{CELL_FILTER} increases, C_{CELL_FILTER} should be proportionally decreased.	20	100	1100	Ω
R_{BAL}	Required resistance	Cell-balancing current-limiting resistor	Adjust this value to set the balancing current, and verify the power dissipation compared to package limit.		43		Ω
h_{FE_QBAL}	BJT DC current gain	External balancing BJT Q_{BAL}	A lower h_{EF} may limit the external balancing current.	50			

Because R_{BAL} sets the balancing current and dissipates most of the power, ensure that an appropriate resistor and resistor package are selected, especially for resistors below 100Ω. For example, if R_{BAL} = 43Ω, there is 410mW of power dissipation when the lithium cell voltage = 4.2V. This means that a package of at least 2512 (6432 Metric) should be used.

It is also important to consider the thermal design of the overall board and enclosure. The MP2790 can simultaneously balance only odd or even cells, meaning 5 cells in a 10-cell system. When balancing is run continuously on 5 cells, 2.05W is dissipated as heat with a 43Ω R_{BAL}. To keep the MP2790 in the allowed temperature range, consider how this additional heat can be dissipated, as it is added to the amount of heat generated by other components.

Selecting the CP Capacitor

When multiple MOSFETs in parallel are used for DSG or CHG, the CP capacitance should be selected to avoid causing an excessive voltage drop while the MOSFETs turn on. Table 19 lists values for the CP capacitor depending on the total C_{ISS} that the DSG or CHG MOSFET driver must drive. The total C_{ISS} was obtained from the MOSFET datasheets.

Design the number of parallel DSG MOSFETs to match the number of parallel CHG MOSFETs. If 4 parallel DSG MOSFETs are used, then the individual MOSFET's C_{ISS} should be multiplied by 4, and the resulting C_{ISS} value should be used.

Table 19: CP Capacitor Selection

C_{CP}	Total C_{ISS}
47nF	47nF
68nF	68nF
100nF	100nF

Unused Pins

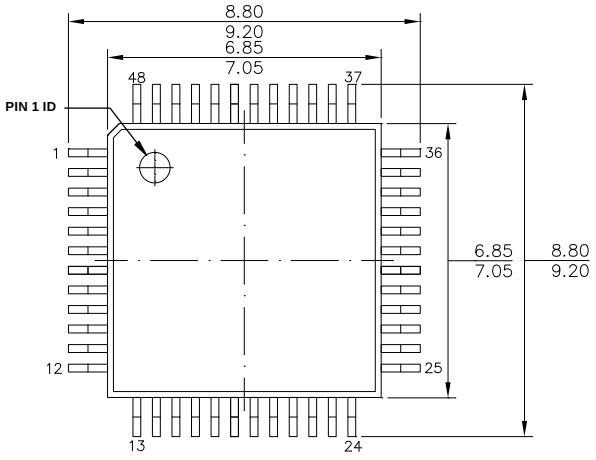
For a particular application, some pins may not be needed. Table 20 shows how to connect these pins when they are not used.

Table 20: Unused Pins Connection

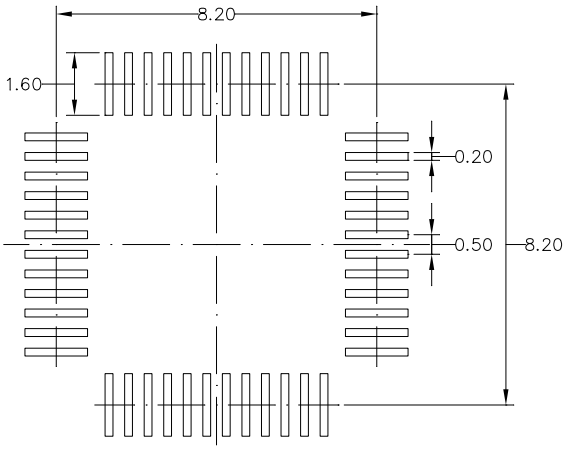
Pin #	Name	Recommendation
1–8, 46–48	C6 to C10	If fewer than 10 series cells are used, directly connect all upper unused cell channels to the practical maximum cell channel. For example, if only 8 cells are used, C10~C8 should be connected together.
12–14	C0 to C2	If fewer than 6 series cells are used, directly connect all upper unused cell channels to the practical maximum cell channel and connect all low unused cell channels to the practical minimum cell channel. For example, if only 4 cells are used, C10~C6 should be connected together and C0~C2 should be connected together.
15, 16	SRP, SRN	If the current-sense function is not required, connect these pins to AGND.
17–20	NTC1, NTC2, NTC3, NTC4	Float the unused NTC channels.
21	NTCB	If NTC temperature monitoring is not used, float this pin.
28	XALERT	Float this pin if it is not used.
29	WDT	Float this pin if it is not used.
33	SDO	Float this pin if it is not used.
34	GPIO3/nCS	Float this pin if it is not used. Note that the GPIO3 should be set to 20kΩ pull-up mode by the GPIO_CFG register; otherwise there may be additional power consumption.
35, 36	GPIO1, GPIO2	Float this pin if it is not used. Note that the unused GPIO should be set to 20kΩ pull-up mode by the GPIO_CFG register; otherwise there may be additional power consumption.
37	GPIOHV1	Float this pin if it is not used.
38	PACKP	If the DSG MOSFET driver is not used, and the PACKP vs. TOP comparator is not needed, connect this pin to TOP.
39	DSG	If the HS-FET drivers are not used and normal mode is required, connect this pin to PACKP via a 100Ω resistor and a 1nF capacitor. If normal mode is not required, float this pin.
41	SBYDSG	Float this pin if it is not used.
42	CP	If the HS-FET drivers are not used and normal mode is required, connect this pin to MID via a 47nF CP capacitor. If normal mode is not required, float this pin.
43	MID	If the HS-FET drivers are not used, connect this pin to TOP.
44	CHG	If the HS-FET drivers are not used and normal mode is required, connect this pin to TOP via a 100Ω resistor and a 1nF capacitor. If normal mode is not required, float this pin.

PACKAGE INFORMATION

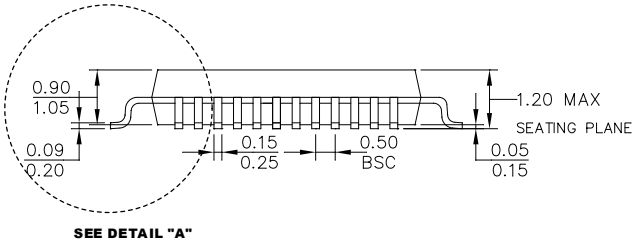
TQFP-48 (7mmx7mm)



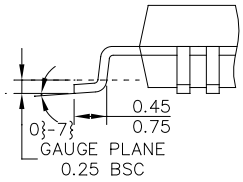
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

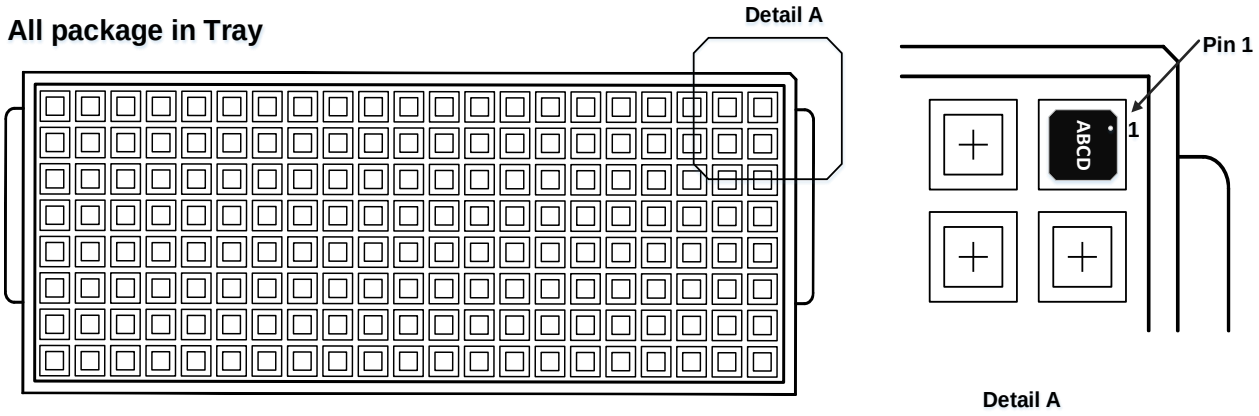


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-143.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2790DFP-xxxx-T	TQFP-48 (7mmx7mm)	N/A	N/A	250pcs	N/A	N/A	N/A

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/22/2023	Initial Release	-
1.1	5/14/2024	Full rewrite; all key content updated (14)	All

Note:

14) Contact an MPS FAE for more information.