MP2659

36V, Standalone Switching Charger with Integrated MOSFETs for 3-Cell to 6-Cell Series Battery Pack

DESCRIPTION

The MP2659 is a highly integrated switching charger designed for portable devices with 3-cell to 6-cell series Li-ion or Li-polymer battery packs. The device achieves up to 3A of charge current with different battery regulation voltages.

The device operates under a maximum 36V DC input voltage and hold-off up to 45V. When an input power supply is present, the MP2659 charges the battery with three phases: pre-charge, constant current charge, and constant voltage charge.

Power management is based on the input current and input voltage. If the input current exceeds the preset input current limit, or the input voltage decreases to the preset input voltage limit, the MP2659 automatically decreases the charge current to protect the input power supply from overload.

To guarantee safe operation, the MP2659 offers robust protection features such as battery over-voltage protection, battery temperature sensing and protection, thermal shutdown, and a charging safety timer.

The MP2659 is available in a QFN-19 (3mmx3mm) package.

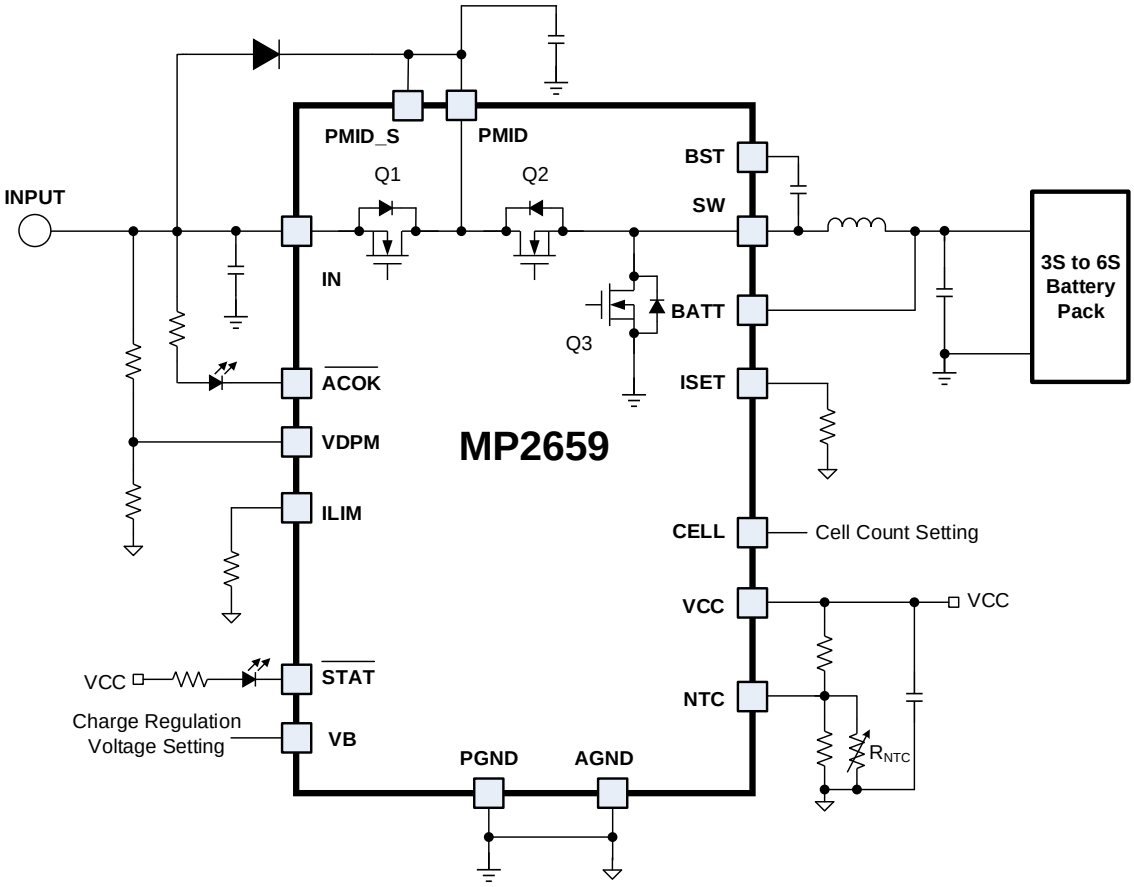
FEATURES

- Up to 36V Operating Input Voltage
- 45V Max Sustainable Voltage when Not Switching
- Up to 3A Charge Current
- 3-Cell to 6-Cell Series with 3.6V/4.2V/4.35V /4.15V Battery Regulation Voltage for Each Cell
- 0.5% Battery Regulation Voltage Accuracy
- Integrated Input Current Sensing and Reverse Blocking FET
- Internal Loop Compensation
- Input Current Limit Regulation
- Minimum Input Voltage Regulation
- Charge Operation Indicator
- Dead Battery Pack Recovery
- Battery Over-Voltage Protection
- Charge Safety Timer
- Battery NTC Thermal Monitor
- Available in a QFN-19 (3mmx3mm) Package

APPLICATIONS

- Industrial Medical Equipment
- Power Tools
- Robots and Portable Vacuum Cleaners
- Wireless Speakers

TYPICAL APPLICATION



Typical Application

CELL Pin Connection	Battery Cell Counts
AGND	3-Cell Series
Float	4-Cell Series
Pull up to VCC	5-Cell Series
100kΩ resistor to AGND	6-Cell Series

VB Pin Connection	Charge Regulation Voltage
AGND	3.6V
Float	4.2V
Pull up to VCC	4.35V
100kΩ resistor to AGND	4.15V

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2659GQ-xxxx**	QFN-19 (3mmx3mm)	*See Below*	1
EV2659-Q-02A	Evaluation kit	N/A	

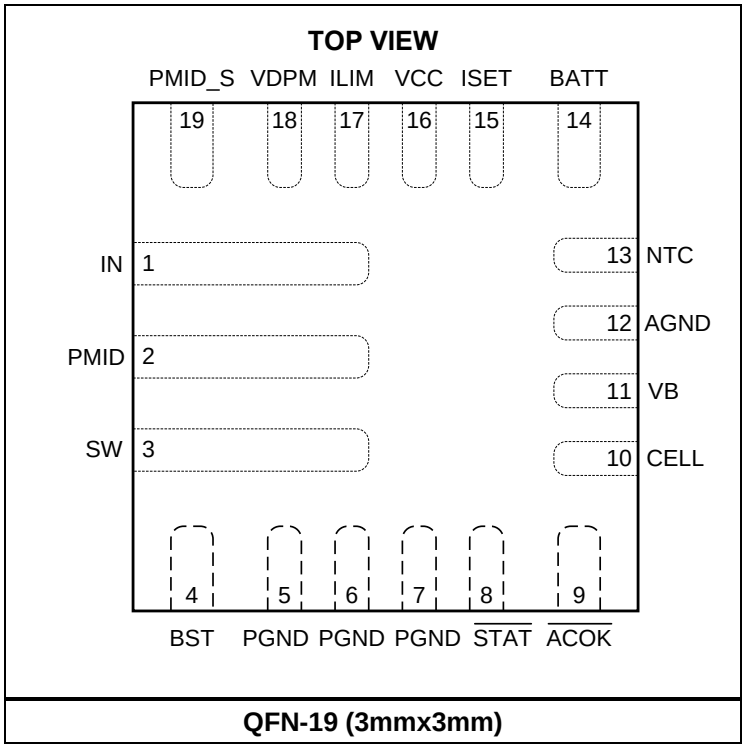
* For Tape & Reel, add suffix –Z (e.g. MP2659GQ-xxxx–Z).
** "xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I^2C register map. Contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

BFLY
LLL

BFL: Product code of MP2659GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-19 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
1	IN	Power	**Power input.** Place a 1µF capacitor from IN to PGND. See Application Section for capacitor and voltage clamping recommendation
2	PMID	Power	**Decoupling capacitor of the power stage.** Bypass it with a ceramic 2.2µF capacitor from PMID to PGND, placed as close as possible to the IC with the shortest route. A 2A/40V schottky diode is required from IN pin to PMID pin.
3	SW	Power	**Switching node.**
4	BST		**Bootstrap pin.** Connect a 100nF bootstrap capacitor between the BST and SW pins to form a floating supply to drive the high-side MOSFET above the supply voltage.
5, 6, 7	PGND	Power	**Power ground.**
8	$\overline{\text{STAT}}$	O	**Status indication.** This pin acts as the indicator for charging operation status and fault status with an open-drain output (see Table 3).
9	$\overline{\text{ACOK}}$	O	**Input valid indication.** Open-drain output, active low.
10	CELL	I	**Battery cell number selection.**
11	VB	I/O	**Battery regulation voltage setting.**
12	AGND	Power	**Analog ground.** Short to PGND on PCB.
13	NTC	I	**Temperature-sense input.** Connect a negative temperature coefficient thermistor to NTC. The hot and cold temperature window can be configured with a resistor divider from VCC to NTC to AGND. Charging suspends when the NTC pin voltage is out of range.
14	BATT	Power	**Battery positive terminal.** Place a minimum 10µF capacitor from BATT to PGND. See Application Section for capacitor and voltage clamping recommendation
15	ISET	I	**Charging current setting.** Connect a resistor to AGND.
16	VCC	I	**Internal circuit power supply.** Bypass to AGND with a 1µF ceramic capacitor. When an input source is present, a 5V output is generated on the VCC pin.
17	ILIM	I	**Input current limit setting.** Connect a resistor to AGND.
18	VDPM	I	**Input voltage clamp setting.** Connect to a resistor divider from IN to AGND. This pin also can be used to disable charging when pulled down to logic low (below 0.2V).
19	PMID_S	I	**PMID voltage-sense input.** Short to the PMID pin.

ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID, PMID_S, $\overline{ACOK}$, BATT to PGND…….....-0.3V to +45V
SW to PGND.....-0.3V(-2V for 20ns) to +45V
BST to PGND…….. .....SW to SW + 5.5V
All other pins to AGND.....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2)
..... 2.5W
Junction temperature……150°C
Lead temperature (solder) .....260°C
Storage temperature…….. -65°C to +150°C

ESD Rating

Human body model (HBM) (3)..... 2000V
Charged device model (CDM) (4)..... 750V

Recommended Operating Conditions (5)

Supply voltage (V_{IN}) .....4.5V to 36V
Input current (I_{IN}).....Up to 3A
Charge current (I_{CHG}) .....Up to 3A
Battery voltage (V_{BATT}) .....Up to 26.1V
Operating junction temp (T_J).... -10°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-19 (3mmx3mm) .....50.....12.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per ANSI/ESDA/JEDEC JS-001.
4) Per JESD22-C101.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, 4-cell, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristic						
IN under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.3	3.6	3.9	V
IN UVLO threshold hysteresis		V_{IN} rising		420		mV
IN vs. BATT headroom	V_{HDRM}	V_{IN} rising	1.4	1.9	2.4	V
		V_{IN} falling	1.1	1.5	1.9	V
DC/DC Converter						
Input shutdown current	I_{IN_SHDN}	V_{IN} = 36V, VDPM = AGND,		550		µA
Input quiescent current	I_{IN_Q}	V_{IN} = 36V, charge is enabled, 4-cell, charge termination		1		mA
VCC LDO output voltage	V_{VCC}	V_{IN} = 24V	4.85	5	5.2	V
VCC LDO output current limit			50			mA
Blocking FET on resistance	R_{ON_Q1}			40		mΩ
HS-FET on resistance	R_{ON_Q2}			40		mΩ
LS-FET on resistance	R_{ON_Q3}			56		mΩ
Peak current limit for high-side MOSFET (HS-FET) (Q2)	I_{HS_PK}	CC charge mode	4.8	5.4	6	A
		Pre-charge mode		3.4		A
Valley current limit for low-side MOSFET (LS-FET) (Q3)	I_{LS_VL}	CC charge mode		3.9		A
Negative current limit for LS-FET (Q3)	I_{LS_ZCD}		-1.6	-1.25	-0.9	A
Switching frequency	f_{SW}	f_{SW} = 680kHz	580	680	790	kHz
		f_{SW} = 350kHz	290	350	420	kHz
Battery Charger						
Pre-charge to fast-charge threshold	V_{BATT_PRE}	VB set to 4.2V/4.35V/4.15V	2.9	3	3.1	V/cell
		VB set to 3.6V	2.4	2.5	2.6	V/cell
Pre-charge voltage hysteresis		VB set to 4.2V, CELL set to 4		1.2		V
Battery short-circuit threshold	V_{BATT_SRT}	VB set to 4.2V, CELL set to 4	1.4	1.5	1.6	V/cell

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, 4-cell, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Battery charge voltage regulation	V_{BATT_REG}	VB set to 3.6V, CELL set to 3	10.746	10.8	10.854	V
		VB set to 4.2V, CELL set to 3	12.537	12.6	12.663	
		VB set to 4.2V, CELL set to 4	16.716	16.8	16.884	
		VB set to 4.2V, CELL set to 5	20.895	21	21.105	
		VB set to 4.2V, CELL set to 6	25.074	25.2	25.326	
		VB set to 4.35V, CELL set to 3	12.985	13.05	13.115	
		VB set to 4.35V, CELL set to 4	17.313	17.4	17.487	
		VB set to 4.35V, CELL set to 5	21.641	21.75	21.859	
		VB set to 4.35V, CELL set to 6	25.970	26.1	26.231	
		VB set to 4.15V, CELL set to 6	24.77	24.9	25.03	
Battery charge termination current	I_{TERM}	I_{TERM} = 200mA	100	200	300	mA
		I_{TERM} = 100mA	60	110	160	mA
Battery termination deglitch time	t_{TERM_DGL}			50		ms
Recharge threshold	V_{RECH}	V_{RECH} = 250mV/cell	200	250	300	mV/cell
		V_{RECH} = 100mV/cell	90	120	155	mV/cell
Battery over-voltage protection (OVP) threshold	V_{BATT_OVP}	Comparing with V_{BATT_REG}, rising		180		mV/cell
Battery OVP threshold hysteresis		Comparing with V_{BATT_OVP}, falling		150		mV/cell
BATT leakage current in shutdown mode	I_{BATT_SHDN}	V_{BATT} = 28V, V_{IN} = PGND			10	µA
Charge current	I_{CC}	R_{ISET} = 96kΩ	0.9	1	1.1	A
		R_{ISET} = 48kΩ	1.8	2	2.2	
Pre-charge current	I_{PRE}	V_{IN} = 24V, CELL = 4, V_{BATT} = 9V	100	200	300	mA
Input current regulation during battery short circuit	I_{SHORT}	V_{IN} = 24V, V_{BATT} < 1.5V/cell, current in Q1		60		mA
Input Voltage and Input Current Regulation						
Input current limit	I_{IN_LIM}	R_{ILIM} = 96kΩ	0.9	1	1.1	A
		R_{ILIM} = 48kΩ	1.8	2	2.2	
Input minimum voltage regulation reference	$V_{IN\_MIN\_REF}$		1.18	1.2	1.22	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, 4-Cell, V_{BATT} = 4.2V/Cell, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal Regulation and Protection						
Thermal shutdown rising threshold (7)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (7)				20		°C
Battery Temperature Monitoring and Protection						
NTC cold temperature threshold	V_{TH_COLD}	V_{NTC} rising as percentage of V_{VCC}	70.3	71	71.8	%
NTC cold temperature threshold hysteresis		V_{NTC} falling as percentage of V_{VCC}		1.4		%
NTC hot temperature threshold	V_{TH_HOT}	V_{NTC} falling as percentage of V_{VCC}	47.5	48.2	49	%
NTC hot temperature threshold hysteresis		V_{NTC} rising as percentage of V_{VCC}		1.4		%
NTC float threshold	V_{TH_FLOAT}	V_{NTC} rising as percentage of V_{VCC}	90.2	91.1	92	%
Logic I/O Pin Characteristic						
STAT pin output voltage		I_{SINK} = 5mA			0.4	V
ACOK pin output voltage		I_{SINK} = 1mA			0.4	V
Timing Characteristic						
Charge safety timer	t_{TMR}	t_{TMR} = 20hrs		20		hours
LED blinking frequency (7)		V_{NTC} = AGND		2		Hz

Notes:

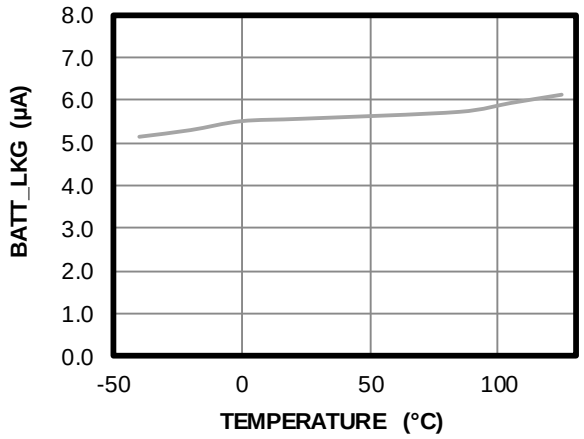
7) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

L = 10µH/35mΩ, C_{BATT} = 10µF, T_A = 25°C, unless otherwise noted.

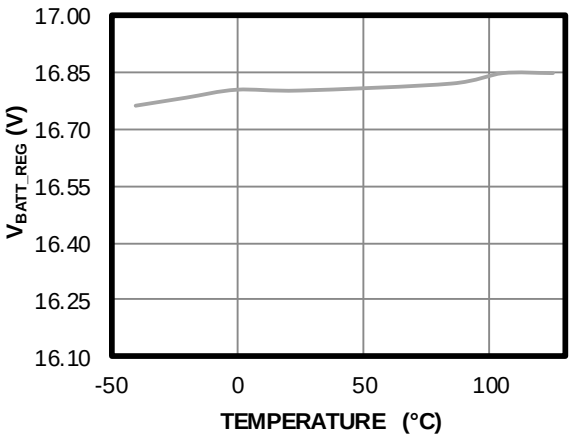
BATT_LKG vs. Temperature

BATT = 28V



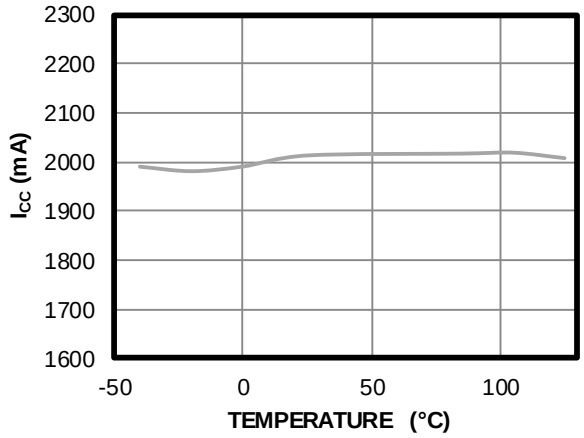
Battery Charge Voltage Regulation vs. Temperature

BATT_REG = 16.8V

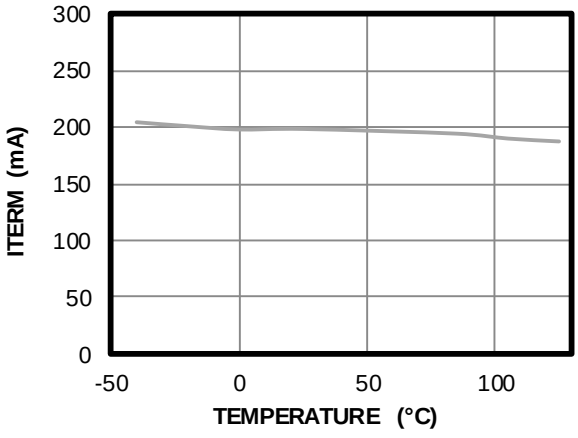


Current Charge vs. Temperature

I_{CC} = 2A

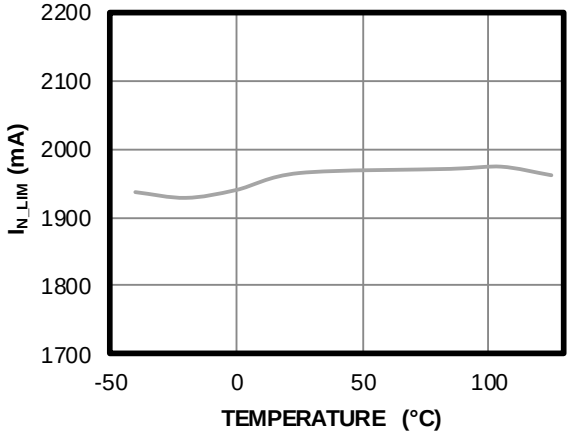


Termination Current vs. Temperature

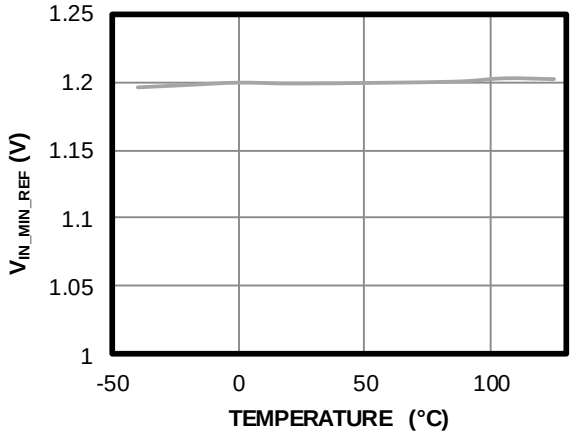


Input Current Limit vs. Temperature

I_{IN_LIMIT} = 2A



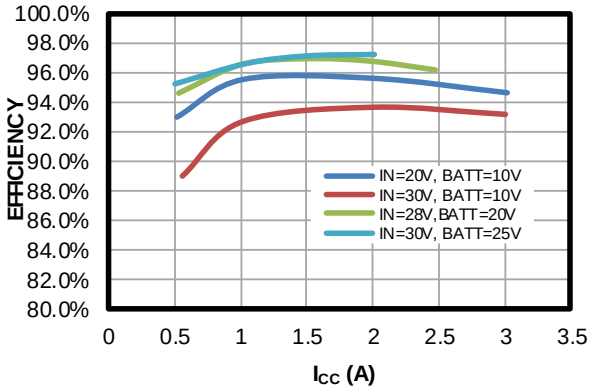
VIN_MIN Voltage Reference vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

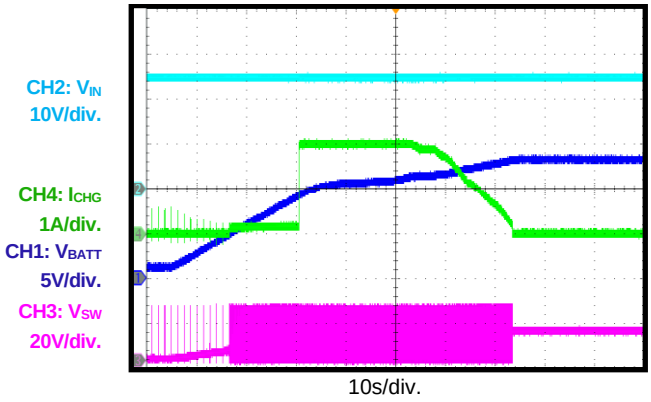
L = 10µH/35mΩ, C_{BATT} = 10uF, T_A = 25°C, unless otherwise noted.

Efficiency vs. Charge Current



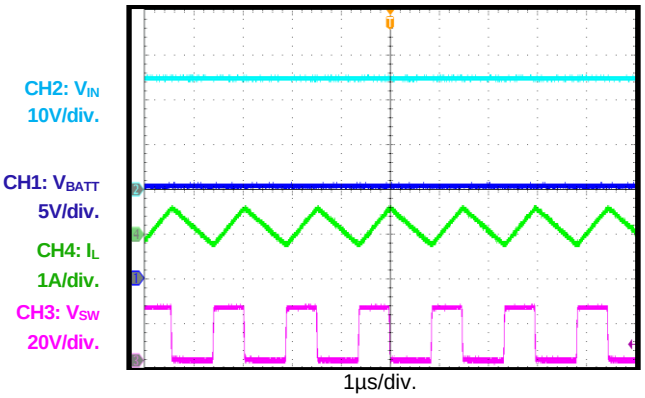
Battery Charge Curve

V_{IN} = 24V, 3-cell, $V_{BATTREG}$ = 4.2V, I_{CC} = 2A, I_{IN_LIM} = 2A



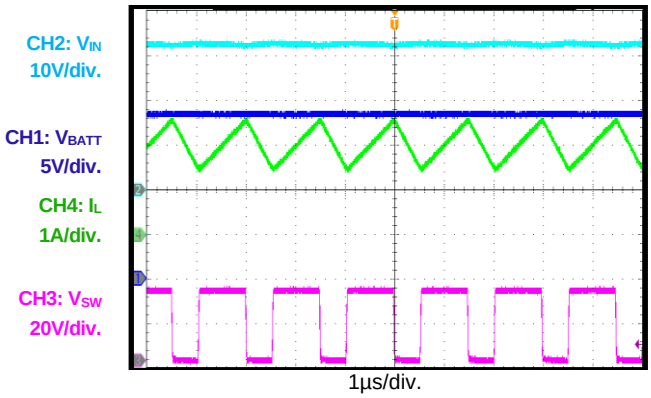
PRE Charge Steady State

V_{IN} = 24V, 4-cell, V_{BATT} = 10V



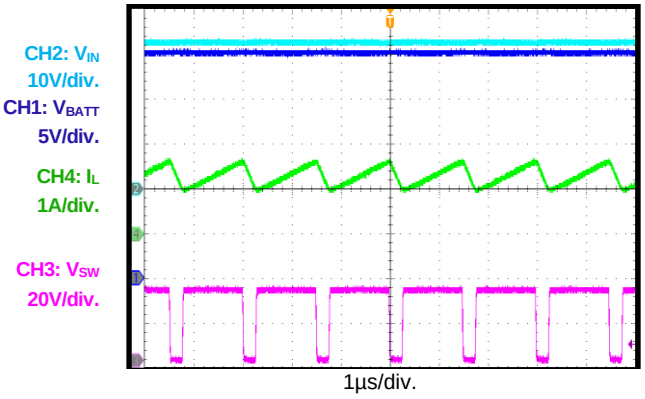
CC Charge Steady State

V_{IN} = 32V, 5-cell, V_{BATT} = 18V , I_{CC} = 2A, I_{IN_LIM} = 2A



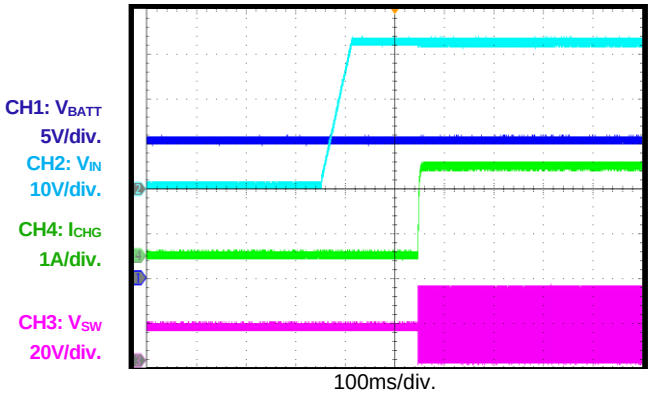
CV Charge Steady State

V_{IN} = 32V, 6-cell, V_{BATT} = 25.2V, I_{CC} = 2A, I_{IN_LIM} = 2A



Start-Up, CC Charge Mode

V_{IN} = 32V, 4-cell, V_{BATT} = 15V , I_{CC} = 2A, I_{IN_LIM} = 2A



FUNCTIONAL BLOCK DIAGRAM

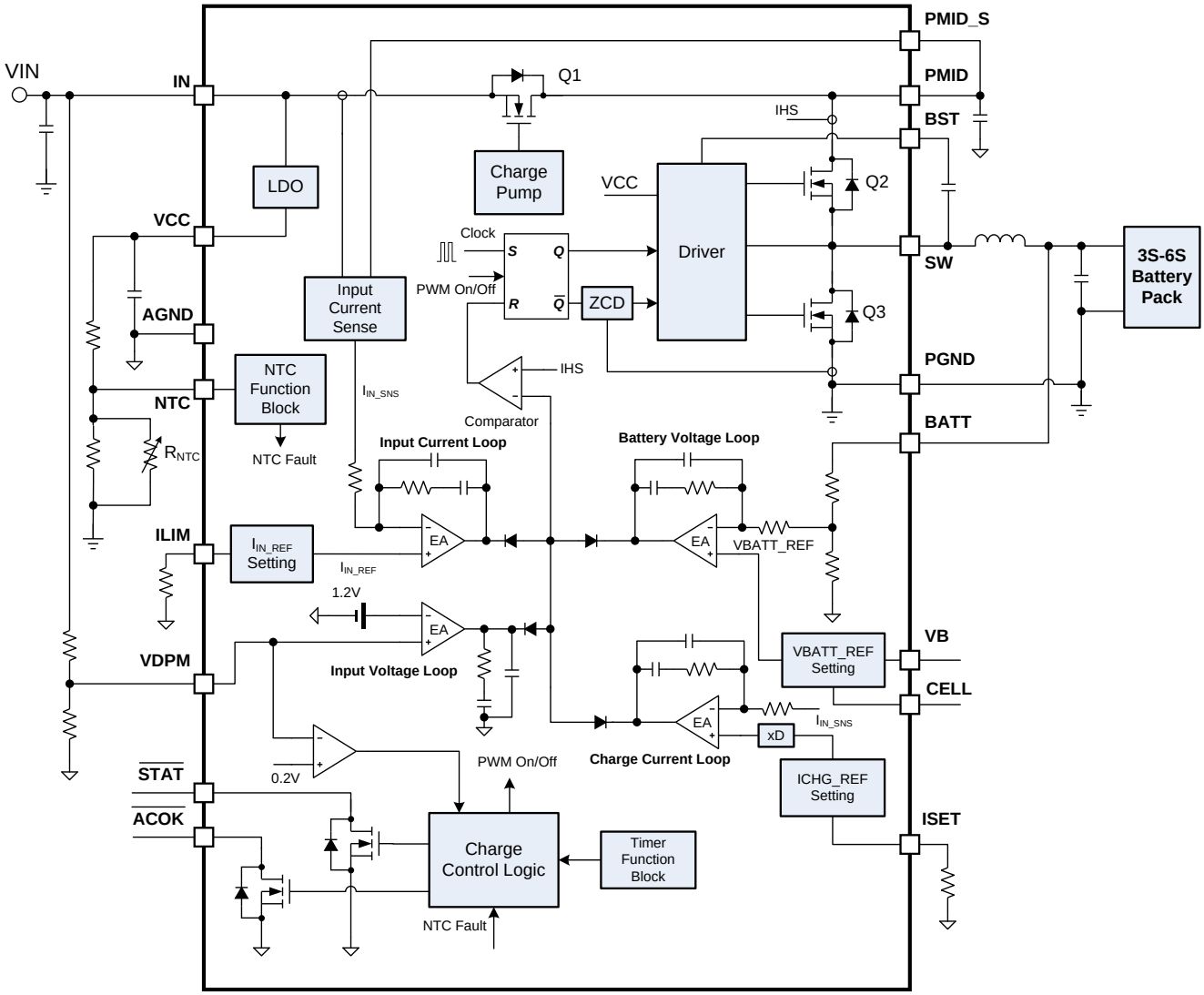


Figure 1: Functional Block Diagram

OPERATION

Introduction

The MP2659 is a highly integrated switching charger designed for portable devices with 3-cell to 6-cell series Li-ion or Li-polymer batteries. The device manages battery charging with various series cell number selections and battery regulation voltages.

Power Supply

The VCC pin is powered by the IN pin, and then generates a regulated 5V output with a minimum 50mA current limit. The VCC voltage (V_{VCC}) is utilized by the internal bias circuit and the power MOSFET driver. It can also be used for external resistive logic pull-up, or LED driver bias. When a battery is present but the input source is absent, VCC has no output.

The IC exits sleep mode and is ready to start the charging progress once V_{CC} exceeds the internal lockout threshold.

Input Valid Indication

The IC checks the voltage of the input source (V_{IN}) before start-up. The input source has to meet the following requirements:

- $V_{IN} > V_{IN\_UVLO}$
- $V_{IN} > V_{BATT} + V_{HDRM}$

The $\overline{ACOK}$ pin pulls low after V_{IN} meets the conditions above, which indicates that the input power source is ready. After a 170ms delay, the DC/DC converter is enabled.

Charge Cycle

The MP2659 has a battery short-circuit protection mechanism to limit the input current when the battery voltage is below 1.5V/cell. This activates the dead battery pack and resets the protection MOSFET in the battery pack. In this mode, the input current is regulated at I_{SHORT} (60mA) for 20ms, and is suspended for 1.4s.

During normal charging, the IC has three charging phases in the charging cycle: pre-charge, constant current charge, and constant voltage charge.

Pre-charge (phase 1): When the battery voltage exceeds 1.5V/cell but is below 3V/cell (2.5V/cell if the battery regulation is set to 3.6V), the IC charges the battery with a constant 200mA charge current.

Constant current charge (phase 2): When the battery voltage exceeds 3V/cell (2.5V/cell if the battery regulation is set to 3.6V), the IC enters constant current charge phase. The charge current can be set by the ISET pin resistor.

Constant voltage charge (phase 3): When the battery voltage reaches the charge regulation voltage (V_{BATT_REG}), the charge current begins to decrease. When the charge current drops to the battery termination threshold (I_{TERM}), the charge cycle is considered complete after a deglitch time (t_{TERM_DGL}). If the charge current does not reach I_{TERM} before the charging safety timer expires, the charge cycle ends, and the corresponding timeout fault signal is asserted.

Figure 2 shows a typical charge cycle.

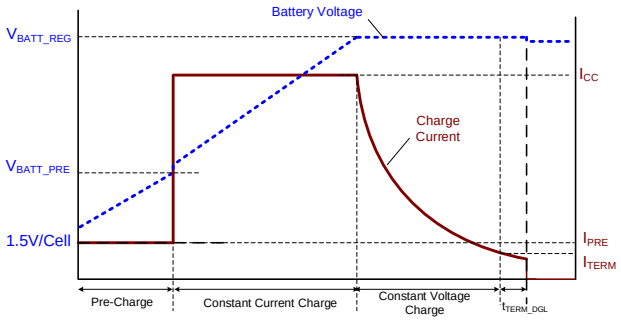


Figure 2: Battery Charging Cycle

Auto-Recharge

Once the battery charge cycle completes, the charger remains off. During this time, the external load may consume battery power, or the battery may auto-discharge. A new charge cycle automatically begins if input power is present and the battery voltage falls below the auto-recharge threshold. The charging safety timer resets when the auto-recharge cycle begins.

Input Voltage and Input Current Limiting

The MP2659 has input current and input voltage limiting to avoid overloading the input power supply. The VDPM pin voltage is the feedback input for the input voltage regulation loop. When the VDPM voltage falls to 1.2V, the

charge current is reduced to prevent the input source from being overloaded.

The input voltage can be regulated by a resistor divider connected to the IN pin, VDPM pin, and AGND. The regulation voltage (V_{IN_MIN}) can be calculated with Equation (1):

$$V_{IN\_MIN\_REF} = V_{IN\_MIN} \times \frac{R_2}{R_1 + R_2} (V) \quad (1)$$

Where $V_{IN\_MIN\_REF}$ is the internal voltage reference (about 1.2V), and R_1 and R_2 are the resistor dividers.

When the VDPM voltage is pulled below 0.2V, the charger is disabled.

The input current limit (I_{IN_LIM}) can be set by the ILIM pin with a resistor (R_{ILIM}) to AGND. If the input current of Q1 reaches the preset limit, the charge current is reduced to regulate the input current.

I_{IN_LIM} can be calculated with Equation (2):

$$I_{IN\_LIM}(A) = \frac{96(k\Omega)}{R_{ILIM}(k\Omega)} (A) \quad (2)$$

Cell Selection

The MP2659 can be configured to charge 3- to 6-series cell battery packs. The battery configuration is determined by the connection on the CELL pin.

Table 1: CELL Pin Selection

CELL Pin Connection	Battery Cells
AGND	3-cell
Float	4-cell
Pull up to VCC	5-cell
100kΩ resistor to AGND	6-cell

With different series cell number selections, the battery short-circuit threshold (V_{BATT_SRT}), the pre-charge to fast-charge threshold (V_{BATT_PRE}), the battery charge voltage regulation (V_{BATT_REG}) and the recharge threshold (V_{RECH}) scale with the cell number to properly manage the charging phases.

Battery Regulation Voltage

The MP2659 supports several battery charge regulation voltages, which can be configured via the VB pin (see Table 2).

Table 2: Selecting Battery Regulation Voltage

VB Pin Connection	Charge Regulation Voltage
AGND	3.6V
Float	4.2V
Pull up to VCC	4.35V
100kΩ resistor to AGND	4.15V

Charge Current Setting

The MP2659 eliminates the external sense resistor and senses the charge current (I_{CC}) internally. The charge current can be set by the resistor (R_{ISET}) between the ISET and AGND pins, calculated with Equation (3):

$$I_{CC}(A) = \frac{96(k\Omega)}{R_{ISET}(k\Omega)} (A) \quad (3)$$

The maximum charge current can be set up to 3A. It is related to the PCB thermal dissipation condition and input voltage. With a lower input voltage, the IC's switching loss is smaller, and the maximum deliverable current can be higher. The charge current should be set according to the thermal performance for each application.

Negative Thermal Coefficient (NTC) Input

Connect an appropriate resistor from VCC to the NTC pin, and connect the thermistor from the NTC pin to AGND. The resistor divider determines the NTC pin voltage. If the NTC voltage falls outside of the NTC window, the MP2659 stops charging. The charger restarts if the temperature goes back into the NTC window range.

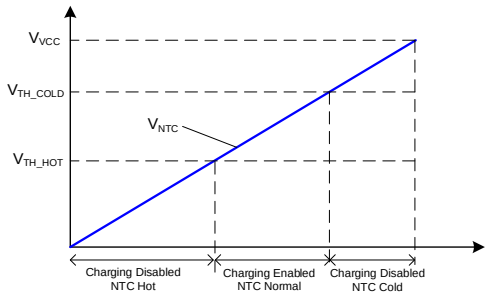


Figure 3: NTC Charging Window

Battery Over-Voltage Protection

The MP2659 has battery over-voltage protection. If the battery voltage exceeds the battery over-voltage threshold (V_{BATT_OVP}), charging is disabled, the switcher stops, and the fault status is reported on the $\overline{STAT}$ pin.

Charging Safety Timer

The IC provides a safety timer to prevent extended charging cycles due to abnormal battery conditions. If the charging timer finishes before charging completes, charging is terminated.

The safety timer resets at the beginning of a new charge cycle. The following actions restart the safety timer:

- Input voltage removal and reinsertion
- A new charge cycle starts
- The VDPM pin is pulled below 0.2V, then released

Operation Indication

The IC has $\overline{ACOK}$ and $\overline{STAT}$ pins to indicate the power source and operation status. The status of the $\overline{ACOK}$ and $\overline{STAT}$ pins changes based on different input power sources and operating conditions (see Table 3).

Table 3: Operation Indicators

IN	Charging State	$\overline{ACOK}$	$\overline{STAT}$
Absent	N/A	Hi-Z	Hi-Z
Present	Charging	Low	Low
Present	Charging complete, charge disable	Low	Hi-Z
Present	NTC fault, safety timer expiration, battery OVP	Low	Blinking at 2Hz
Present	Regulation mode	Low	Blinking at 1Hz

Regulation Mode

If OTP bit NTCDET is set to 1 and the NTC pin is pulled up to VCC, the MP2659 operates in regulation mode. In this mode, battery charge termination is blocked, and the device generates an output voltage that is equal to V_{BATT_REG}.

One-Time Programming (OTP)

The MP2659 has one-time programming (OTP) to configure the default value of several parameters. The OTP Map section on page 15 shows the configurable parameters.

OTP MAP

Bit #	Symbol	Default	Description
5	V_{RECH}	0	Recharge threshold. This value is below the battery regulation voltage. 0: 250mV/cell 1: 100mV/cell
4	I_{TERM}	0	Termination current selector. 0: 200mA 1: 100mA
3	NTCDET	0	When this bit is enabled and NTC is pulled up to VCC, the MP2659 is operates in regulation mode, battery charge termination is blocked. 0: Disable 1: Enable
2	f_{SW}	0	Switching frequency selector. 0: 680kHz 1: 350kHz
1	t_{TMR}	0	Charging safety timer selector. 0: 20Hrs 1: 10Hrs
0	TMR_DIS	0	This bit enables the safety timer. 0: Enable 1: Disable

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

Choose an inductor that does not saturate under the worst-case load condition. Estimate the required inductance with Equation (4):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L\_MAX}} \times \frac{V_{BATT}}{V_{IN} \times f_{SW}} \quad (4)$$

Where V_{IN} is the input voltage, V_{BATT} is the battery voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is usually designed at 30% to 40% of the CC charge current.

It is recommended to use a 10µH inductor with a 5A saturation current for most applications.

Selecting the PMID Capacitor (C_{PMID})

The PMID pin capacitor (C_{PMID}) serves as the buck regulator's decoupling capacitor. A ceramic 2.2µF/50V capacitor with X5R or X7R dielectrics and 1206 size is recommended.

Do not put additional capacitance on the PMID pin. Connect a 2A/40V Schottky diode in an SMA package from IN to PMID.

Selecting the IN Capacitor

For applications where the input is ≤20V, it is recommended to make the input capacitor (C_{IN}) a 1µF/50V ceramic capacitor in a 0805 or 1206 package.

For applications where the input is >20V, (especially for those with input hot insertion conditions), add a ≥47µF electrolytic capacitor on the IN pin.

If a high-voltage adapter is plugged in during input hot insertion, the cable's parasitic inductance (together with the IN/PMID node capacitance) can generate an inrush current and voltage spike. An electrolytic capacitor and a TVS diode can help dampen or clamp the voltage spike.

The ESR of the electrolytic capacitor can effectively damp the inrush oscillation magnitude. A 47µF/50V electrolytic capacitor is recommended (see Table 3).

The hot insertion must be tested and verified for real applications. In case of a higher input voltage application (e.g. 28V), it is recommended to place a TVS diode across the IN and GND pins. It is recommended to use one of the following diodes:

- 1SMA33A from Sunmate in an SMA package
- SMAJ33AQ from Diode in an SMA package

Selecting the BATT Capacitor

The MP2659 requires ≥10µF capacitance to stabilize the loop on the BATT node. However, the battery capacitor (C_{BATT}) is generally effective only during hot plug insertion or short-circuit conditions.

When the battery is plugged in, there might be an overshoot on the BATT pin due to the oscillation caused by C_{BATT} and battery cable parasitic inductance. For 5-cell or 6-cell applications, this overshoot may harm the BATT pin. A 47µF/50V electrolytic capacitor can damp the overshoot with its ESR. Otherwise, use a TVS diode to clamp the BATT node spike. The recommended TVS diodes are listed above.

If the BATT node can be shorted to ground, C_{BATT} and the cable inductance can induce a negative voltage spike on the BATT pin, and may harm the IC. An electrolytic capacitor can help dampen the spike, or a unidirectional TVS diode can clamp the spike (see Table 3).

Protecting the PMID Pin

When a high-voltage battery is plugged in, there is a current path that flows from the main inductor, high-side MOSFET body diode, then charges up the PMID pin capacitor. An LC resonant circuit may induce a voltage spike on the PMID pin. With a high voltage battery, the PMID voltage can rise to a dangerous level, so the PMID pin must be protected.

For 5-cell or 6-cell applications, the PMID pin overshoot of battery insertion should be tested and verified in real application. A TVS diode can be added on PMID node to clamp the overshoot. The recommended TVS diodes are listed above. If the PMID pin has a TVS diode, the IN pin does not require a TVS diode (see Table 3).

Table 3: Components Selection Guide

Pin	Condition	Recommendations
IN	≤20V input	1µF/50V ceramic capacitor for adapter applications. Add a ≥47µF capacitance for solar applications.
	>20V input	Add a 47µF/50V electrolytic capacitor. A TVS diode is required if the IN voltage exceeds the pin's maximum voltage rating during a VIN hot insertion test.
BATT	3-cell or 4-cell	10µF/50V ceramic capacitor.
	5-cell or 6-cell	Add a TVS diode or ≥47µF electrolytic capacitor.
PMID	-	2.2µF/50V ceramic capacitor (1206 size preferred). Connect a 2A/40V Schottky diode from IN to PMID. A TVS diode is required if the PMID voltage exceeds the pin's maximum voltage rating during a VBATT hot insertion test.

Setting the VDPM Pin

Multiple functions can be designed with the VDPM pin:

Minimum Input Voltage Limiting

A resistive voltage divider from the IN pin to the VDPM pin sets the minimum input voltage limit (V_{IN_MIN}).

The maximum V_{IN_MIN} regulation voltage should be set below the minimum DC output voltage of the power supply, including the IR voltage drop from the DC input current and series resistance on the PCB, connector, and cable.

The minimum V_{IN_MIN} regulation voltage should be set above V_{BATT_REG} + V_{HDRM}.

Enable (EN) Control

Pull down the VDPM pin below 0.2V disables the charger and reset the safety timer. Figure 4 shows a recommended application circuit for this function.

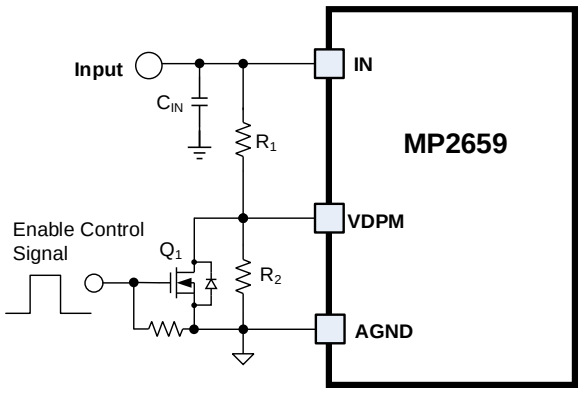


Figure 4: Enable Control

Where R2 is recommended to be 10kΩ.

Disable Input Voltage Limiting

If the input voltage limit function is not required, the VDPM pin can be tied to the VCC pin.

Direct Enable (EN) Control

If input voltage limiting is not used, the VDPM pin can be directly driven by the host to enable/disable the charging. It is recommended to use a 100kΩ resistor to pull up the VDPM pin to VCC. The logic high level should exceed 1.3V, and the logic low level should be below 0.2V.

Resistor Selection for the NTC Sensor

The battery temperature-sensing NTC thermistor can be connected in series or parallel. Figure 5 shows an NTC connected in parallel.

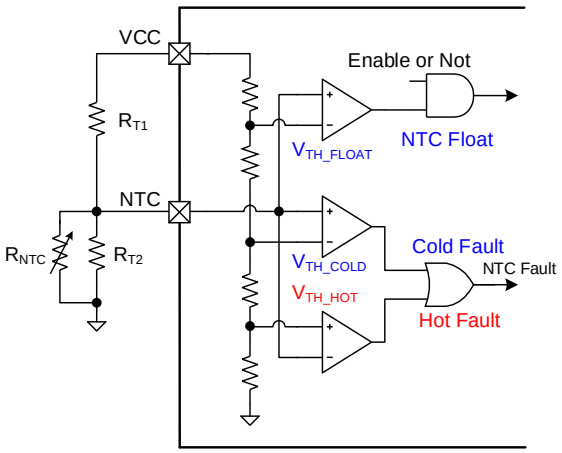


Figure 5: NTC Parallel Connection

Calculate the appropriate R_{T1} and R_{T2} values to set the NTC window with Equation (5) and Equation (6), respectively:

$$R_{T1} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{COLD} \times V_{HOT} \times (R_{NTC\_COLD} - R_{NTC\_HOT})} \quad (5)$$

$$R_{T2} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{HOT} \times (1 - V_{COLD}) \times R_{NTC\_COLD} - V_{COLD} \times (1 - V_{HOT}) \times R_{NTC\_HOT}} \quad (6)$$

Where R_{NTC_HOT} is the value of the NTC resistor at the upper bound of its operating temperature range, R_{NTC_COLD} is its lower bound, V_{HOT} is the hot temperature threshold percentage, and V_{COLD} is the cold temperature threshold percentage.

For example, for a 103AT-2 thermistor, the thermistor has the following electrical characteristics:

- At 0°C, $R_{NTC\_COLD} = R_{0°C} = 27.28k\Omega$
- At 60°C, $R_{NTC\_HOT} = R_{60°C} = 3.02k\Omega$

Put the above resistor values into Equation (5) and Equation (6) to determine $R_{T1} = 2.26k\Omega$, and $R_{T2} = 6.95k\Omega$.

Figure 6 shows an NTC connected in series.

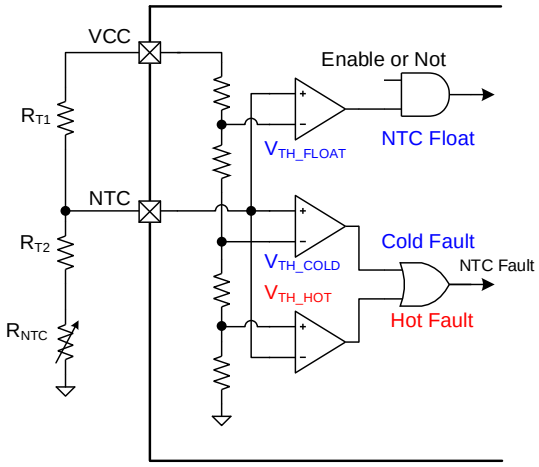


Figure 6: NTC Series Connection

R_{T1} and R_{T2} are then calculated using Equation (7) and Equation (8), respectively:

$$R_{T1} = \frac{(R_{NTC\_COLD} - R_{NTC\_HOT}) \times (1 - V_{COLD}) \times (1 - V_{HOT})}{(1 - V_{HOT}) \times V_{COLD} - (1 - V_{COLD}) \times V_{HOT}} \quad (7)$$

$$R_{T2} = \frac{V_{COLD} \times R_{T1}}{1 - V_{COLD}} - R_{NTC\_COLD} \quad (8)$$

Put the R_{NTC_COLD} and R_{NTC_HOT} resistor values into the equations above to determine R_{T1} = 15.98kΩ, and R_{T2} = 11.85kΩ.

PCB Layout Guidelines

PCB layout is critical to meet specified noise, efficiency, and stability requirements. For the best results, follow the guidelines below:

1. Place the PMID capacitor as close as possible to the PMID and PGND pins using a short copper plane connection.
2. Place the PMID capacitor on the same layer as the IC.
3. Minimize the high-frequency current path loop between the PMID capacitor and the buck converter's power MOSFETs (PMID pin to capacitor, PGND to capacitor).
4. Place the inductor input terminal as close as possible to the SW pin.
5. Minimize the copper area of the inductor input terminal trace to reduce electrical and magnetic field radiation, but ensure the trace is wide enough to carry the charging current.
6. Minimize parasitic capacitance from the inductor input terminal to any other trace or plane.
7. If possible, choose a PMID capacitor with 1206 dimensions, and route SW traces beneath the PMID capacitor.
8. Connect the AGND pin to the ground of the battery capacitor, such as C_{BATT} or PCB ground.
9. Place decoupling capacitors (e.g. the VCC pin capacitor) as close as possible to the IC pins, and make the connection as short as possible.
10. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
11. Ensure that the number and physical size of the vias is sufficient for a current path.

TYPICAL APPLICATION CIRCUIT

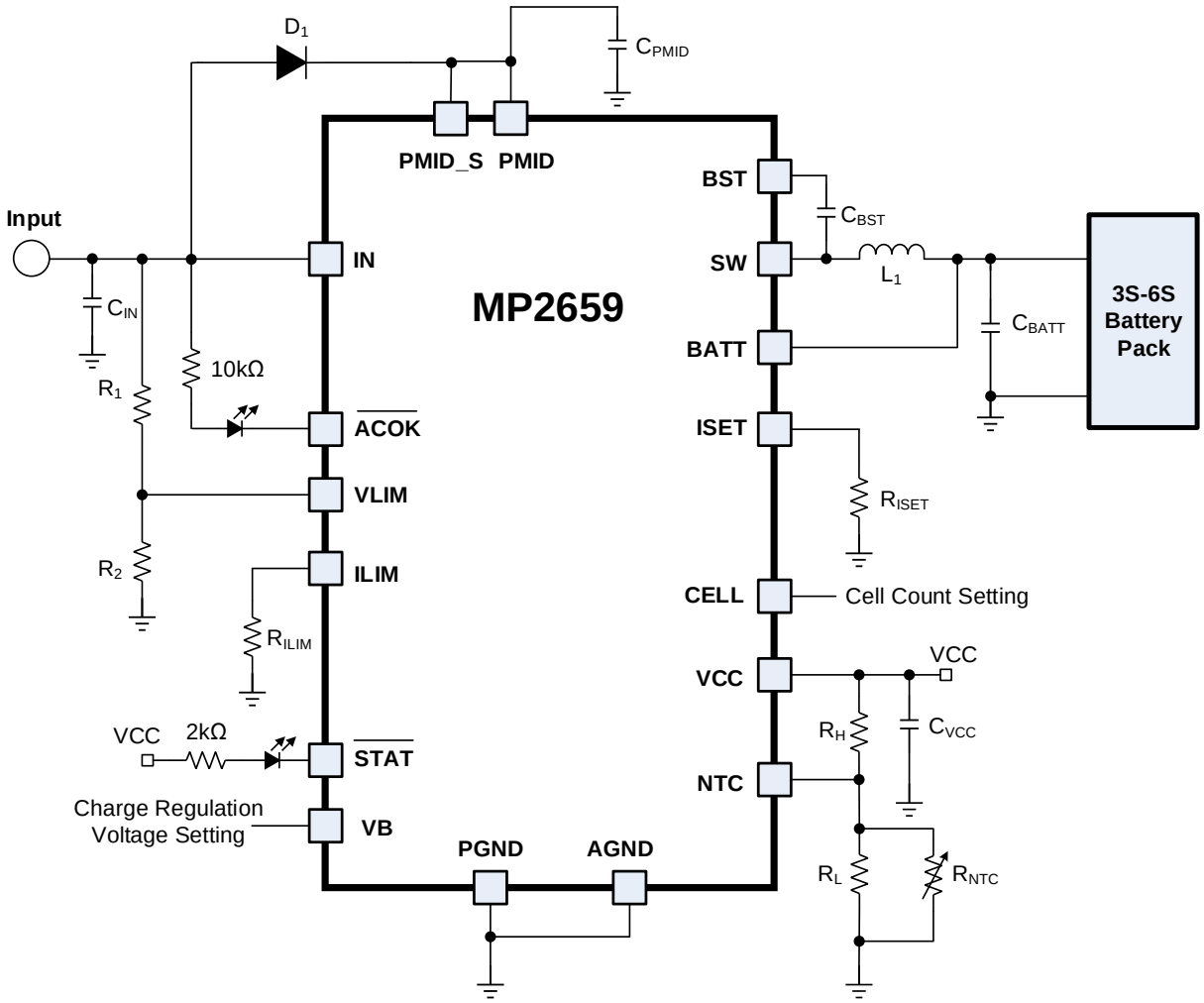


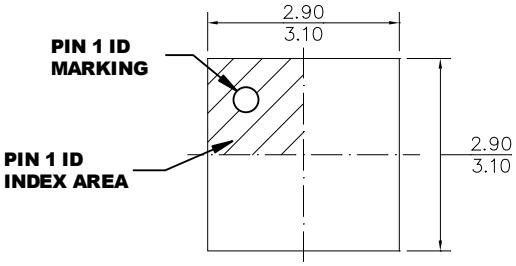
Figure 7: Typical Application Circuit for 16V Input, 3-cell

Table 4: Key BOM

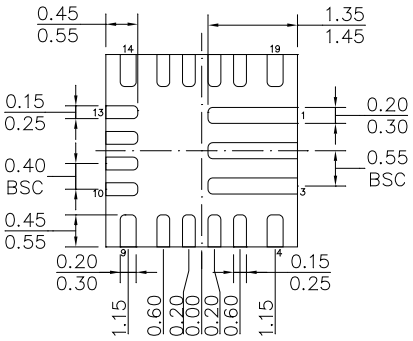
Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	1µF	Ceramic capacitor, 50V, X5R or X7R	0805	Any
1	C_{BATT}	10µF	Ceramic capacitor, 50V, X5R or X7R	1206	Any
1	C_{PMID}	2.2µF	Ceramic capacitor, 50V, X5R or X7R	1206	Any
1	C_{VCC}	1µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	10µH	Inductor, I_{SAT} > 4A	SMD	Any
1	D1	B240A	Schottky diode 2A/40V	SMA	Any

PACKAGE INFORMATION

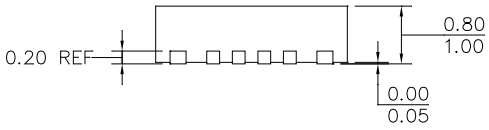
QFN-19 (3mmx3mm)



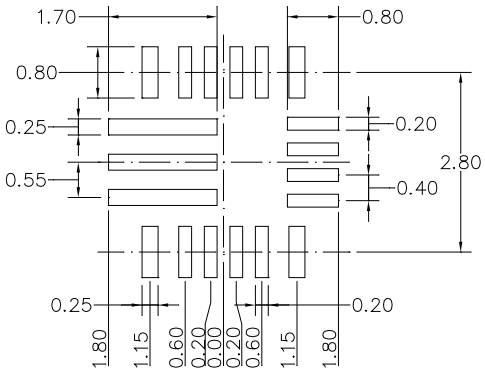
TOP VIEW



BOTTOM VIEW



SIDE VIEW

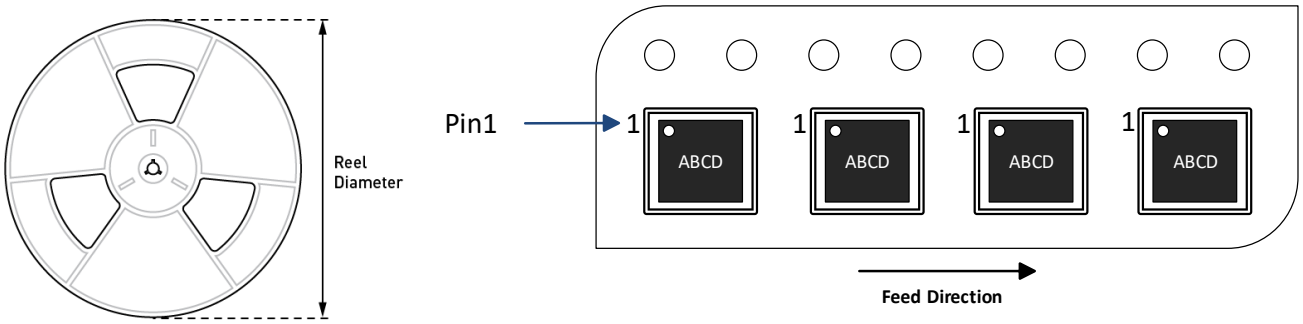


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2659GQ-xxxx–Z	QFN (3mmx3mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/29/2020	Initial Release	-
1.1	10/29/2020	Changed the maximum voltage rating from 40V to 45V	1, 5
		Modified the application section components selection guide	4, 16–17
1.2	2/22/2024	Modified a package dimension from 0.35 to 1.35 in the Bottom View section	20
		Updated the formatting of the Revision History table	22