MP2642

Integrated, 1A, Bidirectional Active Balancer

DESCRIPTION

The MP2642 is a highly integrated, bidirectional active balancer that provides up to 1A of charge redistribution among Li-ion, Li-polymer, or lithium iron phosphate batteries in a two-series battery pack. As an alternative to dissipating energy with passive balancing, the MP2642 efficiently moves charge between cells to minimize balancing time and heat generation. The device can also compensate for cell capacity mismatch to extend battery runtime.

By combining multiple MP2642 devices, active balancing can be scaled to any number of series cells, and charge can be redistributed to and from any cells within the pack.

The MP2642 can balance adjacent cells using two modes: buck-balance mode and boost-balance mode. In buck-balance mode, the MP2642 transfers energy from the upper cell (CU) to the lower cell (CL). In boost-balance mode, the MP2642 transfers energy from CL to CU.

To guarantee safe operation, the MP2642 provides CL and CU over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MP2642 is available in a QFN-26 (4mmx4mm) package.

FEATURES

- Wide Operating Voltage Range Compatible with LiFePO4 Batteries:
  - 2.4V Minimum Cell Voltage
  - 4.35V Maximum Cell Voltage
- Low Quiescent Current (I_Q):
  - CU Pin I_Q: Below 15μA
  - CL Pin I_Q: Below 0.1μA
- Buck-Balance Mode:
  - Net Transfer Current to Lower Cell (CL)
  - Configurable between 0.5A and 1A
- Boost-Balance Mode:
  - Net Transfer Current to Upper Cell (CU)
  - Configurable between 0.5A and 1A
- Protections:
  - Thermal Shutdown
  - Internal CL Port Battery Reverse Leakage Blocking
  - Integrated CU Low Voltage Protection in Boost-Balance Mode
- Directly Powered from the Battery Cells
- Interleavable for Transfer across Many Cells
- Available in a QFN-26 (4mmx4mm) Package

APPLICATIONS

- Grid-Level Energy Storage Systems (ESS)
- Residential ESS
- Battery Backup Systems
- Material Handling Equipment

TYPICAL APPLICATION

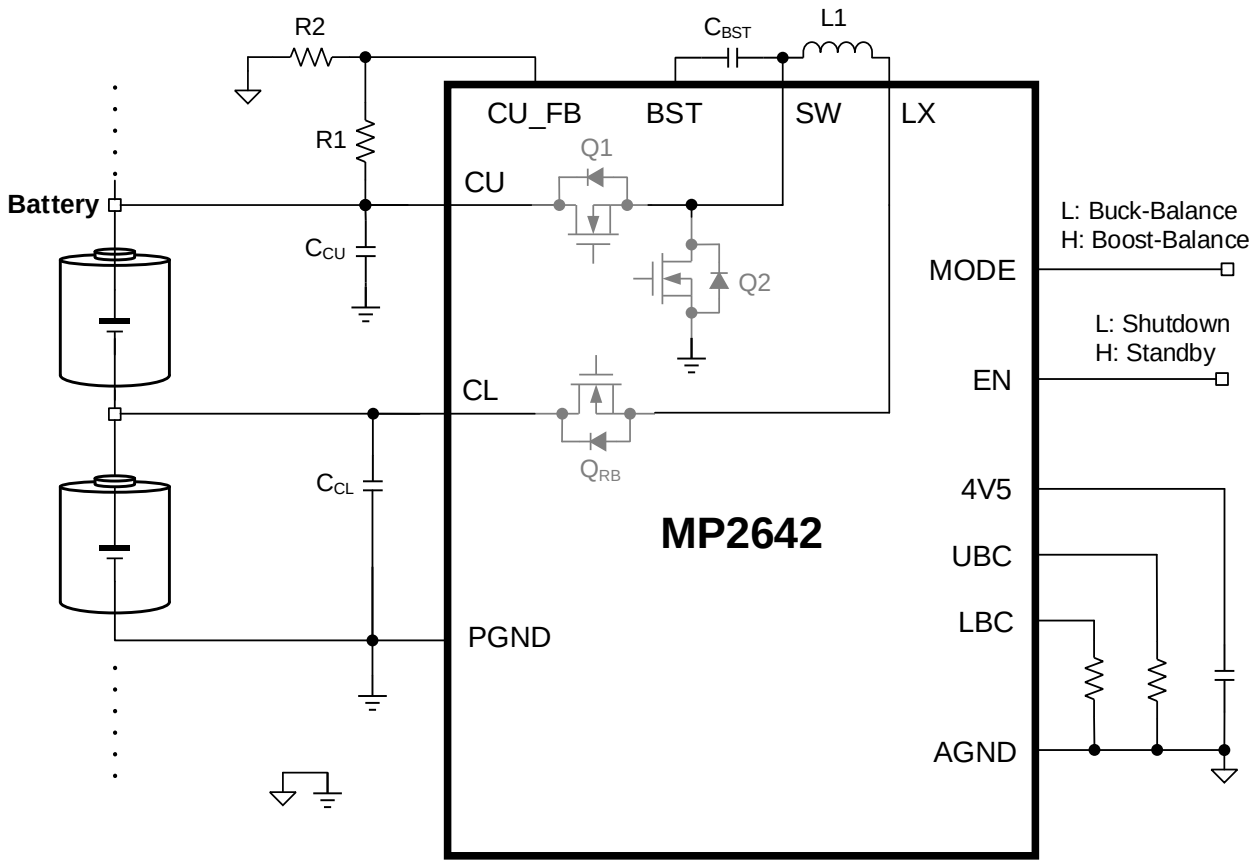


Table 1: Mode Selection for Cell Balancing

MODE Pin	Mode	Active SW	Topology
High	Boost-balance mode	Q2	Step-up
Low	Buck-balance mode	Q1	Step-down

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2642GR	QFN-26 (4mmx4mm)	*See Below*	1

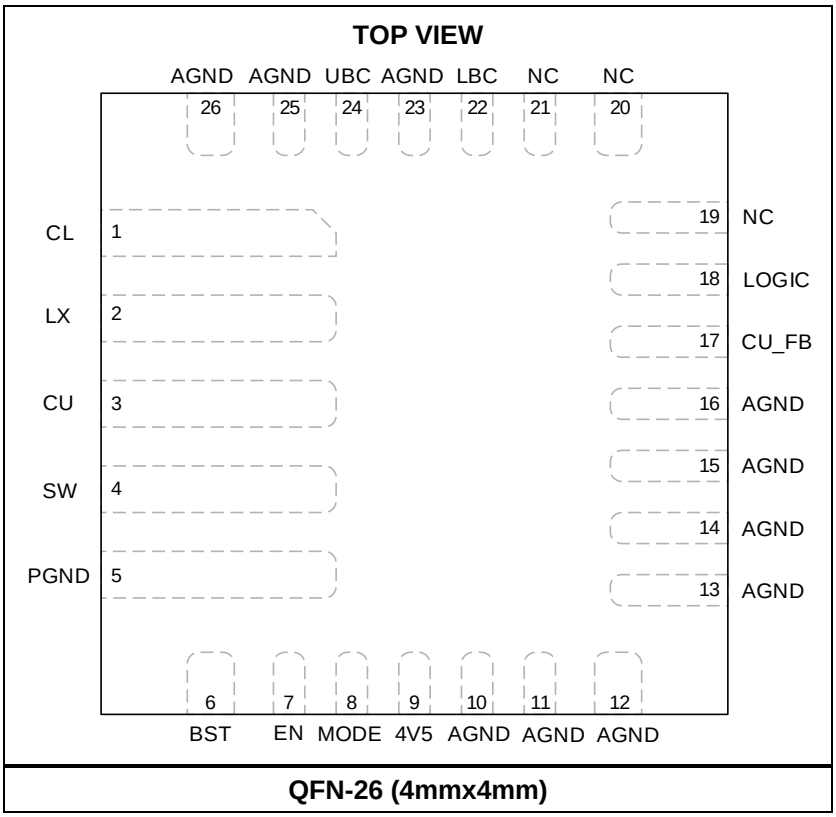
* For Tape & Reel, add suffix -Z (e.g. MP2642GR-Z).

TOP MARKING

MPSYWW
MP2642
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2642: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-26 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	CL	**Positive terminal of the lower battery cell.** Connect the CL pin to the positive terminal of the lower battery cell in the two-series battery pack.
2	LX	**Connection node between the inductor and the internal block switch.**
3	CU	**Positive terminal of the upper battery cell.** Connect the CU pin to the positive terminal of the upper battery cell in the two-series battery pack.
4	SW	**Switching node.**
5	PGND	**Power ground.** Connect the PGND pin to the negative terminal of the lower cell battery.
6	BST	**Bootstrap.** Connect a BST capacitor (C_{BST}) between the BST pin and SW node.
7	EN	**IC enable.** The EN pin is low by default. If EN is pulled low, the IC is in sleep mode, where the quiescent currents at the CU and CL terminals are very small. The MODE state does not change the IC's sleep mode. If EN is pulled high, the IC is in standby mode, where the chip enters different modes depending on the MODE pin's state.
8	MODE	**Balance mode selection.** Pull the MODE pin logic low to make the MP2642 enter buck-balance mode; pull MODE logic high to make the MP2642 enter boost-balance mode.
9	4V5	**Internal circuit power supply.** Bypass the 4V5 pin to AGND (pin 10) via a 1μF ceramic capacitor. 4V5 can be used for pull-up logic on the MP2642. This pin is not intended to carry other external loads. 4V5 only has an output when EN is pulled high.
10, 11, 12, 13, 14, 15, 16, 23, 25, 26	AGND	**Analog ground.**
17	CU_FB	**CU voltage feedback in boost-balance mode.** Set the maximum CU pin voltage via the resistor divider connected between the CU, CU_FB, and AGND pins.
18	LOGIC	**Internal circuit power logic.** The LOGIC pin must be shorted to 4V5 directly.
19, 20, 21	NC	**Not connected.** Float the NC pins.
22	LBC	**Boost-balance current setting.** Connect an external resistor between the LBC and AGND pins to configure the lower battery cell's balance current.
24	UBC	**Buck-balance current setting.** Connect an external resistor between the UBC and AGND pins to configure the upper battery cell's balance current.

ABSOLUTE MAXIMUM RATINGS (1)

CU.....-0.3V to +20V
SW.....-0.3V (-2V for 50ns) to +20V
CL.....-0.3V to +5.5V
BST to SW.....-0.3V to +5.5V
All other pins to AGND.....-0.3V to +5.5V
Continuous power dissipation.....(T_A = 25°C) (2)
..... 2.97W
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 2kV

Recommended Operating Conditions (3)

CU to PGND..... 3.9V to 16V
CL to PGND.....2.4V to 4.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-26 (4mmx4mm).....	42	9.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal Characteristics						
4V5 voltage	V_{4V5}	V_{CU} = 5V, V_{CL} = 2.1V	4.4	4.5	4.6	V
High-side (HS) N-channel MOSFET on resistance	$R_{DS(ON)\_Q1}$	T_A = 25° C		17	35	mΩ
Low-side (LS) N-channel MOSFET on resistance	$R_{DS(ON)\_Q2}$	T_A = 25°C		25	35	mΩ
Reverse blocking N-channel MOSFET on resistance	$R_{DS(ON)\_RB}$	T_A = 25°C		12	15	mΩ
Peak current limit for HS N-channel MOSFET	I_{HS_PK}	Buck-balance mode, V_{CL} = 3V	6.7	8		A
Peak current limit for LS N-channel MOSFET	I_{LS_PK}	Boost-balance mode	7.6	9.2		A
Operating frequency	f_{SW}		900	1080	1200	kHz
Thermal shutdown threshold (5)	T_{J_SHDN}			155		°C
Thermal shutdown hysteresis (5)				18		°C
CU quiescent current		V_{CL} = 3.6V, V_{CU} = 7.2V, EN = low		12	15	μA
CL quiescent current		V_{CL} = 3.6V, V_{CU} = 7.2V, EN = low			0.4	μA
CU under-voltage (UV) threshold	V_{CU_UVLO}	V_{CU} falling	3.5	3.8	4.1	V
CU under-voltage lockout (UVLO) threshold hysteresis		V_{CU} rising		300		mV
Buck-Balance Mode						
Buck-balance current range (5)			0.5		1	A
Buck-balance current (6)	I_{UBC}	R_{UBC} = 430kΩ	0.45	0.5	0.55	A
		R_{UBC} = 215kΩ	0.9	1	1.1	A
CL voltage limit	V_{CL_LIM}			4.35		V
CL over-voltage (OV) threshold	V_{CL_OVP}			4.60	4.90	V
CL OV recovery hysteresis				125	155	mV
Boost-Balance Mode						
CU voltage limit reference	$V_{CU\_LIM\_REF}$		1.18	1.2	1.22	V
CU voltage limit (5) (6)	V_{CU_LIM}	R1 = 2MΩ (1%), R2 = 402kΩ (1%)	6.93	7.17	7.41	V
CU voltage limit feedback input current	I_{FB_LKG}	Sink into the CU_FB pin			420	nA
CU over-voltage protection (OVP) threshold reference	$V_{CU\_OVP\_REFBST}$	V_{CU_LIM} < 7V		1.41		V
		V_{CU_LIM} > 7V		1.35		V
CU OVP threshold reference hysteresis				32		mV

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CU OVP threshold (5) (6)	V_{CU_OVP}	V_{CU_LIM} = 7.17V, $V_{CU\_OVP\_REFBST}$ = 1.35V, R1 = 2MΩ (1%), R2 = 402kΩ (1%)	7.8	8.07	8.33	V
		V_{CU_LIM} = 6.78V, $V_{CU\_OVP\_REFBST}$ = 1.41V, R1 = 2MΩ (1%), R2 = 430kΩ (1%)	7.7	7.97	8.23	V
CU OVP threshold hysteresis (5) (6)		V_{CU_LIM} = 7.17V, R1 = 2MΩ (1%), R2 = 402kΩ (1%)		191		mV
		V_{CU_LIM} = 6.78V, R1 = 2MΩ (1%), R2 = 430kΩ (1%)		180		mV
Boost-balance current range (5)			0.5		1	A
Boost-balance current (6)	I_{LBC}	V_{CL} = 3.6V, V_{CU} = 7.2V, R_{LBC} = 536kΩ	0.46	0.5	0.54	A
		V_{CL} = 3.6V, V_{CU} = 7.2V, R_{LBC} = 267kΩ	0.92	1	1.08	A
Lower battery cell UV threshold	V_{CL_UVLO}	V_{CL} falling in boost-balance mode		2.1		V
		V_{CL} rising in boost-balance mode		2.4		V
Logic I/O Pin Characteristics						
EN and MODE input logic low voltage					0.4	V
EN and MODE input logic high voltage			1			V

Notes:

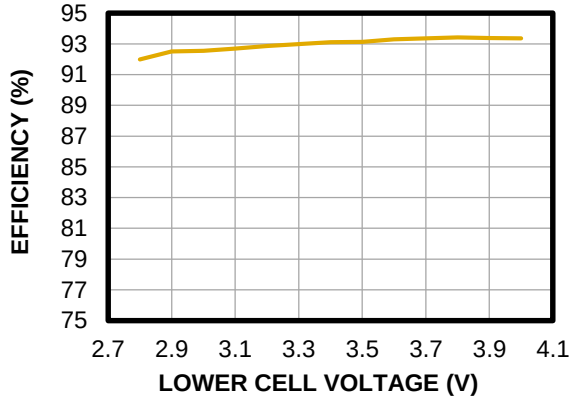
5) Guaranteed by design.
6) Calculated result.

TYPICAL CHARACTERISTICS

T_A = 25°C, C_{CL} = 10µF, C_{CU} = 10µF, L = 1.5µH (DCR = 10mΩ), R_{UBC} = 215kΩ, R_{LBC} = 267kΩ, unless otherwise noted.

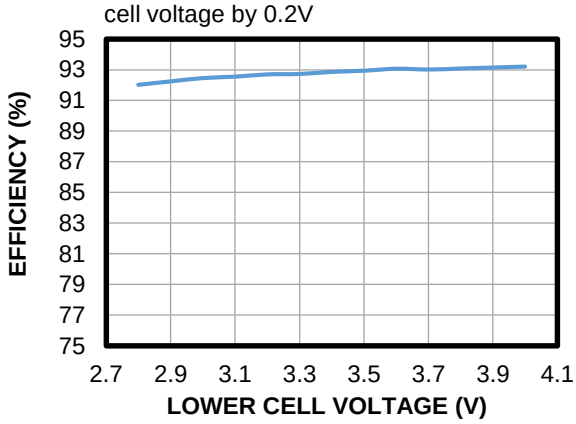
Buck-Balance Efficiency

The upper cell voltage exceeds the lower cell voltage by 0.2V



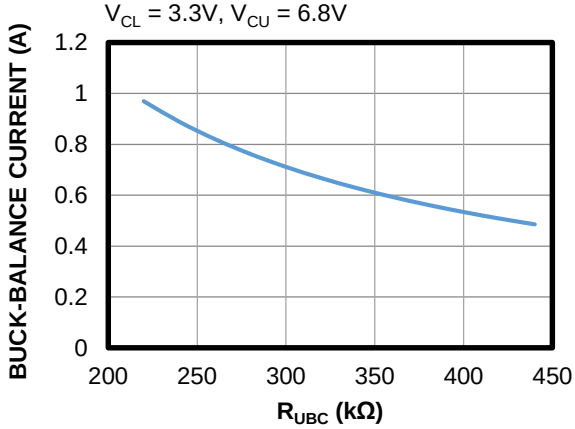
Boost-Balance Efficiency

The upper cell voltage is below the lower cell voltage by 0.2V



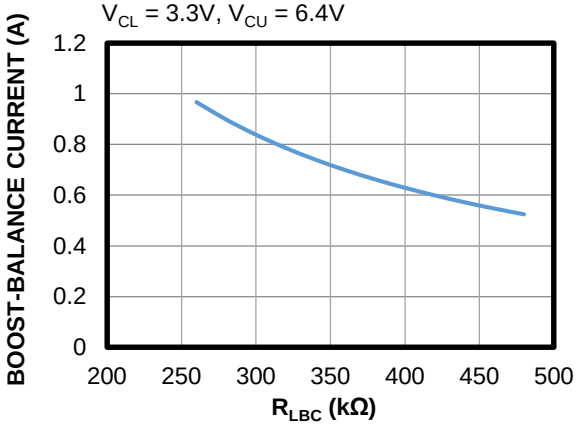
Buck-Balance Current

V_{CL} = 3.3V, V_{CU} = 6.8V



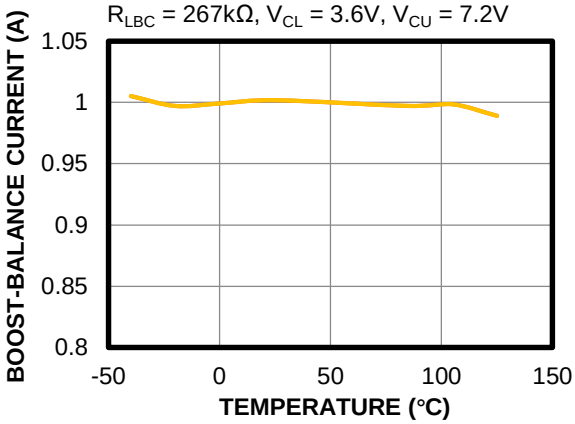
Boost-Balance Current

V_{CL} = 3.3V, V_{CU} = 6.4V



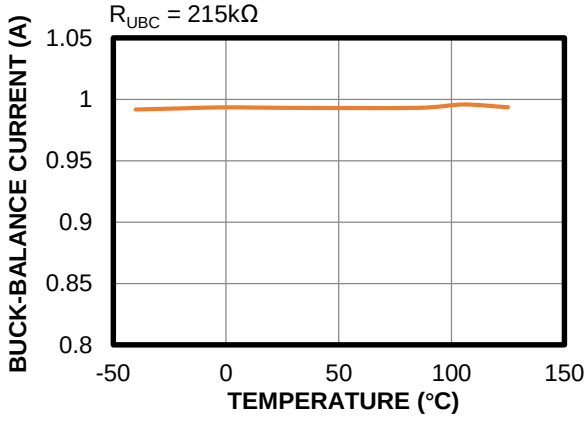
Boost-Balance Current vs. Temperature

R_{LBC} = 267kΩ, V_{CL} = 3.6V, V_{CU} = 7.2V



Buck-Balance Current vs. Temperature

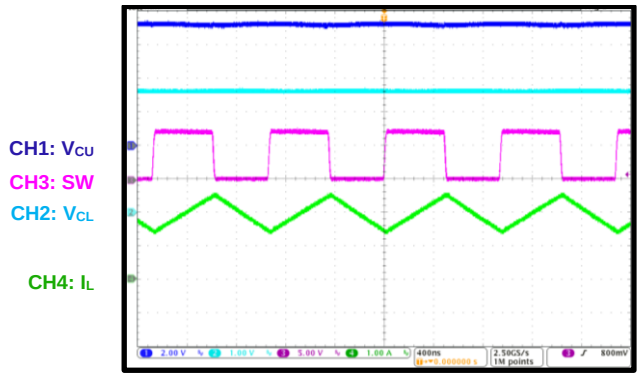
R_{UBC} = 215kΩ



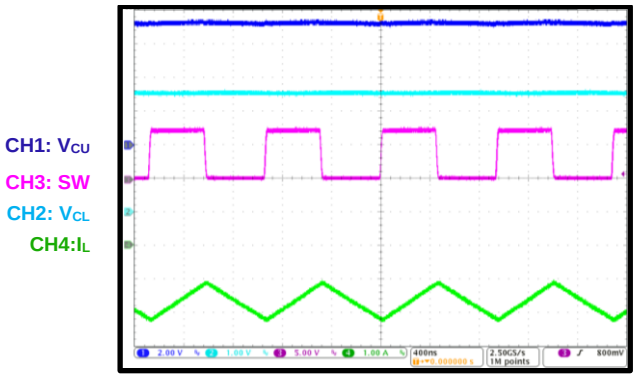
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CU} = 7.2V, V_{CL} = 3.6V, R_{UBC} = 215kΩ, R_{LBC} = 267kΩ, R1 = 2MΩ, R2 = 392kΩ, L = 1.5μH, T_A = 25°C, unless otherwise noted.

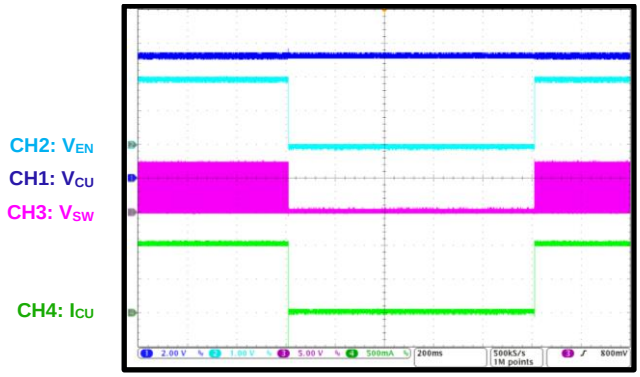
Buck-Balance Steady Operation



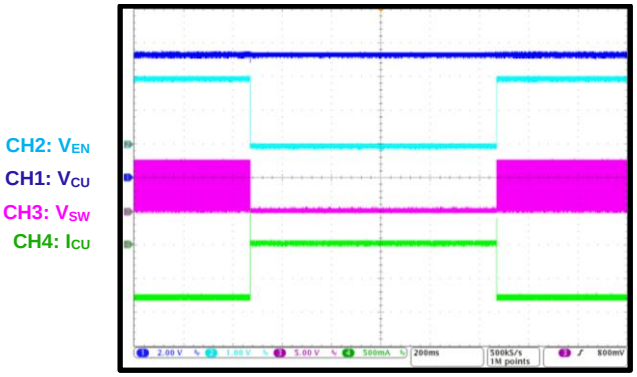
Boost-Balance Steady Operation



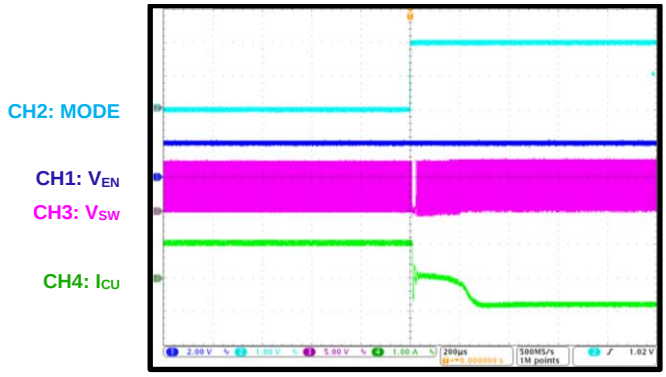
Buck-Balance Mode Enable/Disable via EN



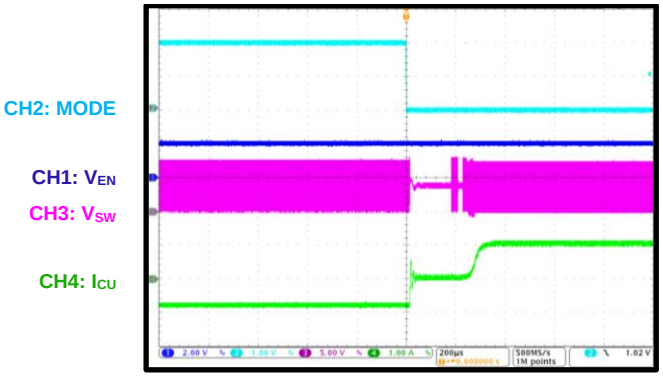
Boost-Balance Mode Enable/Disable via EN



Transient from Buck-Balance Mode to Boost-Balance Mode via MODE



Transient from Boost-Balance Mode to Buck-Balance Mode via MODE



FUNCTIONAL BLOCK DIAGRAM

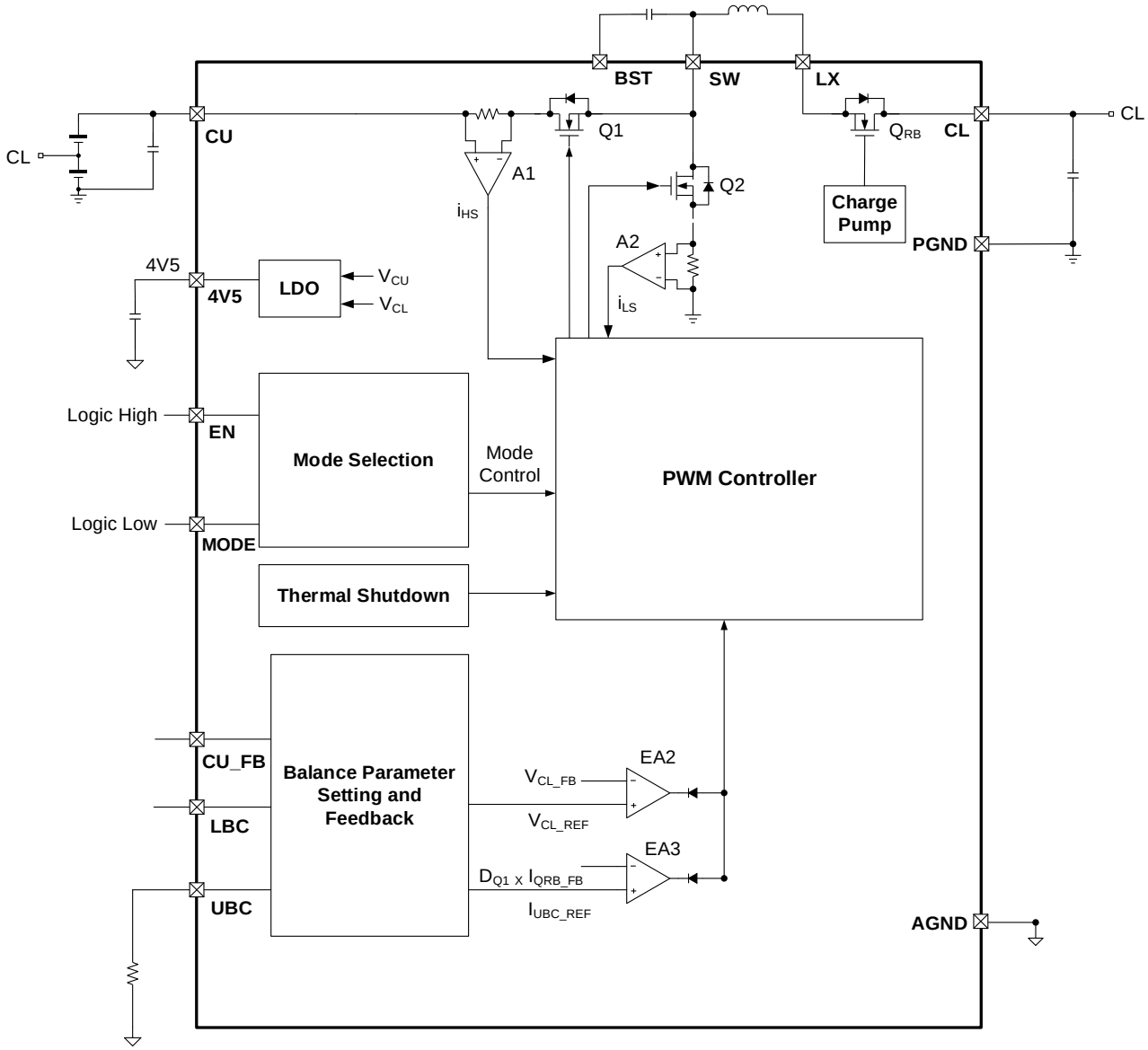


Figure 1: Functional Block Diagram (Buck-Balance Mode)

FUNCTIONAL BLOCK DIAGRAM *(continued)*

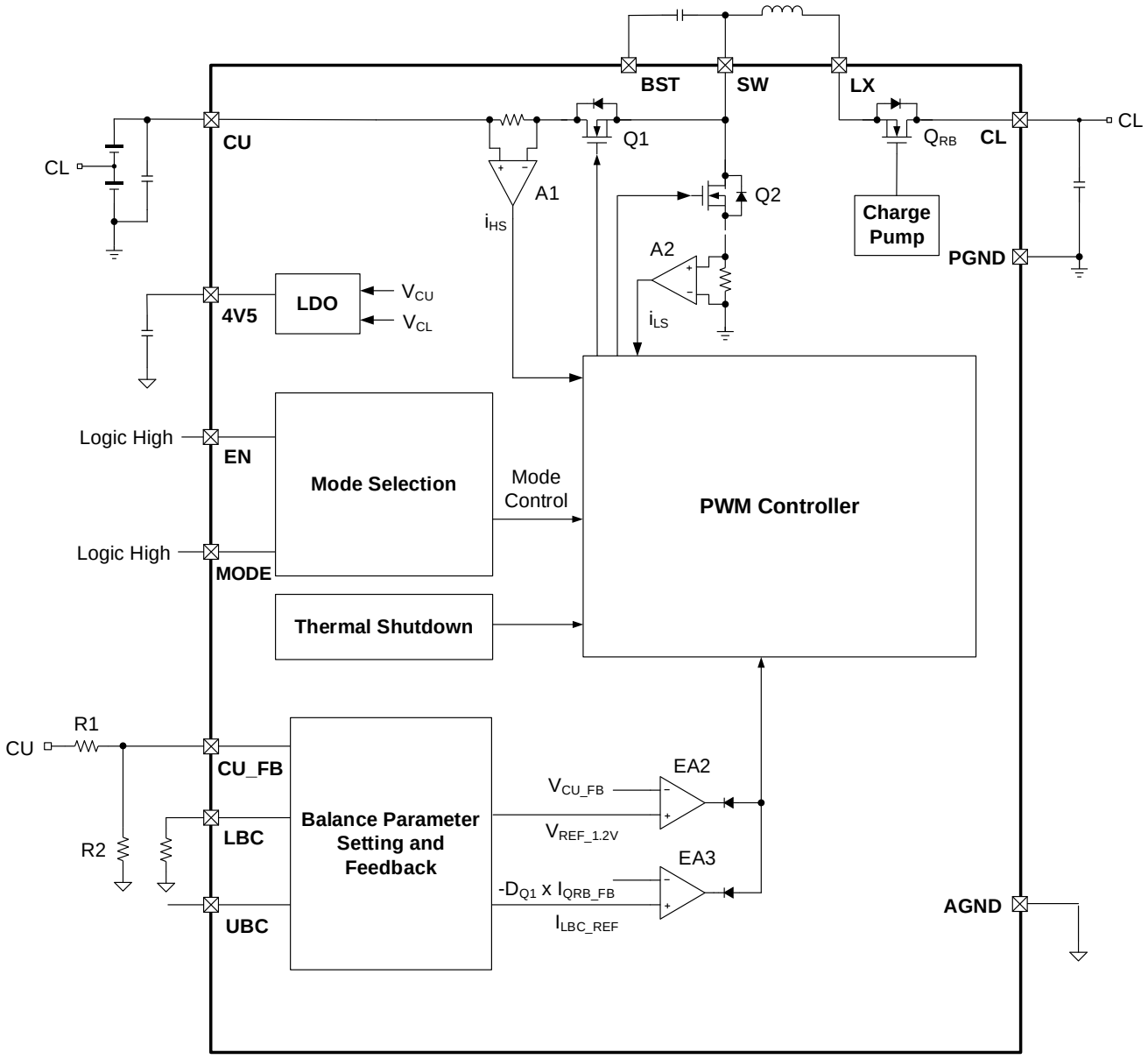


Figure 2: Functional Block Diagram (Boost-Balance Mode)

OPERATION

Introduction

The MP2642 is a highly integrated active balancer designed to transfer charge between two adjacent battery cells for the purpose of balancing the cells. By interleaving these devices, charge can be transferred across many cells in series.

Balance Direction Selection

Buck-balance mode is used to transfer charge from the upper cell to the lower cell. In this mode, the lower cell experiences a net current that is estimated with the buck-balance current (I_{UBC}) (see Figure 3).

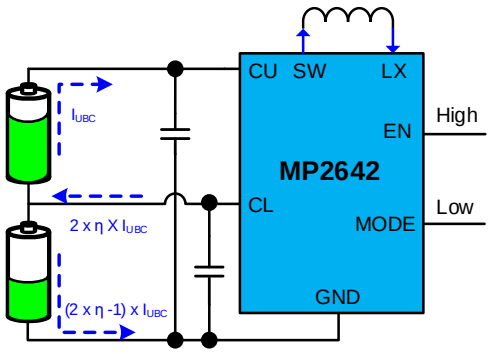


Figure 3: Buck-Balance Mode

This approximation assumes that both cell voltages are the same, such that the net transfer current differs from I_{UBC} by only the buck converter efficiency, η.

Buck-balance is initiated when the MP2642 is enabled by pulling EN high while pulling the MODE pin low. MODE is pulled low internally.

Boost-balance mode transfers charge from the lower cell to the upper cell. In this mode, the upper cell experiences a net current that is estimated with the boost-balance current (I_{LBC}) (see Figure 4).

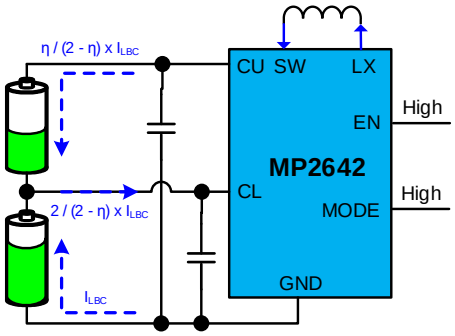


Figure 4: Boost-Balance Mode

This approximation assumes that both cell voltages are the same, such that the net transfer current differs from I_{LBC} by only the boost converter efficiency, η.

Boost-balance is initiated when the MP2642 is enabled by pulling EN high while pulling MODE high.

Internal Power Supply

The MP2642 includes a low-dropout (LDO) regulator (4V5) for the internal circuitry and the MOSFET driver. The LDO regulator only operates while the part is enabled (EN is high). Once the MP2642 is enabled and the 4V5 voltage (V_{4V5}) exceeds the under-voltage lockout (UVLO) threshold, the MP2642 is ready to balance the adjacent cells according to MODE control.

Connect a 1μF ceramic capacitor between the 4V5 and AGND pins. The 4V5 pin can be used to pull up the MP2642's logic pins but is otherwise not recommended for any external loads.

BUCK-BALANCE MODE

To enable buck-balance mode, pull EN high while MODE is low. Buck-balance mode begins if the following conditions are met:

1. EN is high while MODE is low
2. $19.5V > V_{CU} > V_{CU\_UVLO}$
3. $V_{CU} > V_{CL} + 400mV$
4. $V_{CL} < V_{CL\_OVP}$
5. No fault occurs

Buck-Balance Current Setting

The buck-balance current (I_{UBC}) is configured via a single resistor (R_{UBC}) connected between the UBC and AGND pins. I_{UBC} can be calculated with Equation (1):

$$I_{UBC} = \frac{640}{3 \times R_{UBC}} \quad (1)$$

Where I_{UBC} is in A, and R_{UBC} is in kΩ.

I_{UBC} must be limited to a maximum of 1A.

CL Voltage Limit Setting

The MP2642 includes a built-in lower cell voltage limit (V_{CL_LIM}) of 4.35V. During buck balancing, when the CL voltage (V_{CL}) rises to this limit, the MP2642 gradually reduces the balance current to avoid exceeding the voltage limit. If the lower cell voltage (V_{CL_OVP}) exceeds 4.6V, the MP2642 suspends buck-balance immediately.

BOOST-BALANCE MODE

To enable boost-balance mode, pull EN high while MODE is high. Boost balancing begins if the following conditions are met:

1. EN is high while MODE is high
2. $V_{CU\_OVP} > V_{CU} > V_{CU\_UVLO}$
3. $V_{CL} > V_{CL\_UVLO}$
4. No fault occurs

Boost-Balance Current Setting

In boost-balance mode, the balance current (I_{LBC}) is configured via a single resistor (R_{LBC}) connected between the LBC and AGND pins. I_{LBC} can be calculated with Equation (2):

$$I_{LBC} = \frac{V_{CU} - \eta \times V_{CL}}{\eta \times V_{CL}} \times \frac{640}{3 \times R_{LBC}} (A) \quad (2)$$

Where R_{LBC} is in kΩ, η is the boost-balance efficiency, V_{CL} is the lower cell voltage between the CL and AGND pins, and V_{CU} is the voltage of the upper and lower cells between the CU and AGND pins. V_{CL} and V_{CU} are measured without balancing enabled.

To determine I_{LBC}, the boost-balance efficiency (η) must be calculated. Table 2 shows the η selection, where η depends on the cell voltage.

Table 2: η Selection

V_{CL} (V)	η
<3.65V	0.89
≥3.65V	0.91

I_{LBC} is not a fixed current. During the boost balancing process, I_{LBC} changes depending on the cell voltages. Equation (2) also can be used to calculate R_{LBC} according to the sensed cell voltages when balance is disabled.

I_{LBC} can be configured to maximum of 1A.

CU Voltage Limit Setting in Boost-Balance Mode

The MP2642 provides resistor-configurable voltage limits on V_{CU} (V_{CU_LIM} and V_{CU_OVP}). When V_{CU} reaches V_{CU_LIM}, the MP2642 holds the boost voltage by adjusting the boost regulator duty cycle. If V_{CU} exceeds the CU over-voltage protection (OVP) threshold (V_{CU_OVP}), the MP2642 disables boost balancing and turns off the reverse-blocking MOSFET (Q_{RB} FET). When V_{CU} returns to a safe level, boost balancing restarts.

V_{CU_LIM} and V_{CU_OVP} are set via the voltage divider connected between the CU, CU_FB, and PGND pins. V_{CU_LIM} can be calculated with Equation (3):

$$V_{CU\_LIM} = V_{CU\_LIM\_REF} \times \frac{R1+R2}{R2} (V) \quad (3)$$

Where $V_{CU\_LIM\_REF}$ is the reference V_{CU}, which is 1.2V.

V_{CU_OVP} can be calculated with Equation (4):

$$V_{CU\_OVP} = V_{CU\_OVP\_REFBST} \times \frac{R1+R2}{R2} (V) \quad (4)$$

Where the reference of the CU output over-voltage (OV) threshold comparator ($V_{CU\_OVP\_REFBST}$) depends on the V_{CU_LIM} setting (see $V_{CU\_OVP\_REFBST}$ in the Electrical Characteristics section on page 6).

APPLICATION INFORMATION

Setting the Buck-Balance Current

The MP2642's buck-balance current (I_{UBC}) can be configured between 0.5A and 1A via a single resistor (R_{UBC}) connected between the UBC and AGND pins. By rewriting Equation (1) from page 13, R_{UBC} given a target I_{UBC} can be calculated with Equation (5):

$$R_{UBC} = \frac{640}{3 \times I_{UBC}} (k\Omega) \quad (5)$$

Using this calculated R_{UBC}, select the closest available resistance.

Calculating the Minimum and Maximum Buck-Balance Current

Once a resistance is selected, the minimum and maximum range of I_{UBC} can be estimated by considering the I_{UBC} tolerance (ΔI_{UBC}) and the resistor tolerance (ΔR). The MP2642 ΔI_{UBC} is ±10%.

Determining the Maximum Buck-Balance Current Range

Consider an example where R_{UBC} is calculated for a target I_{UBC}, as well as the I_{UBC} minimum and maximum range based on ΔR and ΔI_{UBC}. If V_{CU} is 7V, V_{CL} is 3.6V, and I_{UBC} is 1A, then R_{UBC} is determined to be 213.3kΩ based on Equation (5). Using a 1% resistor tolerance, the closest standard resistance is 215kΩ. With a ΔI_{UBC} of 10% and a ΔR of 1%, Table 3 shows the I_{UBC} range between 0.88A and 1.102A, with a typical value (I_{UBC_TYP}) at the target 2A.

Table 3: I_{UBC} Range when Setting I_{UBC_TYP}

Parameter	R_{UBC} (kΩ)	Typ I_{UBC} (A)	Min I_{UBC} (-10%) (A)	Max I_{UBC} (+10%) (A)
Typ R	215	1	0.9	1.1
Min R	212.85	1.002	0.902	1.102
Max R	217.15	0.982	0.884	1.08

Setting the Maximum Buck-Balance Current

Consider the R_{UBC} accuracy and the I_{UBC} tolerance to set a maximum I_{UBC} (I_{UBC_MAX}). The minimum R_{UBC} (R_{UBC_MIN}) can be calculated with Equation (6):

$$R_{UBC\_MIN} = \frac{640 \times (1 + \Delta I_{UBC})}{3 \times I_{UBC\_MAX} \times (1 - \Delta R)} (k\Omega) \quad (6)$$

Select the closest standard resistance that either exceeds or is equal to R_{UBC_MIN}.

Consider an example where R_{UBC} is calculated for a target I_{UBC_MAX} of 1A based on ΔR = ±1% and ΔI_{UBC} = ±10%. R_{UBC_MIN} is 237.04kΩ according to Equation (6). The closest 1% standard resistance that either exceeds or is equal to R_{UBC_MIN} is 240kΩ. Table 4 shows I_{UBC_MIN} and I_{UBC_MAX}, based on a 240kΩ 1% resistor. I_{UBC} does not exceed I_{UBC_MAX}, which is 1A.

Table 4: I_{UBC} Range when Setting I_{UBC_MAX}

Parameter	R_{UBC} (kΩ)	Typ I_{UBC} (A)	Min I_{UBC} (-10%) (A)	Max I_{UBC} (+10%) (A)
Typ R	240	0.89	0.8	0.98
Min R	237.6	0.9	0.81	0.99
Max R	242.4	0.88	0.79	0.97

Setting the Minimum Buck-Balance Current

To set the minimum I_{UBC} (I_{UBC_MIN}), the maximum R_{UBC} (R_{UBC_MAX}) can be calculated with Equation (7):

$$R_{UBC\_MAX} = \frac{640 \times (1 - \Delta I_{UBC})}{3 \times I_{UBC\_MIN} \times (1 + \Delta R)} (k\Omega) \quad (7)$$

Select the closest standard resistance that is either below or equal to R_{UBC_MAX}.

Consider an example where R_{UBC} is calculated for a target I_{UBC_MIN} based on ΔR = ±1% and ΔI_{UBC} = ±10%. R_{UBC_MAX} is 380kΩ according to Equation (7). The closest 1% standard resistance that is either below or equal to R_{UBC_MAX} is 374kΩ. Table 5 shows I_{UBC_MIN} and I_{UBC_MAX} based on a 374kΩ 1% resistor. I_{UBC} does not drop below I_{UBC_MIN}, which is 0.5A.

Table 5: I_{UBC} Range when Setting I_{UBC_MIN}

Parameter	R_{UBC} (kΩ)	Typ I_{UBC} (A)	Min I_{UBC} (-10%) (A)	Max I_{UBC} (+10%) (A)
Typ R	374	0.57	0.531	0.627
Min R	370.26	0.576	0.518	0.634
Max R	377.74	0.565	0.508	0.622

Setting the Boost-Balance Current

The MP2642's boost-balance current (I_{LBC}) can be configured between 0.5A and 1A via an external resistor (R_{LBC}) connected between the LBC and AGND pins. By rewriting Equation (2) from page 13, R_{LBC} given a target I_{LBC} can be calculated with Equation (8):

$$R_{LBC} = \frac{V_{CU} - \eta \times V_{CL}}{\eta \times V_{CL}} \times \frac{640}{3 \times I_{LBC}} (k\Omega) \quad (8)$$

Where η is the boost-balance efficiency, V_{CL} is the lower cell voltage between CL and AGND, and V_{CU} is the voltage of both series cells between CU and AGND.

Based on this calculated resistance, the closest available resistance should be selected.

Calculating the Minimum and Maximum Boost-Balance Current

For a given configuration, the minimum and maximum I_{LBC} (I_{LBC_MIN} and I_{LMC_MAX}, respectively) can be estimated by considering the I_{LBC} tolerance (ΔI_{LBC}), R_{LBC}, tolerance (ΔR), and the variation in the cell voltages (V_{CU} and V_{CL}) during operation. The MP2642's maximum ΔI_{LBC} is ±10%.

Based on Equation (2) on page 13, I_{LBC_MAX} occurs when both the cell voltages are the closest to being equal, and I_{LBC_MIN} occurs at the largest difference between the cell voltages. Therefore, the ratio of V_{CU} / V_{CL} for I_{LBC_MAX} and I_{LBC_MIN} can be estimated using the voltage difference that initiates balancing and the voltage difference that ends balancing. For example, if boost-balance mode is initiated when V_{CL} is 3.7V and V_{CU} is 7V, then V_{CU} / V_{CL} is 1.9. If boost-balance mode is finished when V_{CL} is 3.6V, V_{CU} is 7.2V, and V_{CU} / V_{CL} is 2.

Equation (8) can then be simplified, where R_{LBC} can be calculated with Equation (9):

$$R_{LBC} = \left(\frac{V_{CU}}{\eta \times V_{CL}} - 1 \right) \times \frac{640}{3 \times I_{LBC}} (k\Omega) \quad (9)$$

Determining the Boost-Balance Range

Consider an example where R_{LBC} can be calculated for a target typical I_{LBC} balance current of 1A. To determine the full I_{LBC} range during the balancing process, assume that the cell voltages start with V_{CL} = 3.6V and V_{CU} = 7V, and end with V_{CL}= 3.5V and V_{CU} = 7V. Based on Table 2 on page 13, η is 0.89 since V_{CL} is below 3.65V.

Using Equation (9) combined with V_{CU} / V_{CL} = 2 (corresponding to the balance end point), I_{LBC_MAX} can be calculated with Equation (10):

$$I_{LBC\_MAX} = 1.247 \times \frac{640}{3 \times R_{LBC}} (A) \quad (10)$$

Using Equation (9) combined with V_{CU} / V_{CL} = 1.94 (corresponding to the balance beginning point), I_{LBC_MIN} can be calculated with Equation (11):

$$I_{LBC\_MIN} = 1.185 \times \frac{640}{3 \times R_{LBC}} (A) \quad (11)$$

Using Equation (9) combined with the average V_{CU} / V_{CL} = 1.97, the typical I_{LBC} (I_{LBC_TYP}) can be calculated with Equation (12):

$$I_{LBC\_TYP} = 1.216 \times \frac{640}{3 \times R_{LBC}} (A) \quad (12)$$

By rewriting Equation (12), R_{LBC} for a typical I_{LBC} can be calculated with Equation (13):

$$R_{LBC\_TYP} = 1.216 \times \frac{640}{3 \times I_{LBC}} (k\Omega) \quad (13)$$

Based on Equation (13), R_{LBC} is 259.4kΩ for a typical I_{LBC} of 1A. Using 1% resistor tolerance (ΔR = 1%), the closest standard resistance is 261kΩ.

For Equation (10), Equation (11), and Equation (12), if R_{LBC} is 261kΩ, ΔI_{LBC} is 10% and ΔR is 1%, I_{LBC} ranges between 0.86A and 1.133A during the balancing operation. Table 6 shows the I_{LBC} range when setting the typical I_{LBC} (I_{LBC_TYP}).

Table 6: I_{LBC} Range when Setting I_{LBC_TYP}

Parameter	R_{LBC} (kΩ)	Typ I_{LBC} (A)	Min I_{LBC} (-10%) (A)	Max I_{LBC} (+10%) (A)
Typ R	261	0.994	0.87	1.121
Min R	258.39	1.004	0.88	1.133
Max R	263.61	0.984	0.863	1.11

Setting the Maximum Boost-Balance Current

I_{LBC_MAX} corresponds to the lowest R_{LBC}, meaning the minimum R_{LBC} (R_{LBC_MIN}) must be determined first to ensure I_{LBC} does not exceed its target maximum. R_{LBC_MIN} can be calculated by considering the I_{LBC} tolerance (ΔI_{LBC}) and resistor tolerance (ΔR). Based on Equation (9), R_{LBC_MIN} (in kΩ) can be calculated with Equation (14):

$$R_{LBC\_MIN} = \left(\frac{V_{CU}}{\eta \times V_{CL}} - 1\right) \times \frac{640 \times (1 + \Delta I_{LBC})}{3 \times I_{LBC\_MAX} \times (1 - \Delta R)} \quad (14)$$

Consider an example where R_{LBC_MIN} is calculated for a target I_{LBC_MAX} of 1A. If ΔR is ±1%, ΔI_{LBC} is ±10%, V_{CL} is 3.6V, and V_{CU} is 7V at the start of balancing, then V_{CL} is 3.5V and V_{CU} is 7V at the end of balancing, and η is 0.89.

From Equation (14), R_{LBC_MIN} occurs when the cell voltages are the closest to being equal, which corresponds to the end of balancing. In this example, both cells have equal voltages at the end of balancing (V_{CU} = 2 x V_{CL}). Entering these variables into Equation (14), R_{LBC_MIN} is 295.6kΩ. This is the lowest resistance that ensures the target I_{LBC_MAX}. The closest standard resistance that either exceeds or is equal to R_{LBC_MIN} is 300kΩ.

Table 7 shows the results from entering these variables into Equation (2) on page 13 and confirms that I_{LBC} remains below I_{LBC_MAX}, which is 1A.

Table 7: I_{LBC} Range when Setting I_{LBC_MAX}

Parameter	R_{LBC} (kΩ)	Typ I_{LBC} (A)	Min I_{LBC} (-10%) (A)	Max I_{LBC} (+10%) (A)
Typ R	300	0.865	0.76	0975
Min R	297	0.875	0.765	0.985
Max R	303	0.855	0.75	0.965

Setting the Minimum Boost-Balance Current

I_{LBC_MIN} corresponds to the highest R_{LBC}, meaning the maximum R_{LBC} (R_{LBC_MAX}) must be determined first to ensure that I_{LBC} does not drop below the target minimum. R_{LBC_MAX} can be calculated by considering the I_{LBC} tolerance (ΔI_{LBC}) and resistor tolerance (ΔR).

Based on Equation (9), R_{LBC_MAX} (in kΩ) can be calculated with Equation (15):

$$R_{LBC\_MAX} = \left(\frac{V_{CU}}{\eta \times V_{CL}} - 1\right) X \frac{640 \times (1 - \Delta I_{LBC})}{3 \times I_{LBC\_MAX} \times (1 + \Delta R)} \quad (15)$$

Example: Setting Minimum I_{LBC} Current

Consider an example where R_{LBC_MAX} is calculated for a target I_{LBC_MIN} of 0.5A. If ΔR is ±1%, ΔI_{LBC} is ±10%, V_{CL} is 3.6V, and V_{CU} is 7V at the start of balancing, then V_{CL} is 3.5V and V_{CU} is 7V at the end of balancing, and η is 0.89.

From Equation (15), R_{LBC_MAX} occurs at the largest difference between the cell voltages, which corresponds to the start of balancing. In this example, there is a 200mV difference between the cell voltages at the start of balancing (V_{CU} = 1.94 x V_{CL}). Entering these variables into Equation (15), R_{LBC_MAX} is 450.5kΩ. This is the highest resistance that ensures the target I_{LBC_MIN}. The closest standard resistance that either is below or equal to R_{LBC_MAX} is 442kΩ.

Table 8 shows the results from entering these variables into Equation (2) on page 13 and confirms that I_{LBC} remains above I_{LBC_MIN}, which is 0.5A.

Table 8: I_{LBC} Range when Setting I_{LBC_MIN}

Parameter	R_{LBC} (kΩ)	Typ I_{LBC} (A)	Min I_{LBC} (-10%) (A)	Max I_{LBC} (+10%) (A)
Typ R	442	0.587	0.515	0.662
Min R	437.5	0.593	0.52	0.669
Max R	446.4	0.581	0.509	0.655

Setting the CU Limit Voltage in Boost-Balance Mode

The MP2642 includes an upper cell voltage limit (V_{CU_LIM}) that can regulate the CU pin voltage (V_{CU}) in boost-balance mode. When V_{CU} reaches V_{CU_LIM}, the MP2642 holds the boost voltage by adjusting the boost regulator duty cycle, provided V_{CU} does not exceed the CU over-voltage protection (OVP) threshold (V_{CU_OVP}). V_{CU_LIM} and V_{CU_OVP} are fixed at the same resistance.

V_{CU} is the combined voltage of both series cells. V_{CU_LIM} should be set to the target limit of the combined cells, and is set via a resistor divider (for more details, see Equation (3) on page 13. Equation (3) can be rewritten to determine the resistance for a given V_{CU_LIM}, which is denoted as R2. R2 can be calculated with Equation (16):

$$R2 = \frac{R1 \times V_{CU\_LIM\_REF}}{V_{CU\_LIM} - V_{CU\_LIM\_REF}} (k\Omega) \quad (16)$$

A 2MΩ 1% resistor is recommended for R1.

Example: Calculating R2 for a Target V_{CU_LIM}

Based on Equation (3), if R1 is 2MΩ and the target V_{CU_LIM} is 7.17V, R2 is 400kΩ.

The closest 1% standard resistance for R2 is 402kΩ. According to Equation (3), the resulting V_{CU_LIM} is 7.17V and V_{CU_OVP} is 8.07V. When V_{CU} reaches 7.17V, the MP2642 holds the boost voltage by adjusting the boost regulator duty cycle. If V_{CU} exceeds 8.07V, the MP2642 disables the boost balance and turns off the reverse-blocking MOSFET (Q_{RB} FET). When V_{CU} returns to a safe level, boost-balance restarts.

Selecting the Inductor

Inductor selection requires a tradeoff between cost, size, and efficiency. A lower inductance corresponds to a smaller size, but results in higher ripple currents, magnetic hysteretic losses, and output capacitances. The inductor ripple current (ΔI_L) should not exceed 30% of the maximum balance current under the worst-case conditions. For example, if I_{UBC} is 1A, then ΔI_L is generally set to 0.3A.

Under light-load conditions, ΔI_L is very small, which may result in unstable operation due to the IC's peak current mode control. For stable operation, the minimum limit for ΔI_L is 0.5A. Therefore, ΔI_L is 30% of the maximum balance current between I_{UBC} and 0.5A.

The inductance (L) can be calculated with Equation (17):

$$L = \frac{V_{CU} - V_{CL}}{\Delta I_L} \times \frac{V_{CL}}{V_{CU} \times f_{SW}(MHz)} (\mu H) \quad (17)$$

The inductor peak current (I_{PEAK}) can be calculated with Equation (18):

$$I_{PEAK} = I_{BALANCE} + \Delta I_L \quad (18)$$

Where V_{CU} is the total voltage of the two cells in series, V_{CL} is the lower cell voltage, and f_{SW} is the switching frequency.

Table 9 shows the inductor selection guide.

Table 9: Inductor Selection Guide

Spec	Conditions	L_{MIN} (µH)	L_{MAX} (µH)	L (µH)	Saturation Current (A) (7)	DCR (mΩ)	Package
V_{CU} = 6.2V, V_{CL} = 3V, I_{UBC} = 1A	ΔI_L = max (0.3 x I_{UBC} / duty, 0.5A), ΔI_{L_MIN} = 0.5A, ΔI_{L_MAX} = 0.62A	2.497	3.26	2.2	>3.25	<50	Application required

Note:

7) The inductor's saturation current must exceed I_{PEAK}, with an additional 0.5A margin.

Selecting the CU Capacitor

The CU port is the converter's input during buck balancing, and the converter's output during boost balancing. The CU capacitor (C_{CU}) absorbs the ripple current from the pulse-width modulation (PWM) converter.

In buck-balance mode, C_{CU} is the converter's input capacitor. The input current ripple (I_{RIP_MAX}) can be calculated with Equation (19):

$$I_{RIP\_MAX} = I_{UBC\_MAX} \times \sqrt{(V_{CU\_MAX} - V_{CL\_MIN}) / V_{CL\_MIN}} \quad (19)$$

In boost-balance mode, C_{CU} is the converter's output capacitor. Maintain a small CU ripple (<0.5%) to ensure feedback loop stability.

If I_{UBC_MAX} is 1A, V_{CL_MIN} is 2.4V, and V_{CU_MAX} is 7.2V, then the maximum ripple current is 0.47A. Select the input capacitors to ensure that the temperature rise caused by the ripple current does not exceed 10°C. It is recommended to use 10µF ceramic capacitors with X5R or X7R dielectrics, as well as low ESR and small temperature coefficients. A capacitor with a minimum 16V rating is recommended for a 7.2V input voltage.

The input decoupling capacitor should be placed as close as possible to the CU and PGND pins.

Selecting the CL Capacitor

Select the CL capacitor (C_{CL}) based on the demand of the system current ripple.

C_{CL} is the converter's output capacitor during boost balancing and the converter's input capacitor during buck balancing.

The V_{CL} ripple ratio (Δr_{VCL}) can be calculated with Equation (20):

$$\Delta r_{VCL} = \frac{\Delta V_{CL}}{V_{CL}} = \frac{1 - V_{CL} / V_{CU}}{8 \times C_{CL} \times f_{SW}^{2} \times L} \quad (20)$$

C_{CL} can be calculated with Equation (21):

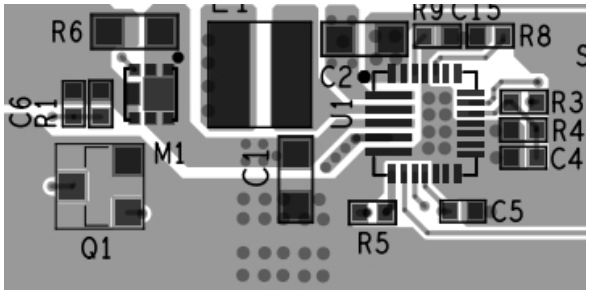
$$C_{CL} = \frac{1 - V_{CL\_MIN} / V_{CU\_LIM}}{8 \times \Delta r_{VCL\_MIN} \times f_{SW}^{2} \times L} \quad (21)$$

The capacitance is not recommended to be below 10µF, meaning the 16V rating capacitor is sufficient.

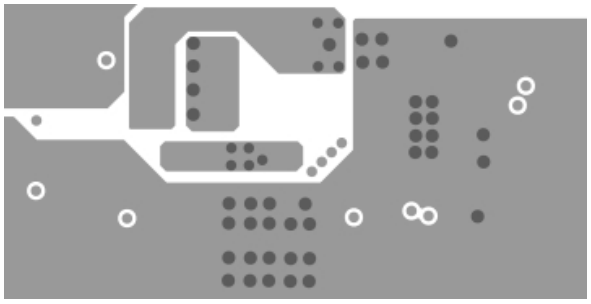
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, especially to meet the specified noise and efficiency requirements. A 4-layer layout is strongly recommended. Additional layers may be required for multi-chip applications. For the best results, refer to Figure 5 and follow the guidelines below:

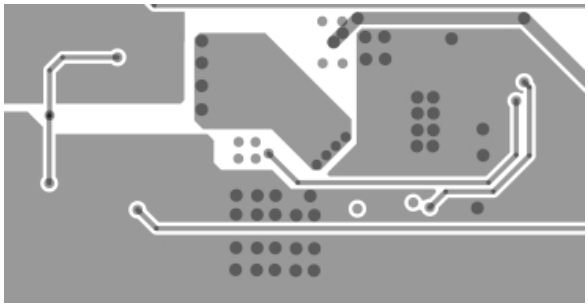
1. Route the loop of the power stages as short as possible.
2. Route the PGND copper for the CL and CU capacitors together using the shortest possible trace.
3. Place the PGND copper of the CL and CU capacitors as close as possible to the PGND pin and the IC's thermal pad using as much copper area as possible.
4. Place the CU and CL as close to the IC pins as possible.
5. Keep the switching node short, and route it away from all small control signals.
6. Place the BST capacitor (C_{BST}) between the SW and BST pins.
7. If there is a resistor in series with C_{BST}, make the RC route as short as possible, and place C_{BST} as close to the IC pin as possible.
8. Place the decoupling capacitors (e.g. VCC capacitor) as close to the IC pin as possible.
9. Connect the IC's power pins (CU, CL, and PGND) to as many copper planes as possible for improved thermal performance.



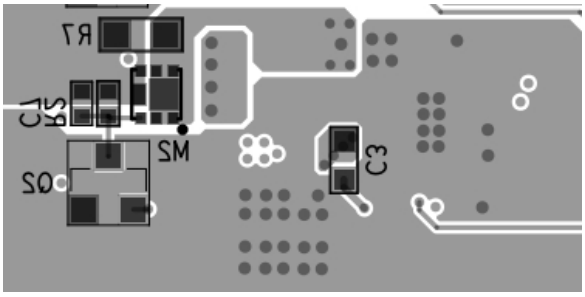
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

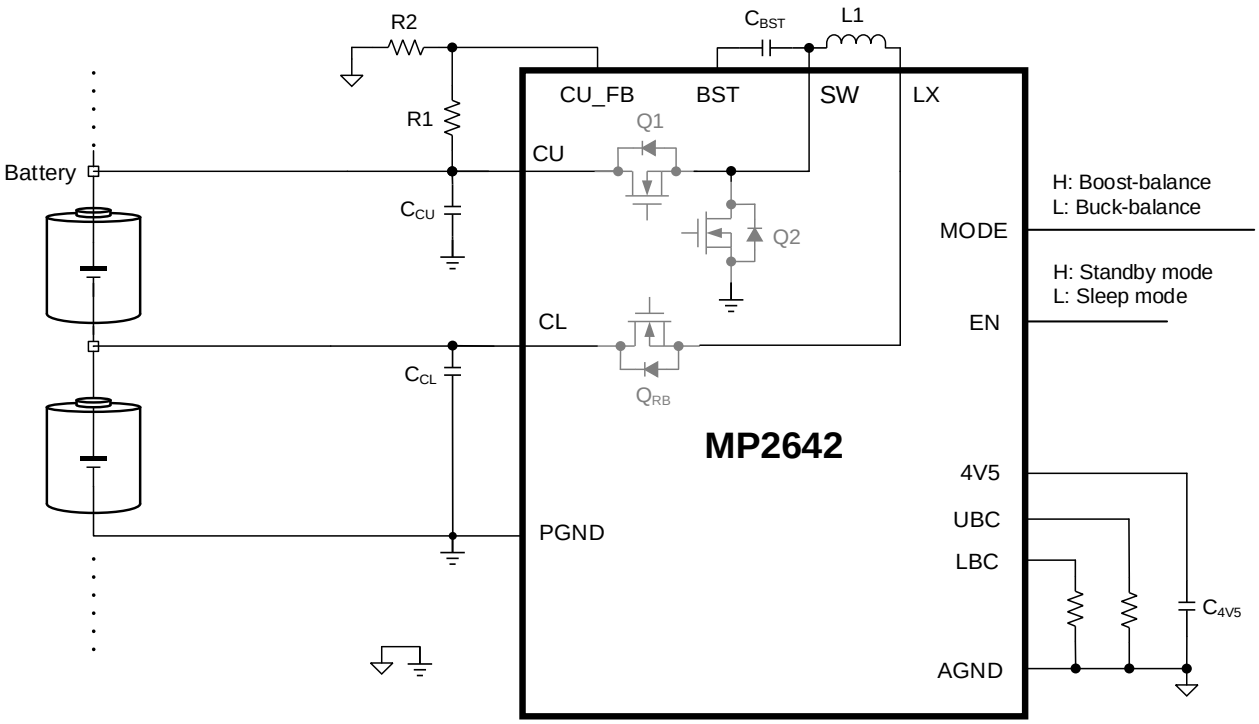


Figure 6: Typical Application Circuit

Table 10: Key BOM for Figure 6

Qty	Ref	Value	Description	Package	Manufacturer
1	C_{CU}	10µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C_{CL}	10µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C_{4V5}	1µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any

TYPICAL APPLICATION CIRCUITS *(continued)*

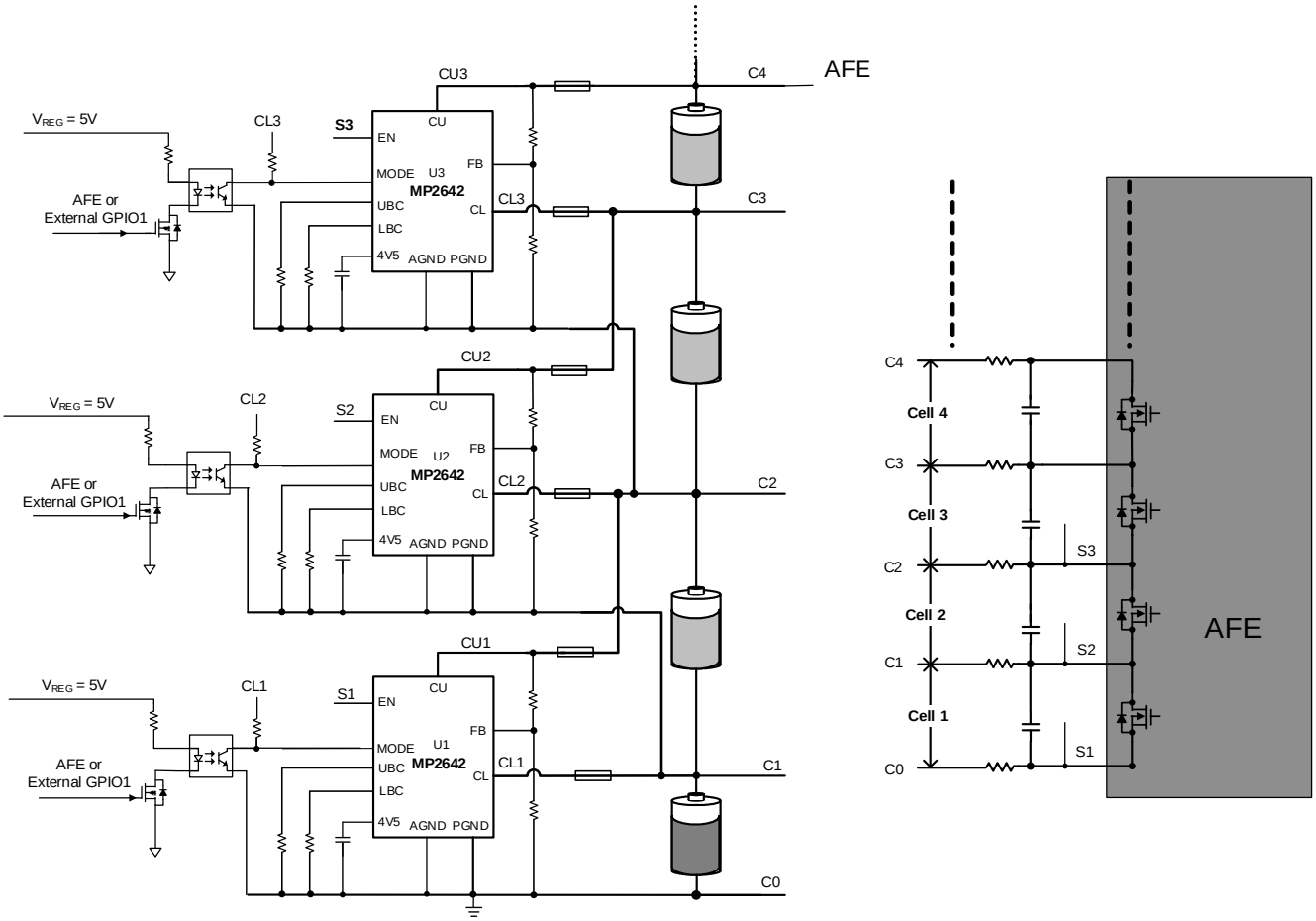
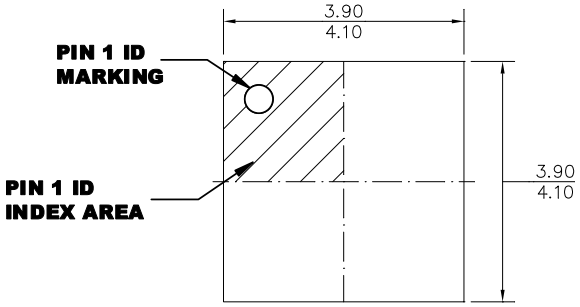


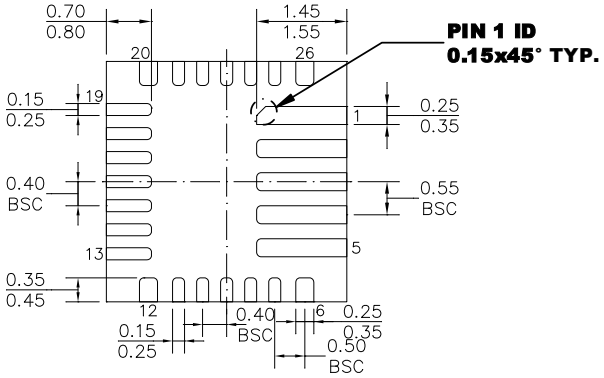
Figure 7: Typical Application Circuit (for ESS Applications)

PACKAGE INFORMATION

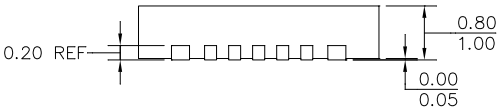
QFN-26 (4mmx4mm)



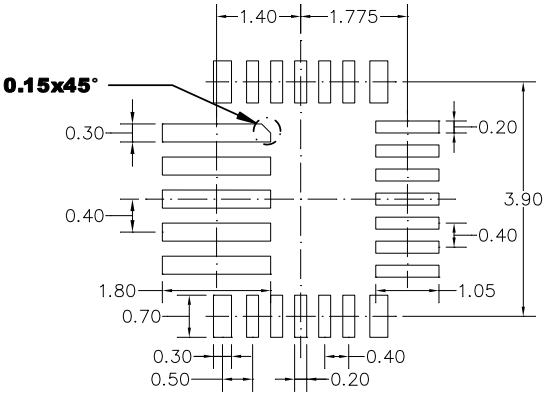
TOP VIEW



BOTTOM VIEW



SIDE VIEW

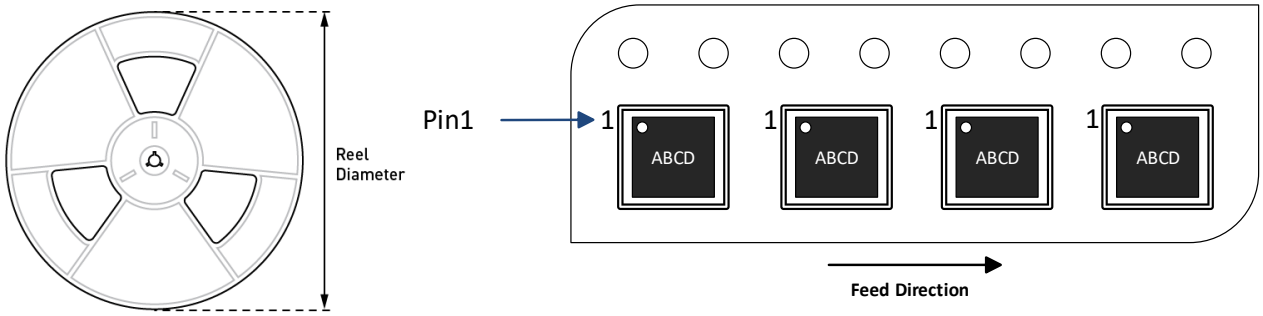


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) DRAWING CONFORMS TO JEDEC MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2642GR-Z	QFN-26 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/2/2025	Initial Release	-