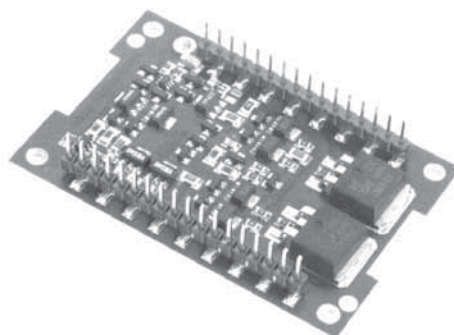


Power Operational Amplifier

RoHS
COMPLIANT

FEATURES

- Low Cost
- High Voltage - 100V
- High Output Current- 50A Pulse Output, 15A Continuous
- 170W Dissipation Capability
- 130V/ μ s Slew Rate
- 500 kHz Power Bandwidth



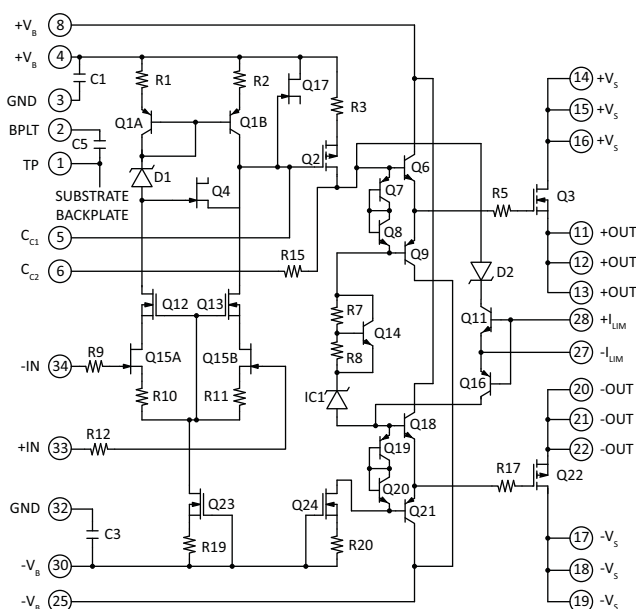
APPLICATIONS

- Inkjet Printer Head Drive
- Piezo Transducer Drive
- Industrial Instrumentation
- Reflectometers
- Ultra-sound Transducer Drive

DESCRIPTION

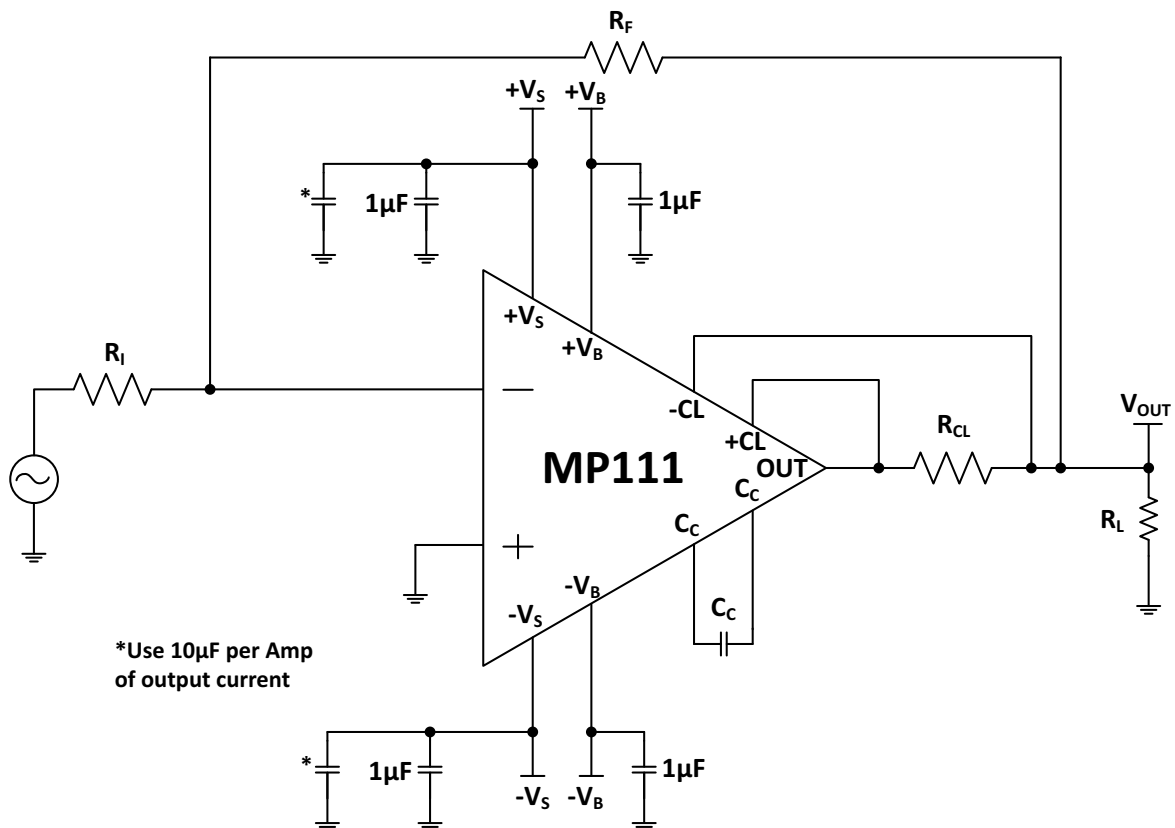
The MP111 operational amplifier is a surface mount constructed component that provides a cost-effective solution in many industrial applications. The MP111 offers outstanding performance that rivals much more expensive hybrid components yet has a footprint of only 4 sq in. The MP111 has many optional features such as four-wire current limit sensing and external compensation. The 500 kHz power bandwidth, 15A continuous, and 50A pulse output of the MP111 makes it a good choice for piezo transducer drive applications. The MP111 is built on a thermally conductive but electrically insulating substrate that can be mounted to a heat sink.

Figure 1: Equivalent Schematic



TYPICAL CONNECTION

Figure 2: Typical Connection



EXTERNAL CONNECTIONS

Figure 3: Pin-out

		-IN	34
		+IN	33
1	TP	GND	32
2	BPLT	NC	31
3	GND	-V _B	30
4	+V _B	NC	29
5	C _{C1}	+CL	28
6	C _{C2}	-CL	27
7	NC	NC	26
8	+V _B	-V _B	25
9	NC	NC	24
10	NC	NC	23
11	+OUT	-OUT	22
12	+OUT	-OUT	21
13	+OUT	-OUT	20
14	+V _S	-V _S	19
15	+V _S	-V _S	18
16	+V _S	-V _S	17

**MP111
(back view)**

Pin Number	Name	Description
1	TP	Apex test pin, do not connect.
2	BPLT	AC coupling to backplate. Connect to signal ground.
3, 32	GND	Ground. Pins 3 and 32 are not connected on the unit. Connect both pins to system signal ground.
4, 8	+V _B	The positive boost supply rail. Short to +V _S if unused. See applicable section.
5, 6	C _C	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
11, 12, 13	+OUT	The positive current output. Short to -OUT pins. Connect these pins to the MP111 side of the current limit resistor and the +CL pin. Output current is sourced from these pins through the current limit resistor and to the load.
14, 15, 16	+V _S	The positive supply rail.
17, 18, 19	-V _S	The negative supply rail.
20, 21, 22	-OUT	The negative current output. Short to +OUT pins. Connect these pins to the MP111 side of the current limit resistor and the +CL pin. Output current sinks to these pins through the current limit resistor from the load.
25, 30	-V _B	The negative boost supply rail. Short to -V _S if unused. See applicable section.
27	-CL	Connect to the load side of the current limit resistor and feedback resistor. Current limit will activate if the voltage across R _{CL} exceeds 0.65V.
28	+CL	Connect to the OUT side of the current limit resistor. Current limit will activate if the voltage across R _{CL} exceeds 0.65V.
33	+IN	The non-inverting input.
34	-IN	The inverting input.
All Others	NC	No Connection.

SPECIFICATIONS

Unless otherwise noted: $T_C = 25^\circ\text{C}$, $C_C = 100\text{pF}$. DC input specifications are value given. Power supply voltage is typical rating.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		100	V
Supply Voltage ¹	$+V_B$		$+V_S + 15$	V
Supply Voltage ¹	$-V_B$		$-V_S - 15$	V
Output Current, peak, within SOA	I_{OUT}		50	A
Power Dissipation, internal DC	P_D		170	W
Input Voltage, common mode	V_{CM}		$+V_B$ to $-V_B$	V
Input Voltage, differential	$V_{IN (Diff)}$	-25	+25	V
Temperature, pin solder, 10s max.			225	$^\circ\text{C}$
Temperature, junction ²	T_J		175	$^\circ\text{C}$
Temperature Range, storage		-40	+105	$^\circ\text{C}$
Operating Temperature Range, case	T_C	-40	+85	$^\circ\text{C}$

1. Power supply voltages $+V_B$ and $-V_B$ must not be less than $+V_S - 0.6\text{V}$ and $-V_S + 0.6\text{V}$ respectively.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

INPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Offset Voltage, initial			1	5	mV
Offset Voltage vs. Temperature	Full temp range		50		$\mu\text{V}/^\circ\text{C}$
Offset Voltage vs. Supply				20	$\mu\text{V}/\text{V}$
Bias Current, initial ¹				100	pA
Bias Current vs. Supply				0.1	pA/V
Offset Current, initial				50	pA
Input Impedance, DC			10^{11}		Ω
Input Capacitance			4		pF
Common Mode Voltage Range				$\pm V_B -/+15$	V
Common Mode Rejection, DC		92			dB
Noise	1 MHz BW, $R_S = 1\text{ k}\Omega$		10		$\mu\text{V RMS}$

1. Doubles for every 10°C of case temperature increase.

GAIN

Parameter	Test Conditions	Min	Typ	Max	Units
Open Loop @ 15 Hz	$R_L = 10\text{ k}\Omega$, $C_C = 33\text{ pF}$	96			dB
Gain Bandwidth Product @ 1 MHz	$C_C = 33\text{ pF}$		6		MHz
Phase Margin	Full temp range	45			°
Power Bandwidth 80 V _{P-P}	$C_C = 33\text{ pF}$, $+V_S = 50\text{ V}$, $-V_S = -50\text{ V}$		500		kHz

OUTPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage Swing	$I_{OUT} = 15\text{ A}$	$+V_S - 10$	$+V_S - 8.4$		V
Voltage Swing	$I_{OUT} = -15\text{ A}$	$-V_S + 10$	$-V_S + 5.8$		V
Voltage Swing	$I_{OUT} = 15\text{ A}$, $+V_B = +V_S + 10\text{ V}$	$+V_S - 0.8$			V
Voltage Swing	$I_{OUT} = -15\text{ A}$, $-V_B = -V_S - 10\text{ V}$	$-V_S + 1.0$			V
Current, continuous, DC		15			A
Slew Rate, $A_V = -20$	$C_C = 33\text{ pF}$	100	130		V/ μs
Settling Time to 0.1%	2V step		1		μs
Resistance	No load, DC		3		Ω

POWER SUPPLY

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage		± 15	± 45	± 50	V
Current, quiescent			142	157	mA

THERMAL

Parameter	Test Conditions	Min	Typ	Max	Units
Resistance, AC, junction to case ¹	Full temp range, $F \geq 60\text{ Hz}$			0.65	°C/W
Resistance, DC, junction to case	Full temp range, $F < 60\text{ Hz}$			0.88	°C/W
Resistance, junction to air	Full temp range			13	°C/W
Temperature Range, case		-40		+85	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stage. $+V_B$ and $-V_B$ denote the positive and negative supply voltages to the input stages.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

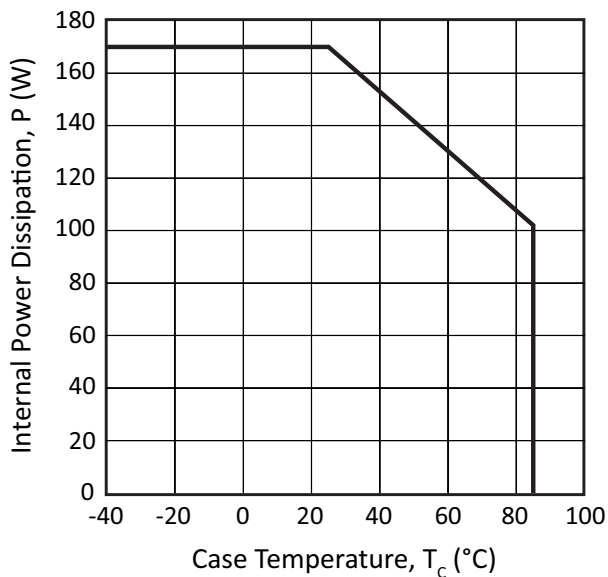


Figure 5: Power Response

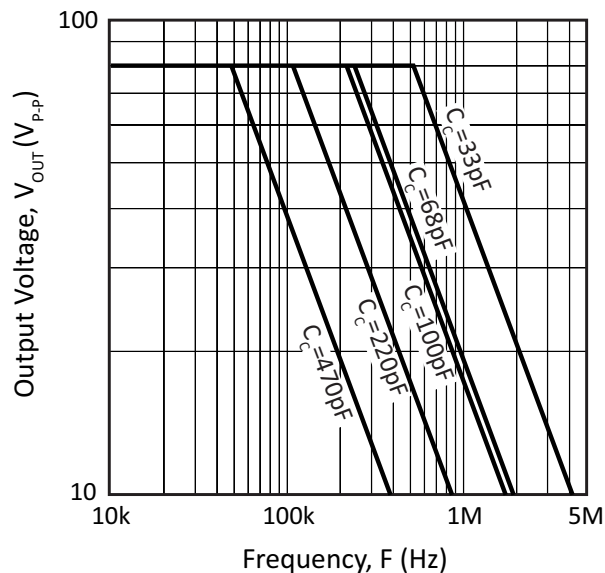


Figure 6: Small Signal Response w/ Boost

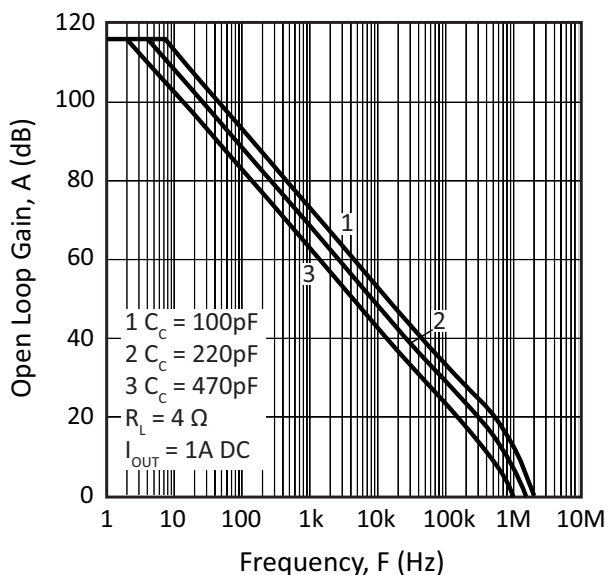


Figure 7: Phase Response w/ Boost

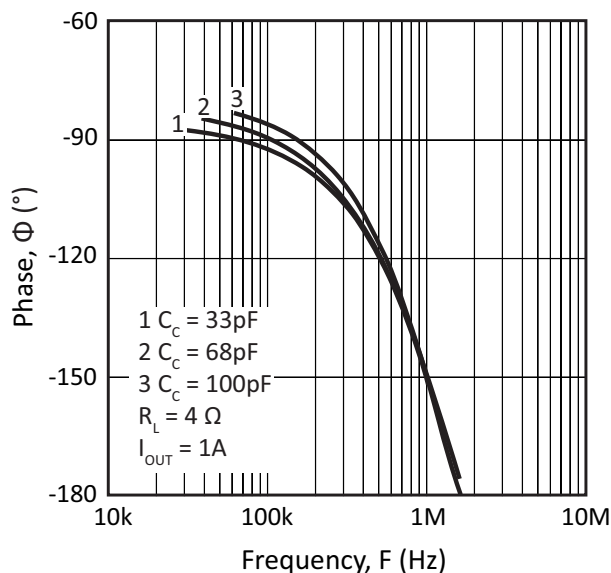


Figure 8: Small Signal Response w/o Boost

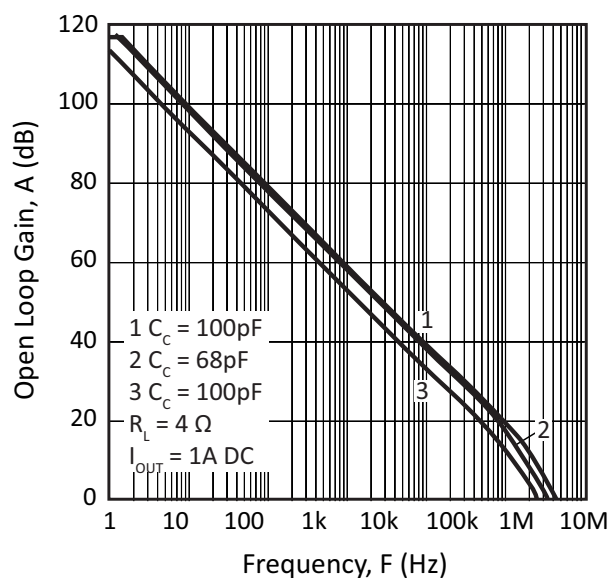


Figure 9: Phase Response w/o Boost

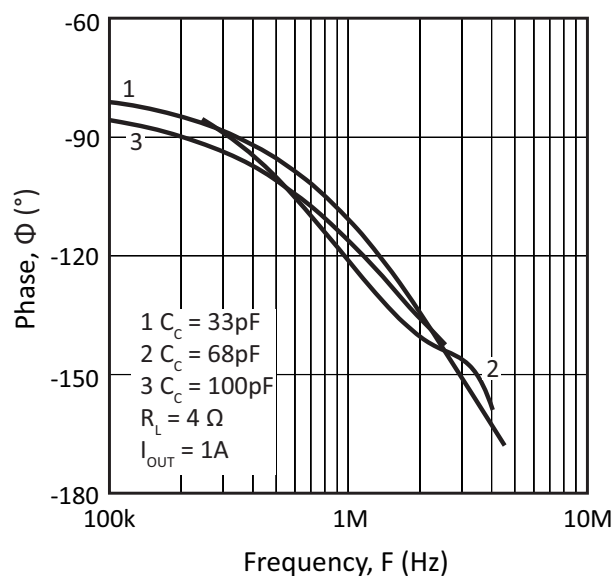


Figure 10: Current Limit

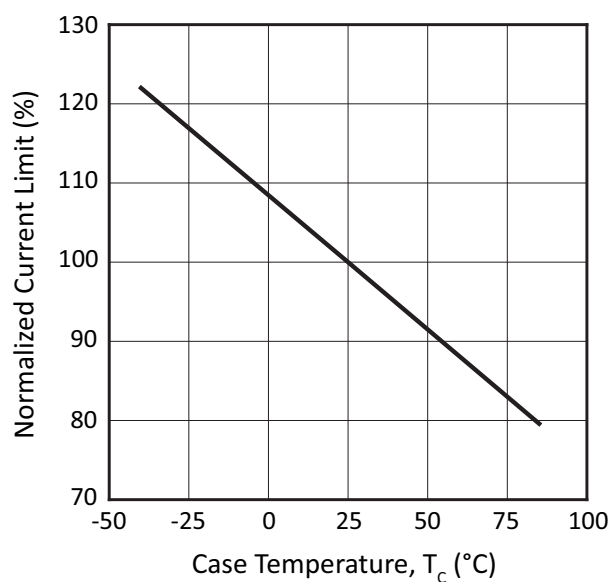


Figure 11: Quiescent Current vs. Supply

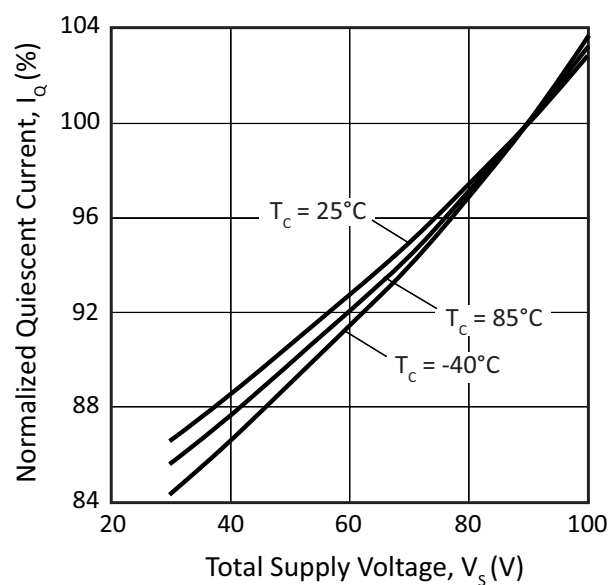


Figure 12: Quiescent Current vs. Temperature

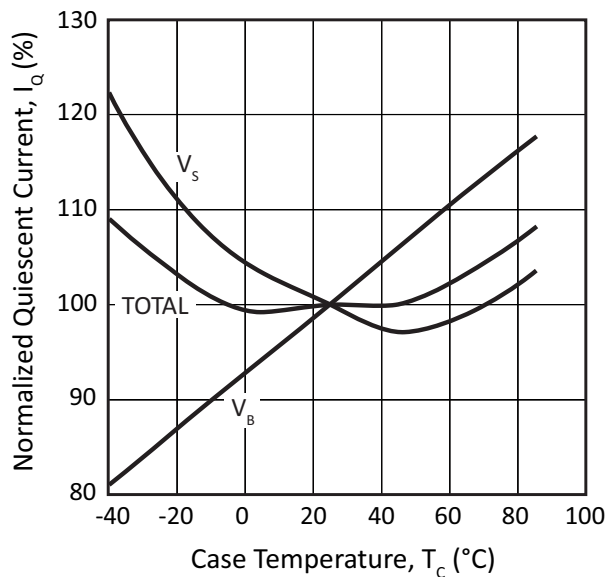


Figure 13: Harmonic Distortion

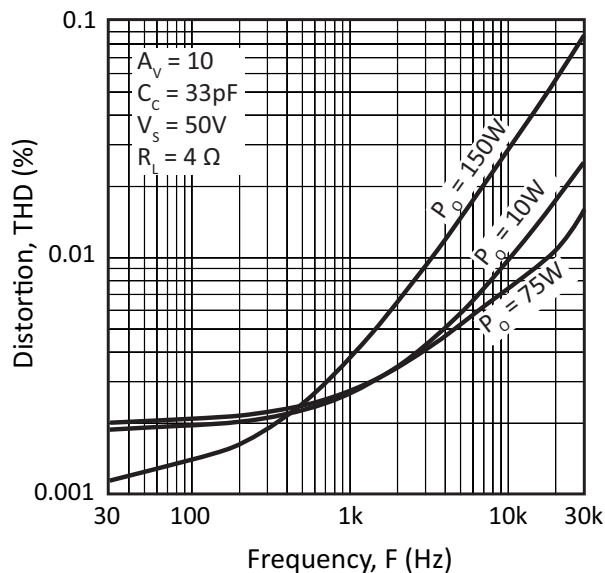
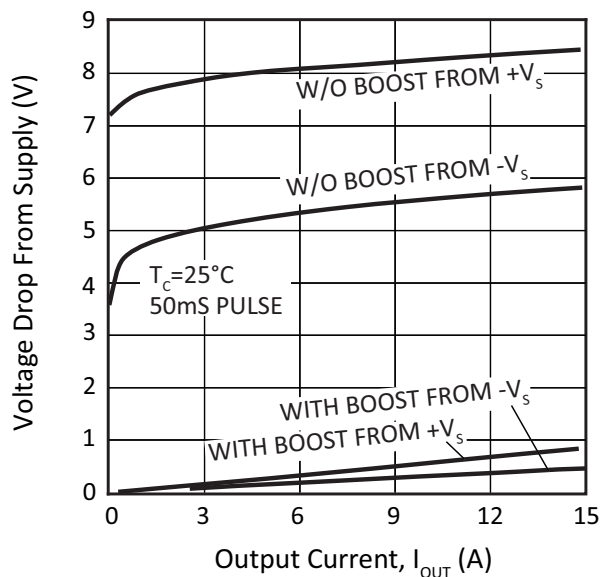


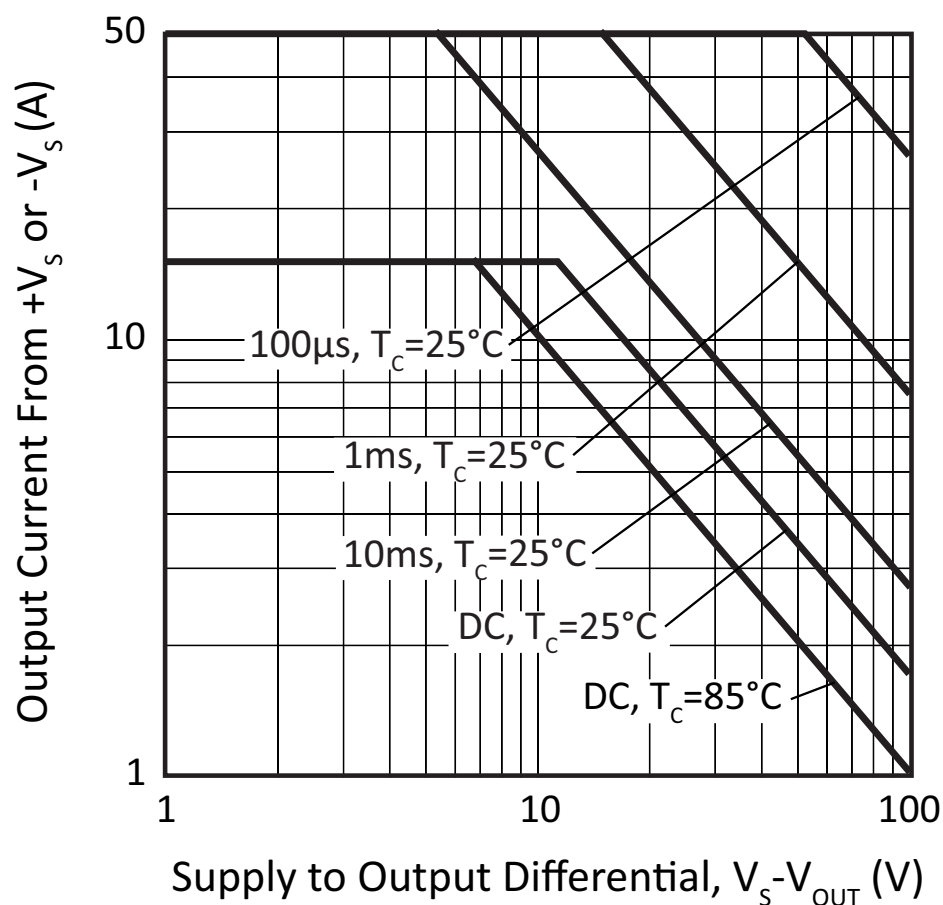
Figure 14: Output Voltage Swing



SAFE OPERATING AREA (SOA)

The MOSFET output stage of the MP111 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast reverse recovery diodes must be used.

Figure 15: SOA



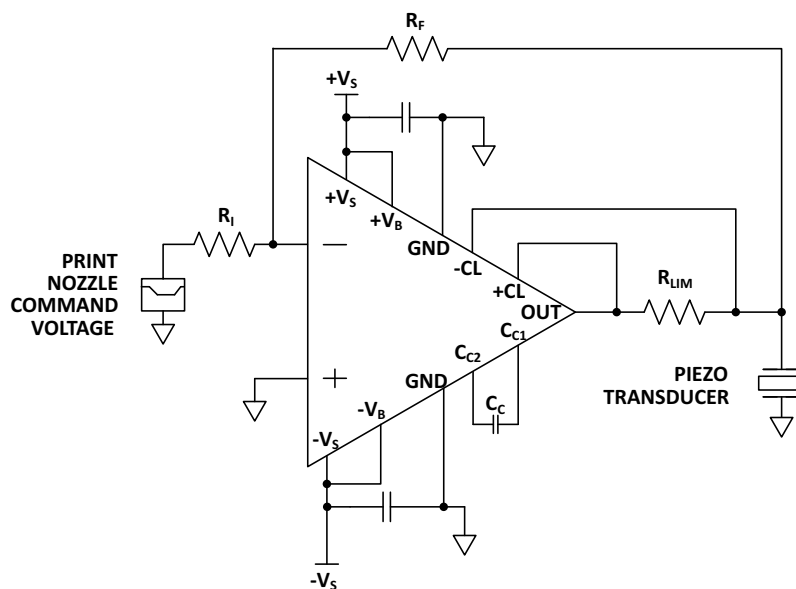
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

The MP111's fast slew rate and wide power bandwidth make it an ideal nozzle driver for industrial inkjet printers. The 50A pulse output capability can drive hundreds of inkjet nozzles simultaneously.

Figure 16: Typical Application



GROUND PINS

The MP111 has two ground pins (pins 3, 32). These pins provide a return for the internal capacitive bypassing of the small signal portions of the MP111. The two ground pins are not connected together on the substrate. Both of these pins are required to be connected to the system signal ground.

PHASE COMPENSATION

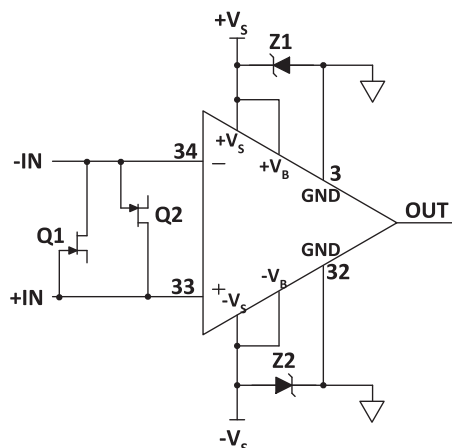
The external compensation capacitor C_C is connected between pins 5 and 6. Unity gain stability can be achieved with any capacitor value larger than 100pF for a minimum phase margin of 45 degrees. At higher gains more phase shift can usually be tolerated in most designs and the compensation capacitor value can be reduced resulting in higher bandwidth and slew rate. Use the typical operating curves and table in this section as a guide to select C_C for the application. An NPO (COG) type capacitor is required rated for the full supply voltage (100V).

Gain w/o boost	C_C	Typ. Slew Rate
≥ 1	100 pF	55 V/ μ s
≥ 4	60 pF	60 V/ μ s
≥ 10	33 pF	130 V/ μ s
Gain with boost	C_C	Typ. Slew Rate
≥ 3	470 pF	12 V/ μ s
≥ 6	220 pF	27 V/ μ s
≥ 10	100 pF	55 V/ μ s

OVERVOLTAGE PROTECTION

Although the MP111 can withstand differential input voltages up to $\pm 25V$, additional external protection is recommended. In most applications 1N4148 signal diodes connected anti-parallel across the input pins is sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 17. In either case the differential input voltage will be clamped to $\pm 0.7V$. This is usually sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over voltage protection devices connected to the power supply rails. Unidirectional transient voltage suppressor diodes or zener diodes are recommended. These diodes clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether TVS or zener diodes are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 17.

Figure 17: Overvoltage Protection



POWER SUPPLY BYPASSING

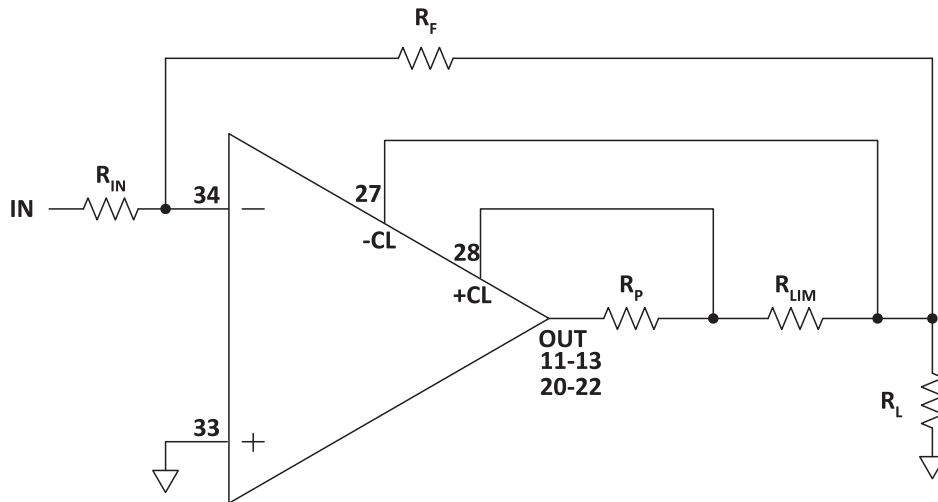
Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP111. Use electrolytic capacitors at least $10\mu\text{F}$ per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) $0.1\mu\text{F}$ or greater. In most applications power supply terminals $+V_B$ and $-V_B$ will be connected to $+V_S$ and $-V_S$ respectively. Supply voltages $+V_B$ and $-V_B$ are bypassed internally but both ground pins 3 and 32 must be connected to the system signal ground to be effective. In all cases power to the buffer amplifier stage of the MP111 at pins 8 and 25 must be connected to $+V_B$ and $-V_B$ at pins 4 and 30 respectively. Provide local bypass capacitors at pins 8 and 25. See Figure 2 for Typical Connection Diagram.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 28 must be connected to the amplifier output side and pin 27 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 18. This connection will bypass any parasitic resistances R_p , formed by socket and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 18. The value of the current limit resistor can be calculated as follows:

$$R_{LIM} = \frac{0.65V}{I_{LIM}}$$

Figure 18: 4-Wire Current Limit



BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at a higher supply voltages than the amplifier's high current output stage. $+V_B$ (pins 4,8) and $-V_B$ (pins 25,30) are connected to the small signal stages and $+V_S$ (pins 14-16) and $-V_S$ (pins 17-19) are connected to the high current output stage. An additional 10V on the $+V_B$ and $-V_B$ pins is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed $+V_S$ and $-V_S$ are connected to the $+V_B$ and $-V_B$ pins respectively. The $+V_B$ and $-V_B$ pins must not be operated at supply voltages less than $+V_S - 0.6\text{ V}$ and $-V_S + 0.6\text{ V}$ respectively.

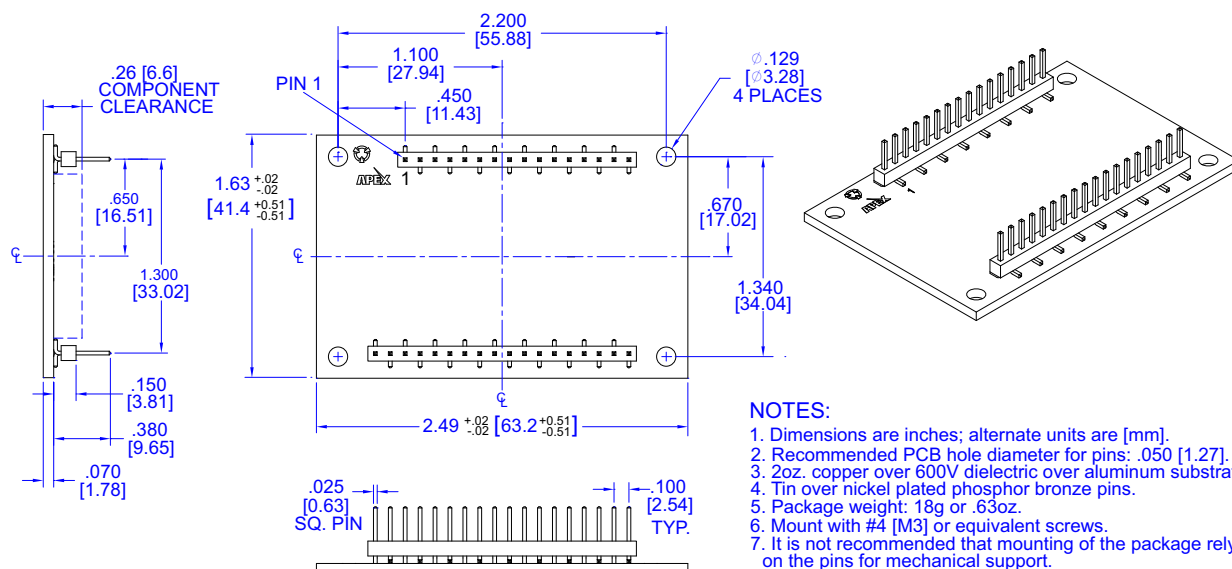
BACKPLATE GROUNDING

The substrate of the MP111 is an insulated metal substrate. It is required that it be connected to signal ground. Connect pin 2 (back plate) to signal ground. The back plate will then be AC grounded to signal ground through a $1\mu\text{F}$ capacitor.

PACKAGE OPTIONS

Part Number	Apex Package Style	Description
MP108	FD	34-pin Open Frame
MP108A	FD	34-pin Open Frame

PACKAGE STYLE FD



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