

# **MP04TT600**

# **Dual Thyristor Water Cooled Module**

**Preliminary Information** 

DS5466-1.1 June 2001

#### **FEATURES**

- Dual Device Module
- Electrically Isolated Package
- Pressure Contact Construction
- International Standard Footprint
- Alumina (Non Toxic) Isolation Medium
- Integral Water Cooled Heatsink

### **APPLICATIONS**

- Motor Control
- Controlled Rectifier Bridges
- Heater Control
- AC Phase Control

### **VOLTAGE RATINGS**

	Type Number	Repetitive Peak Voltages V <sub>DRM</sub> V <sub>RRM</sub> V	Conditions
W\	MP04TT600-18 MP04TT600-17m MP04TT600-16 MP04TT600-15	1800 1700 1600 1500	$\begin{split} & T_{\rm vj} = 0^{\circ} \text{ to } 125^{\circ}\text{C}, \\ & I_{\rm DRM} = I_{\rm RRM} = 50\text{mA} \\ & V_{\rm DSM} = V_{\rm RSM} = \\ & V_{\rm DRM} = V_{\rm RRM} + 100V \\ & \text{respectively} \end{split}$

Lower voltage grades available

### **ORDERING INFORMATION**

Order As:

W١

MP04TT600-XX-W2 1/4 - 18 NPT connection
MP04TT600-XX-W3 1/4 - 18 NPT connection
MP04TT600-XX-W3A 1/4 - 18 NPT water connection
thread

XX shown in the part number about represents  $V_{\text{DRM}}/100$  selection required, eg. MP04TT600-27-W2

Note: When ordering, please use the complete part number.

### **KEY PARAMETERS**

 $\begin{array}{ccc} {\rm V_{DRM}} & & 1800{\rm V} \\ {\rm I_{T(AV)}} & & 580{\rm A} \\ {\rm I_{TSM(per\,arm)}} & & 14000{\rm A} \\ {\rm I_{T(RMS)}} & & 912{\rm A} \\ {\rm V_{isol}} & & 3000{\rm V} \\ \end{array}$ 

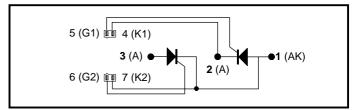


Fig. 1 TT Circuit diagram

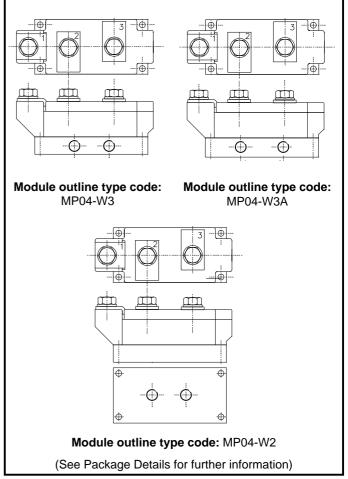


Fig. 2 Module package variants - (not to scale)



# **ABSOLUTE MAXIMUM RATINGS - PER ARM**

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed. Exposure to Absolute Maximum Ratings may affect device reliability.

Symbol	Parameter	Test Conditions		Max.	Units
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load,	T <sub>water (in)</sub> = 25°C	650	Α
		4.5 Ltr/min	T <sub>water (in)</sub> = 40°C	580	Α
I <sub>T(RMS</sub>	RMS value	T <sub>water (in)</sub> = 25°C @ 4.5 Ltr/min		1020	Α
		T <sub>water (in)</sub> = 40°C @ 4.5 Ltr/min		912	Α
I <sub>TSM</sub>	Surge (non-repetitive) on-current	10ms half sine, T <sub>j</sub> = 125°C		14	kA
l²t	I <sup>2</sup> t for fusing	$V_R = 0$		0.975x10 <sup>6</sup>	A <sup>2</sup> s
I <sub>TSM</sub>	Surge (non-repetitive) on-current	10ms half sine, T <sub>j</sub> = 125°C		11.2	kA
l²t	I <sup>2</sup> t for fusing	$V_R = 50\% V_{DRM}$		0.625x10 <sup>6</sup>	A <sup>2</sup> s
$V_{\rm isol}$	Isolation voltage	Commoned terminals to base plate. AC RMS, 1 min, 50Hz		3000	V

# THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
www.DataShee R <sub>th(j-w)</sub>	Thermal resistance - junction to water	dc, 4.5 Ltr/min	-	0.102	°C/kW
	(per thyristor)	Half wave, 4.5 Ltr/min	-	0.106	°C/kW
		3 Phase, 4.5 Ltr/min	-	0.112	°C/kW
$T_{v_{j}}$	Virtual junction temperature	Reverse (blocking)	-	125	°C
T <sub>stg</sub>	Storage temperature range	-	-40	125	°C
-	Screw torque	Mounting - M6	6(53)	-	Nm (lb.ins)
		Electrical connections - M10	-	12(106)	Nm (lb.ins)
-	Weight (nominal)	-	-	Refer to drawings	g



# **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_j = 125^{\circ}C$	-	50	mA
dV/dt	Linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C	-	1000	V/µs
dl/dt	Rate of rise of on-state current	From 67% $V_{DRM}$ to 500A, gate source 10V, $5\Omega$	-	500	A/μs
		t <sub>r</sub> = 0.5μs, T <sub>j</sub> = 125°C			
V <sub>T(TO)</sub>	Threshold voltage	At T <sub>vj</sub> = 125°C	-	0.85	V
r <sub>T</sub>	On-state slope resistance	At T <sub>vj</sub> = 125°C	-	0.38	mΩ

**Note:** The data given in this datasheet with regard to forward voltage drop is for calculation of the power dissipation in the semiconductor elements only. Forward voltage drops measured at the power terminals of the module will be in excess of these figures due to the impedance of the busbar from the terminal to the semiconductor.

## **GATE TRIGGER CHARACTERISTICS AND RATINGS**

	Symbol	Parameter	Test Conditions	Max.	Units
	V <sub>GT</sub>	Gate trigger voltage	$V_{DRM} = 5V$ , $T_{case} = 25^{\circ}C$	3.5	V
	I <sub>GT</sub>	Gate trigger current	$V_{DRM} = 5V$ , $T_{case} = 25^{\circ}C$	200	mA
	$V_{\scriptscriptstyle{GD}}$	Gate non-trigger voltage	At V <sub>DRM</sub> T <sub>case</sub> = 125°C	0.25	٧
	$V_{FGM}$	Peak forward gate voltage	Anode positive with respect to cathode	30	٧
WWV	V /.Data\$¶⊌et4U	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
	$V_{RGM}$	Peak reverse gate voltage	-	5	V
	I <sub>FGM</sub>	Peak forward gate current	Anode positive with respect to cathode	10	А
	$P_{GM}$	Peak gate power	See table fig. 5	150	W
	$P_{G(AV)}$	Mean gate power	-	10	W



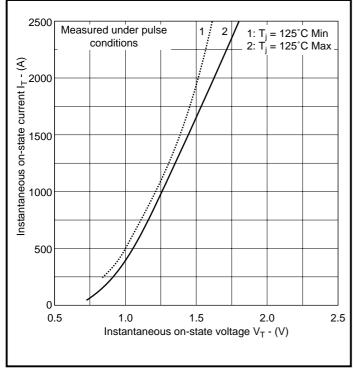
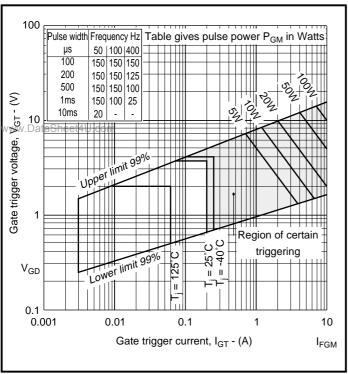


Fig. 3 Maximum (limit) on-state characteristics

Fig. 4 Surge (non-repetitive) on-state current vs time (with 50%  $V_{RSM}$  at  $T_{case}$  = 125°C)





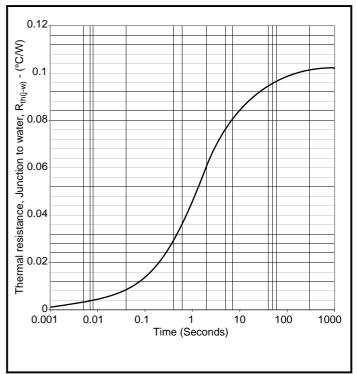


Fig. 6 Transient thermal impedance - dc



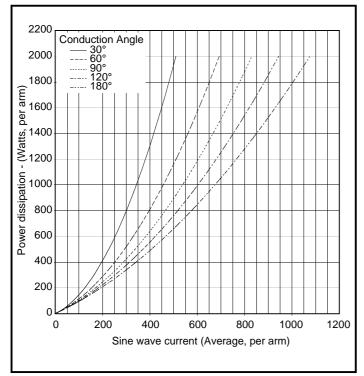


Fig. 7 On-state power loss per arm vs on-state current at specified conduction angles, sine wave 50/60Hz

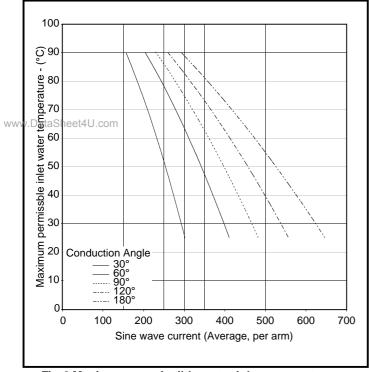


Fig. 9 Maximum permissible water inlet temperature vs on-state current at specified conduction angles, sine wave 50/60Hz

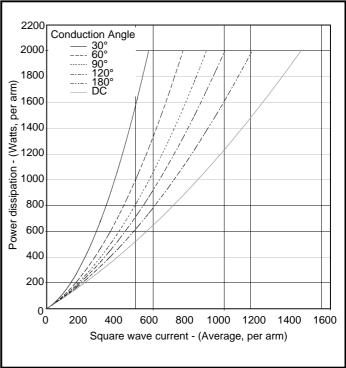


Fig. 8 On-state power loss per arm vs on-state current at specified conduction angles, square wave 50/60Hz

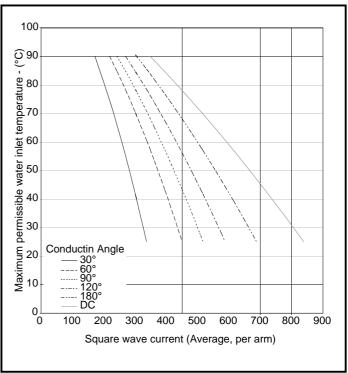
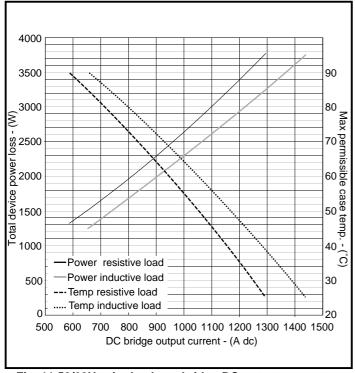
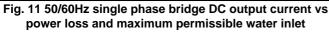


Fig. 10 Maximum permissible water inlet temperature vs on-state current at specified conduction angles, square wave 50/60Hz







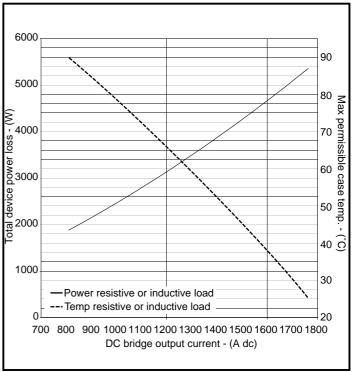


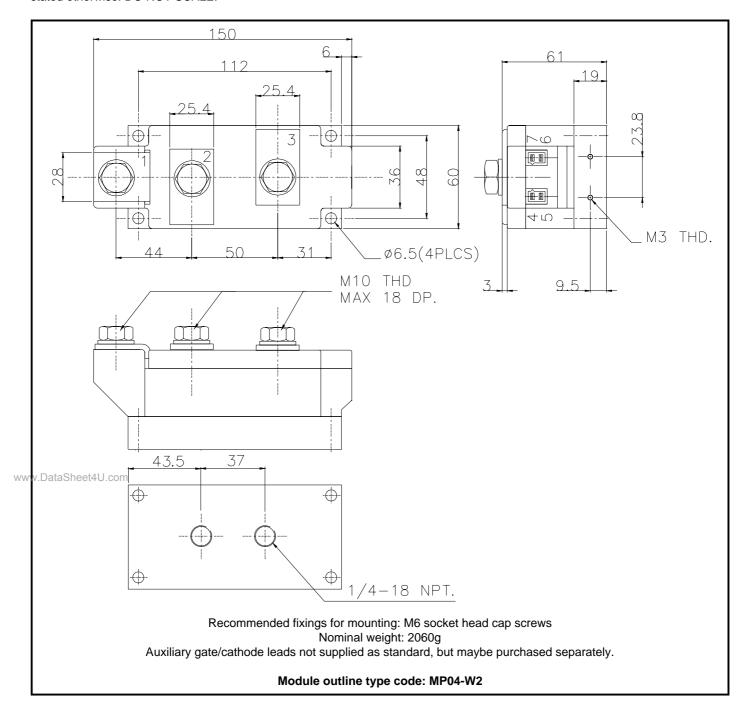
Fig. 12 Fig. 11 50/60Hz Three phase bridge DC output current vs power loss and maximum permissible water inlet

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## **PACKAGE DETAILS**

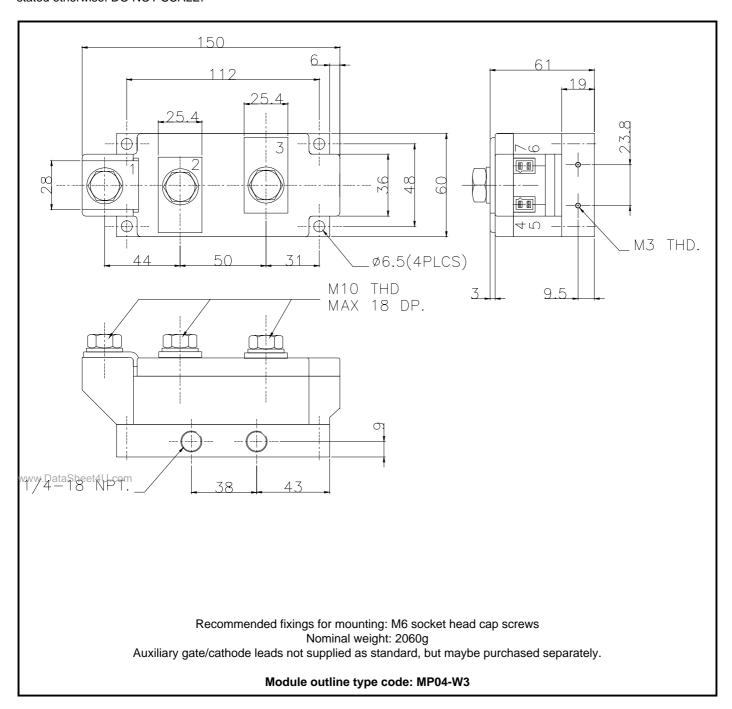
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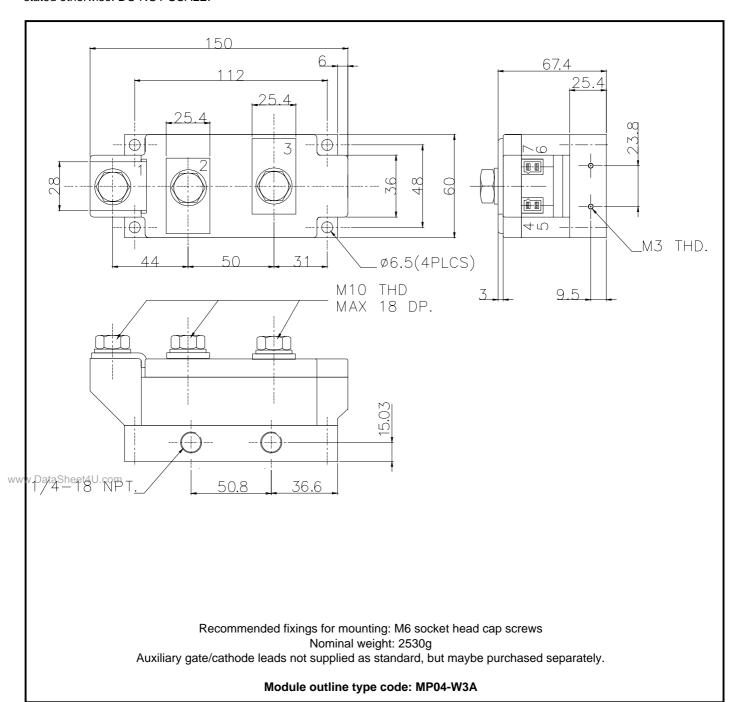
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The Power Assembly group provides support for those customers requiring more than the basic semiconductor switch. Using CAD design tools the group has developed a flexible range of heatsink / clamping systems in line with advances in device types and the voltage and current capability of Dynex semiconductors.

An extensive range of air and liquid cooled assemblies is available covering the range of circuit designs in general use today.

#### **HEATSINKS**

The Power Assembly group has a proprietary range of extruded aluminium heatsinks. These were designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or customer service office.



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