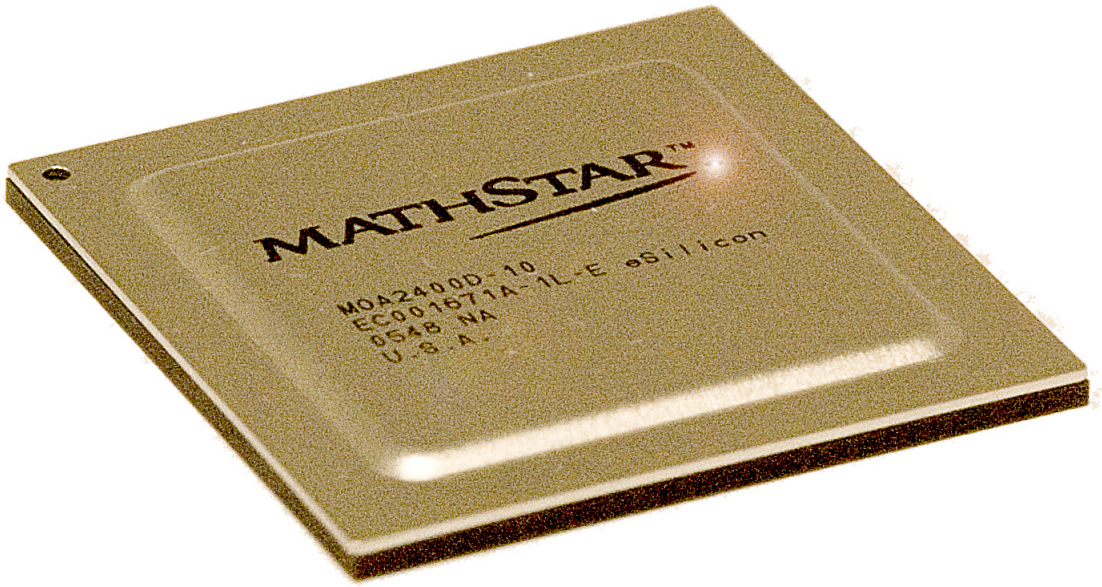
MATHSTAR™

The FPOA™ Leader

Field Programmable Object Array™

Arrix™ Family



Product Data Sheet

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About this Document

The Arrix™ Family Data Sheet consists of a detailed definition of the hardware development environment. The topics covered include the following:

- Pin Definitions
- AC/DC Electrical Characteristics
- Power and Clock Requirements
- Thermal Environment
- Package Information
- Design Caveats

Intended Audience

This document is intended for hardware designers already familiar with FPOA™ concepts. Refer to the Architecture Guide for further information about the FPOA. Detailed descriptions about each object can be found in the Arrix Family Application Developer's Object Reference.

Related Documents

The following documents provide additional information about the FPOA:

Table 0-1 Related Documents

Document	Description
Arrix Family FPOA Architecture Guide	This document describes the structural and communication architecture of the FPOA.
Arrix Family Application Developer's Object Reference	This document provides detailed information about each object in the Arrix family FPOA, including inputs, outputs, configuration parameters, and timing details.
Application Developer's Guide	This document uses an example application to guide you through creating an FPOA design, connecting and assigning the design, and debugging the design. It includes sample screens, typical circuits, and basic procedures based on the MathStar Design Software.

Chapter 1
Introduction

General Description

MathStar™'s Field Programmable Object Array™ (FPOA™) is a breakthrough field-programmable silicon platform that supports high-speed designs. Unlike FPGAs, which implement functions at the gate level, FPOAs employ higher-order building blocks called "objects." These objects provide a much higher level of abstraction than the gates of conventional FPGAs and perform complex operations at very high clock rates.

Each Arrix™ family FPOA contains over 400 objects that are able to pass data and signals to each other through a patented, configurable communication framework. The timing of both the objects and the communication framework is fixed, operating deterministically at frequencies of up to 1 GHz. This deterministic performance eliminates the tedious timing closure design steps associated with previous silicon solutions such as FPGAs and ASICs. MathStar's FPOA allows high-level functions, algorithms, equations, and block diagrams to be quickly, directly, and efficiently realized in high-performance silicon.

The Arrix product family is comprised of six products as shown in Table 1-1.

Table 1-1 Arrix Product Family

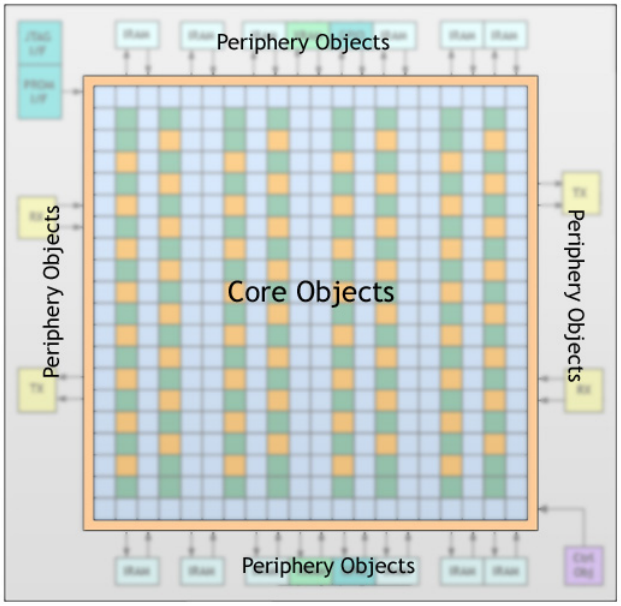
Product	Package Information	Maximum Operating Frequency
MOA2400D-10	HFCBGA-896	1 GHz
MOA2400D-08	HFCBGA-896	800 MHz
MOA2400D-04	HFCBGA-896	400 MHz
MOA2400D-10 R	HFCBGA-896, RoHS Compliant[a]	1 GHz
MOA2400D-08 R	HFCBGA-896, RoHS Compliant[a]	800 MHz
MOA2400D-04 R	HFCBGA-896, RoHS Compliant[a]	400 MHz

a. RoHS (Restriction on Hazardous Substances) compliance requires limited levels of lead (Pb), mercury, cadmium, hexavalent chromium, polybrominated biphenyl (PBB), and polybrominated diphenyl ethers (PBDE). These levels must be below thresholds proposed by the EU.

FPOA Architecture

The objects of the FPOA reside in two areas: the core and the periphery. The core objects do most of the computation while the periphery objects provide additional RAM as well as move data between core objects and external devices. Figure 1-1 illustrates these two areas.

Figure 1-1 FPOA Core and Periphery



The core objects are controlled by the FPOA application and are not discussed in this document. However, the electrical characteristics of the following periphery objects are discussed:

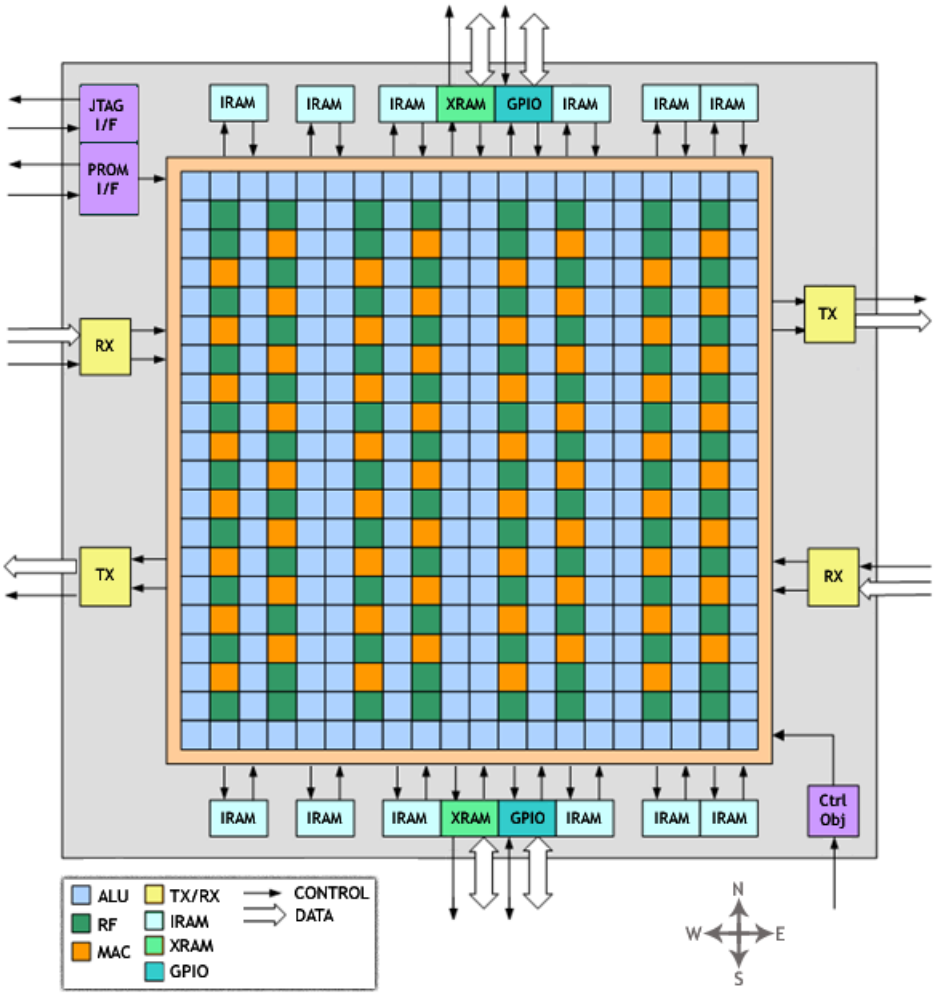
- External RAM (XRAM) — Each XRAM object provides access to 16 meg by 72-bit (4*16 data bits + 4*2 tag bits) RLDRAM-II. Each Arrix product provides two XRAM objects in the periphery.
- General Purpose I/O (GPIO) — The GPIO object provides 48 bidirectional pins of I/O, allowing data transfer between the FPOA and external devices. Each Arrix product provides two GPIO objects in the periphery.
- Receive (RX) Interface — The RX interface is used for parallel LVDS input to the FPOA. Each interface has a 17-bit input (16 data bits + 1 tag bit). Each Arrix product provides two RX interfaces in the periphery.

- Transmit (TX) Interface — The TX interface is used for parallel LVDS output from the FPOA. Each interface has a 17-bit output (16 data bits + 1 tag bit). Each Arrix product provides two TX interfaces in the periphery.

- Initialization and Control components — This includes a PROM and JTAG controller, as well as pins for providing an external reference clock.

Figure 1-2 illustrates the Arrix family FPOA with all objects labeled.

Figure 1-2 FPOA Objects



For more information on the architecture, see the Arrix Family FPOA Architecture Guide. For more information on the internal characteristics of the FPOA objects, see the Application Developer's Object Reference.

Chapter 2
XRAM Hardware

Overview

Each Arrix product provides two external RAM (XRAM) controllers, one on the north side of the periphery and one on the south side. Each XRAM controller provides access to external 36-bit Double-Data-Rate (DDR) Reduced Latency DRAM (RLDRAM-II) memory.

The XRAM controller on the north side is associated with the XRAM1_* pins while the controller on the south side is associated with the XRAM2_* pins. Each controller has 21 pins associated with the address bits, 3 pins associated with bank selection, 2 clock pins, 3 control pins, 36 data pins, 8 pins associated with the data output clock, 8 pins associated with the data input strobe, and 21 pins associated with power and termination (20 pins for XRAM2).

Table 2-1 XRAM General Characteristics

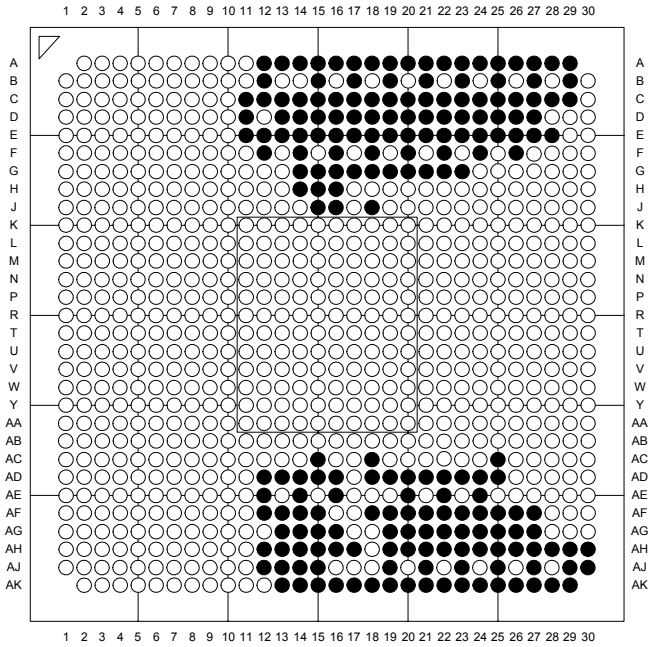
Characteristic	Description
Supported Frequency	175 MHz – 266 MHz[a] See Chapter 8: Clock Characteristics for more information.
Signal Information	❋ 1.8 volts (HSTL) ❋ Single-ended 50 Ω impedance (including clock pairs)
RLDRAM Configurations	❋ One 36-bit RLDRAM for 36 MBytes of memory ❋ Two 18-bit RLDRAM for 72 MBytes of memory ❋ Four 9-bit RLDRAM for 144 MBytes of memory See "RLDRAM Details" on page 31 for more information.

a. The 175 MHz minimum frequency is a Micron requirement for the RLDRAMII device.

External Pins

Table 2-2 describes the pins associated with the XRAM controller. For a list of all pins associated with the Arrix family FPOA, see Appendix A: External Pins.

Figure 2-1 Ball Pattern for XRAM (Top-down View)



NOTE: XRAM-related balls are shown in black.

Table 2-2 XRAM Pin Descriptions

Pin Number	Signal	Type	Signal Type	Notes
XRAM 1				
A24	XRAM1_ADDR_0	O	HSTL	XRAM Address bit (LSB)
B25	XRAM1_ADDR_1	O	HSTL	XRAM Address bit
A25	XRAM1_ADDR_2	O	HSTL	XRAM Address bit
F24	XRAM1_ADDR_3	O	HSTL	XRAM Address bit
E24	XRAM1_ADDR_4	O	HSTL	XRAM Address bit
E23	XRAM1_ADDR_5	O	HSTL	XRAM Address bit
A26	XRAM1_ADDR_6	O	HSTL	XRAM Address bit
D25	XRAM1_ADDR_7	O	HSTL	XRAM Address bit
B27	XRAM1_ADDR_8	O	HSTL	XRAM Address bit

Table 2-2 XRAM Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
A27	XRAM1_ADDR_9	O	HSTL	XRAM Address bit
C26	XRAM1_ADDR_10	O	HSTL	XRAM Address bit
D26	XRAM1_ADDR_11	O	HSTL	XRAM Address bit
A28	XRAM1_ADDR_12	O	HSTL	XRAM Address bit
D27	XRAM1_ADDR_13	O	HSTL	XRAM Address bit
E26	XRAM1_ADDR_14	O	HSTL	XRAM Address bit
F26	XRAM1_ADDR_15	O	HSTL	XRAM Address bit
E25	XRAM1_ADDR_16	O	HSTL	XRAM Address bit
E27	XRAM1_ADDR_17	O	HSTL	XRAM Address bit
C28	XRAM1_ADDR_18	O	HSTL	XRAM Address bit
B29	XRAM1_ADDR_19	O	HSTL	XRAM Address bit
A29	XRAM1_ADDR_20	O	HSTL	XRAM Address bit (MSB)
G21	XRAM1_BANK_0	O	HSTL	XRAM Bank bit
F22	XRAM1_BANK_1	O	HSTL	XRAM Bank bit
E22	XRAM1_BANK_2	O	HSTL	XRAM Bank bit
C24	XRAM1_CLK_N	O	HSTL	XRAM Differential output command clock
D24	XRAM1_CLK_P	O	HSTL	XRAM Command clock
A23	XRAM1_CNTL_0	O	HSTL	XRAM Control bit (REF#)
D23	XRAM1_CNTL_1	O	HSTL	XRAM Control bit (WE#)
B23	XRAM1_CNTL_2	O	HSTL	XRAM Control bit (CS#)
A14	XRAM1_DATA_0	I/O	HSTL	XRAM Data bit (LSB)
F14	XRAM1_DATA_1	I/O	HSTL	XRAM Data bit
E14	XRAM1_DATA_2	I/O	HSTL	XRAM Data bit
D14	XRAM1_DATA_3	I/O	HSTL	XRAM Data bit
C14	XRAM1_DATA_4	I/O	HSTL	XRAM Data bit
A15	XRAM1_DATA_5	I/O	HSTL	XRAM Data bit
H14	XRAM1_DATA_6	I/O	HSTL	XRAM Data bit
G15	XRAM1_DATA_7	I/O	HSTL	XRAM Data bit
H15	XRAM1_DATA_8	I/O	HSTL	XRAM Data bit
F16	XRAM1_DATA_9	I/O	HSTL	XRAM Data bit
E16	XRAM1_DATA_10	I/O	HSTL	XRAM Data bit

Table 2-2 XRAM Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
A16	XRAM1_DATA_11	I/O	HSTL	XRAM Data bit
B17	XRAM1_DATA_12	I/O	HSTL	XRAM Data bit
A17	XRAM1_DATA_13	I/O	HSTL	XRAM Data bit
G17	XRAM1_DATA_14	I/O	HSTL	XRAM Data bit
E17	XRAM1_DATA_15	I/O	HSTL	XRAM Data bit
D17	XRAM1_DATA_16	I/O	HSTL	XRAM Data bit
H16	XRAM1_DATA_17	I/O	HSTL	XRAM Data bit
C18	XRAM1_DATA_18	I/O	HSTL	XRAM Data bit
A18	XRAM1_DATA_19	I/O	HSTL	XRAM Data bit
A19	XRAM1_DATA_20	I/O	HSTL	XRAM Data bit
F18	XRAM1_DATA_21	I/O	HSTL	XRAM Data bit
E18	XRAM1_DATA_22	I/O	HSTL	XRAM Data bit
D18	XRAM1_DATA_23	I/O	HSTL	XRAM Data bit
A20	XRAM1_DATA_24	I/O	HSTL	XRAM Data bit
B19	XRAM1_DATA_25	I/O	HSTL	XRAM Data bit
G19	XRAM1_DATA_26	I/O	HSTL	XRAM Data bit
A21	XRAM1_DATA_27	I/O	HSTL	XRAM Data bit
A22	XRAM1_DATA_28	I/O	HSTL	XRAM Data bit
F20	XRAM1_DATA_29	I/O	HSTL	XRAM Data bit
E20	XRAM1_DATA_30	I/O	HSTL	XRAM Data bit
B21	XRAM1_DATA_31	I/O	HSTL	XRAM Data bit
E21	XRAM1_DATA_32	I/O	HSTL	XRAM Data bit
D21	XRAM1_DATA_33	I/O	HSTL	XRAM Data bit
D22	XRAM1_DATA_34	I/O	HSTL	XRAM Data bit
C22	XRAM1_DATA_35	I/O	HSTL	XRAM Data bit (MSB)
E15	XRAM1_DVLD	I	HSTL	XRAM Data Valid Input This pin should come from the RLDRAM devices associated with XRAM_DATA[8:0].
B15	XRAM1_DK0_N	O	HSTL	XRAM Differential Output clock (bits 0-8)
C15	XRAM1_DK0_P	O	HSTL	XRAM Differential Output clock (bits 0-8)
C16	XRAM1_DK1_N	O	HSTL	XRAM Differential Output clock (bits 9-17)
D16	XRAM1_DK1_P	O	HSTL	XRAM Differential Output clock (bits 9-17)

Table 2-2 XRAM Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
D20	XRAM1_DK2_N	O	HSTL	XRAM Differential Output clock (bits 18-26)
C20	XRAM1_DK2_P	O	HSTL	XRAM Differential Output clock (bits 18-26)
D19	XRAM1_DK3_N	O	HSTL	XRAM Differential Output clock (bits 27-35)
E19	XRAM1_DK3_P	O	HSTL	XRAM Differential Output clock (bits 27-35)
D11	XRAM1_DQS0_N	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
C11	XRAM1_DQS0_P	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
F12	XRAM1_DQS1_N	I	HSTL	XRAM Differential Input strobe (bits 9-17)
E12	XRAM1_DQS1_P	I	HSTL	XRAM Differential Input strobe (bits 9-17)
B12	XRAM1_DQS2_N	I	HSTL	XRAM Differential Input strobe (bits 18-26)
A12	XRAM1_DQS2_P	I	HSTL	XRAM Differential Input strobe (bits 18-26)
D13	XRAM1_DQS3_N	I	HSTL	XRAM Differential Input strobe (bits 27-35)
C13	XRAM1_DQS3_P	I	HSTL	XRAM Differential Input strobe (bits 27-35)
A13	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C12	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C17	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C19	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C21	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C23	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C25	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C27	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C29	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
D15	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
E11	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
E13	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
E28	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G14	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G16	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G18	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G20	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G22	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)

Table 2-2 XRAM Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
G23	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
J15	XRAM1_VREF1	I	Analog	Connect to XRAM reference voltage (0.9V)
J16	XRAM1_VREF2	I	Analog	Connect to XRAM reference voltage (0.9V)
J18	XRAM1_VREF3	I	Analog	Connect to XRAM reference voltage (0.9V)
XRAM 2				
AF23	XRAM2_ADDR_0	O	HSTL	XRAM Address bit (LSB)
AG24	XRAM2_ADDR_1	O	HSTL	XRAM Address bit
AH24	XRAM2_ADDR_2	O	HSTL	XRAM Address bit
AE24	XRAM2_ADDR_3	O	HSTL	XRAM Address bit
AD23	XRAM2_ADDR_4	O	HSTL	XRAM Address bit
AF24	XRAM2_ADDR_5	O	HSTL	XRAM Address bit
AF25	XRAM2_ADDR_6	O	HSTL	XRAM Address bit
AG25	XRAM2_ADDR_7	O	HSTL	XRAM Address bit
AJ27	XRAM2_ADDR_8	O	HSTL	XRAM Address bit
AK27	XRAM2_ADDR_9	O	HSTL	XRAM Address bit
AC25	XRAM2_ADDR_10	O	HSTL	XRAM Address bit
AD25	XRAM2_ADDR_11	O	HSTL	XRAM Address bit
AF26	XRAM2_ADDR_12	O	HSTL	XRAM Address bit
AH28	XRAM2_ADDR_13	O	HSTL	XRAM Address bit
AJ29	XRAM2_ADDR_14	O	HSTL	XRAM Address bit
AK28	XRAM2_ADDR_15	O	HSTL	XRAM Address bit
AH30	XRAM2_ADDR_16	O	HSTL	XRAM Address bit
AJ30	XRAM2_ADDR_17	O	HSTL	XRAM Address bit
AK29	XRAM2_ADDR_18	O	HSTL	XRAM Address bit
AF27	XRAM2_ADDR_19	O	HSTL	XRAM Address bit
AG27	XRAM2_ADDR_20	O	HSTL	XRAM Address bit (MSB)
AK26	XRAM2_BANK_0	O	HSTL	XRAM Bank bit
AJ25	XRAM2_BANK_1	O	HSTL	XRAM Bank bit
AK25	XRAM2_BANK_2	O	HSTL	XRAM Bank bit
AG26	XRAM2_CLK_N	O	HSTL	XRAM Differential output command clock
AH26	XRAM2_CLK_P	O	HSTL	XRAM Command clock

Table 2-2 XRAM Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AK24	XRAM2_CNTL_0	O	HSTL	XRAM Control bit (REF#)
AJ23	XRAM2_CNTL_1	O	HSTL	XRAM Control bit (WE#)
AK23	XRAM2_CNTL_2	O	HSTL	XRAM Control bit (CS#)
AF14	XRAM2_DATA_0	I/O	HSTL	XRAM Data bit (LSB)
AG14	XRAM2_DATA_1	I/O	HSTL	XRAM Data bit
AJ14	XRAM2_DATA_2	I/O	HSTL	XRAM Data bit
AH14	XRAM2_DATA_3	I/O	HSTL	XRAM Data bit
AK15	XRAM2_DATA_4	I/O	HSTL	XRAM Data bit
AK14	XRAM2_DATA_5	I/O	HSTL	XRAM Data bit
AE14	XRAM2_DATA_6	I/O	HSTL	XRAM Data bit
AF15	XRAM2_DATA_7	I/O	HSTL	XRAM Data bit
AJ15	XRAM2_DATA_8	I/O	HSTL	XRAM Data bit
AD15	XRAM2_DATA_9	I/O	HSTL	XRAM Data bit
AJ17	XRAM2_DATA_10	I/O	HSTL	XRAM Data bit
AK19	XRAM2_DATA_11	I/O	HSTL	XRAM Data bit
AK18	XRAM2_DATA_12	I/O	HSTL	XRAM Data bit
AE16	XRAM2_DATA_13	I/O	HSTL	XRAM Data bit
AF16	XRAM2_DATA_14	I/O	HSTL	XRAM Data bit
AG17	XRAM2_DATA_15	I/O	HSTL	XRAM Data bit
AD17	XRAM2_DATA_16	I/O	HSTL	XRAM Data bit
AF17	XRAM2_DATA_17	I/O	HSTL	XRAM Data bit
AH18	XRAM2_DATA_18	I/O	HSTL	XRAM Data bit
AG18	XRAM2_DATA_19	I/O	HSTL	XRAM Data bit
AE18	XRAM2_DATA_20	I/O	HSTL	XRAM Data bit
AF18	XRAM2_DATA_21	I/O	HSTL	XRAM Data bit
AF19	XRAM2_DATA_22	I/O	HSTL	XRAM Data bit
AG19	XRAM2_DATA_23	I/O	HSTL	XRAM Data bit
AJ19	XRAM2_DATA_24	I/O	HSTL	XRAM Data bit
AK20	XRAM2_DATA_25	I/O	HSTL	XRAM Data bit
AJ21	XRAM2_DATA_26	I/O	HSTL	XRAM Data bit
AK21	XRAM2_DATA_27	I/O	HSTL	XRAM Data bit

Table 2-2 XRAM Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AF21	XRAM2_DATA_28	I/O	HSTL	XRAM Data bit
AG21	XRAM2_DATA_29	I/O	HSTL	XRAM Data bit
AG23	XRAM2_DATA_30	I/O	HSTL	XRAM Data bit
AG22	XRAM2_DATA_31	I/O	HSTL	XRAM Data bit
AK22	XRAM2_DATA_32	I/O	HSTL	XRAM Data bit
AH22	XRAM2_DATA_33	I/O	HSTL	XRAM Data bit
AE22	XRAM2_DATA_34	I/O	HSTL	XRAM Data bit
AF22	XRAM2_DATA_35	I/O	HSTL	XRAM Data bit (MSB)
AG15	XRAM2_DVLD	I	HSTL	XRAM Data Valid Input This pin should come from the RLDRAM devices associated with XRAM_DATA[8:0].
AK16	XRAM2_DK0_N	O	HSTL	XRAM Differential Output clock (bits 0-8)
AK17	XRAM2_DK0_P	O	HSTL	XRAM Differential Output clock (bits 0-8)
AH16	XRAM2_DK1_N	O	HSTL	XRAM Differential Output clock (bits 9-17)
AG16	XRAM2_DK1_P	O	HSTL	XRAM Differential Output clock (bits 9-17)
AF20	XRAM2_DK2_N	O	HSTL	XRAM Differential Output clock (bits 18-26)
AE20	XRAM2_DK2_P	O	HSTL	XRAM Differential Output clock (bits 18-26)
AG20	XRAM2_DK3_N	O	HSTL	XRAM Differential Output clock (bits 27-35)
AH20	XRAM2_DK3_P	O	HSTL	XRAM Differential Output clock (bits 27-35)
AF12	XRAM2_DQS0_N	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
AE12	XRAM2_DQS0_P	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
AH12	XRAM2_DQS1_N	I	HSTL	XRAM Differential Input strobe (bits 9-17)
AJ12	XRAM2_DQS1_P	I	HSTL	XRAM Differential Input strobe (bits 9-17)
AG13	XRAM2_DQS2_N	I	HSTL	XRAM Differential Input strobe (bits 18-26)
AF13	XRAM2_DQS2_P	I	HSTL	XRAM Differential Input strobe (bits 18-26)
AK13	XRAM2_DQS3_N	I	HSTL	XRAM Differential Input strobe (bits 27-35)
AJ13	XRAM2_DQS3_P	I	HSTL	XRAM Differential Input strobe (bits 27-35)
AD12	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD13	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD14	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)

Table 2-2 XRAM Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AD16	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD18	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD20	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD21	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD22	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD24	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH13	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH15	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH17	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH19	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH21	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH23	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH25	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH27	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH29	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AC15	XRAM2_VREF1	I	Analog	Connect to XRAM reference voltage (0.9V)
AC18	XRAM2_VREF2	I	Analog	Connect to XRAM reference voltage (0.9V)
AD19	XRAM2_VREF3	I	Analog	Connect to XRAM reference voltage (0.9V)

Length and Routing Recommendations

Given the timing values specified in "Timing Characteristics" on page 26, the guidelines described in this section should be observed.

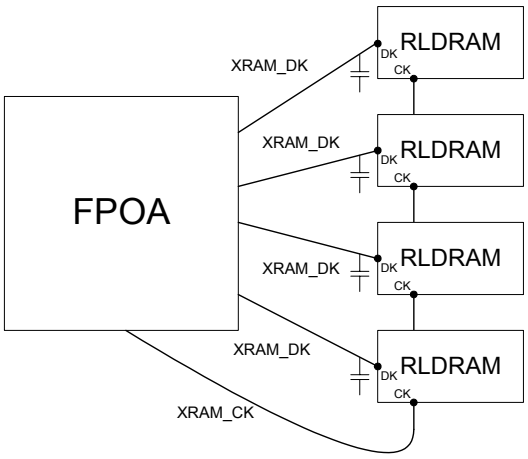
Clock Alignment

Alignment of clocks at the RLDRAM CK and DK pins must be ensured. To meet the timing of the RLDRAM device, the CK and DK nets must closely match wire lengths and loading. There are two options for connecting the clocks:

OPTION 1) *Use the FPOA CK output to drive the RLDRAM CK input pins and use the FPOA DK output to drive the RLDRAM DK input pins*

With this option, the XRAM_CK net will naturally be longer and more heavily loaded than the XRAM_DK nets (when multiple RLDRAM devices are used). The XRAM_CK net will see approximately 2-3 pF of load for each RLDRAM device. To meet timing specs, the XRAM_DK traces will need to be lengthened to match the length of the XRAM_CK trace (see Table 2-3) and these traces may need additional capacitors to match the device load of the XRAM_CK net. Place the capacitor near the XRAM_DK termination resistor as shown in Figure 2-2.

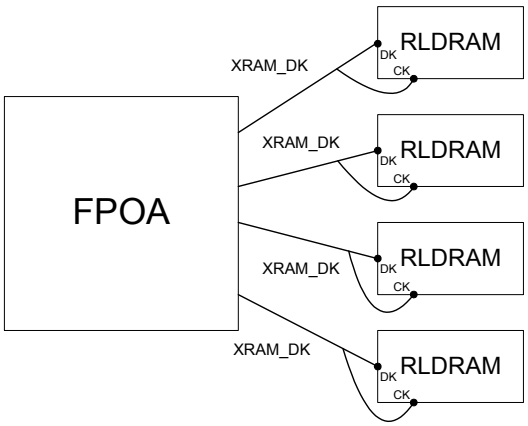
Figure 2-2 XRAM Clock Routing Option #1



OPTION 2) *Use the FPOA DK output to drive both the RLDRAM CK and RLDRAM DK input pins*

With this option, the timing requirements of CK and DK will naturally be met. The FPOA CK output pin is not used for this option and should be terminated to VTT.

Figure 2-3 XRAM Clock Routing Option #2



Length Recommendations

Table 2-3 illustrates the minimum and maximum lengths for the XRAM pins. These lengths denote the maximum difference that can be reasonably tolerated to close system timing. Tightening these values will provide more timing margin and more robust RLDRAM operation.

Table 2-3 XRAM Length Recommendations[a]

Symbol	FPOA Pins	Minimum Trace Length[b,c]	Maximum Trace Length[b, c]	Details
CLK	XRAM*_CLK_*			CLK is the trace length used as the basis for the other XRAM trace lengths.
ADDR/CNTL /BANK	XRAM*_ADDR_* XRAM*_CNTL_* XRAM*_BANK_*	CLK - 1”	CLK + 2”	
DK	XRAM*_DK_*	CLK - 0.5”	CLK + 1”	Lengths for DK traces must match within a one inch tolerance.
DQS	XRAM*_DQS_*	CLK - 1”	CLK + 1”	Lengths for DQS traces must match within a one inch tolerance.
DATA	XRAM*_DATA_* XRAM*_DVLD_*	Must be greater than both DK - 1” and DQS - 1”	Must be less than both DK and DQS	Maximum difference between minimum DATA length and maximum ADDR/CNTL/BANK length is four inches.

a. These values assume 266 MHz operation (or less) using a 300 MHz RLDRAM device.
b. Values are specified in inches.
c. Values assume 175 picoseconds of delay per inch.

Termination

Each signal is terminated with a 50 Ω resistor to VTT.

Table 2-4 XRAM Termination

XRAM 1	XRAM 2
Locate termination resistor near RLDRAM	
XRAM1_ADDR_0 through XRAM1_ADDR_20	XRAM2_ADDR_0 through XRAM2_ADDR_20
XRAM1_CNTL_2 (CS#)	XRAM2_CNTL_2 (CS#)
XRAM1_CNTL_0 (REF#)	XRAM2_CNTL_0 (REF#)
XRAM1_CNTL_1 (WE#)	XRAM2_CNTL_1 (WE#)
XRAM1_BANK_0	XRAM2_BANK_0
XRAM1_BANK_1	XRAM2_BANK_1
XRAM1_BANK_2	XRAM2_BANK_2
XRAM1_CLK_P and XRAM1_CLK _N (clock pair)	XRAM2_CLK_P and XRAM2_CLK _N (clock pair)
XRAM1_DK0_P and XRAM1_DK0_N (clock pair)	XRAM2_DK0_P and XRAM2_DK0_N (clock pair)
XRAM1_DK1_P and XRAM1_DK1_N (clock pair)	XRAM2_DK1_P and XRAM2_DK1_N (clock pair)
XRAM1_DK2_P and XRAM1_DK2_N (clock pair)	XRAM2_DK2_P and XRAM2_DK2_N (clock pair)
XRAM1_DK3_P and XRAM1_DK3_N (clock pair)	XRAM2_DK3_P and XRAM2_DK3_N (clock pair)

Table 2-4 XRAM Termination (Continued)

XRAM 1	XRAM 2
Locate termination resistor near FPOA	
XRAM1_DVLD	XRAM2_DVLD
XRAM1_DQS0_P and XRAM1_DQS0_N (clock pair)	XRAM2_DQS0_P and XRAM2_DQS0_N (clock pair)
XRAM1_DQS1_P and XRAM1_DQS1_N (clock pair)	XRAM2_DQS1_P and XRAM2_DQS1_N (clock pair)
XRAM1_DQS2_P and XRAM1_DQS2_N (clock pair)	XRAM2_DQS2_P and XRAM2_DQS2_N (clock pair)
XRAM1_DQS3_P and XRAM1_DQS3_N (clock pair)	XRAM2_DQS3_P and XRAM2_DQS3_N (clock pair)
Locate termination resistor between RLDRAM and FPOA	
XRAM1_DATA_0 through XRAM1_DATA_35	XRAM2_DATA_0 through XRAM2_DATA_35

Timing Characteristics

Figure 2-4 illustrates the offset between the XRAM clock and the RLDRAM data clock. Timing values are specified in Table 2-5 on page 29.

Figure 2-4 XRAM Clock to Data Clock Timing

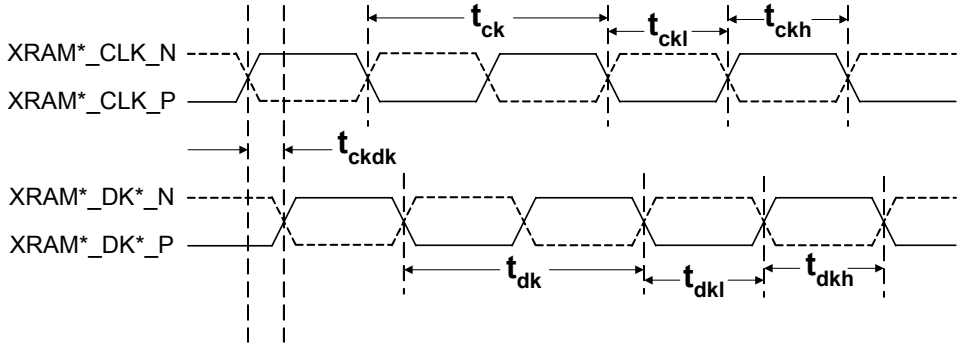


Figure 2-5 illustrates the minimum and maximum valid times for sending address and control signals.

Figure 2-5 XRAM Address and Control Timing

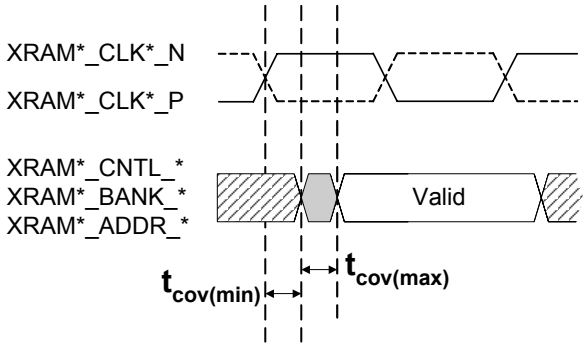


Figure 2-6 illustrates the minimum cycle time (in number of clock cycles) after issuing the MRS command. This command can be issued automatically by the XRAM controller or manually. For more information, see "Initialization" on page 32.

Figure 2-6 XRAM MRS Timing

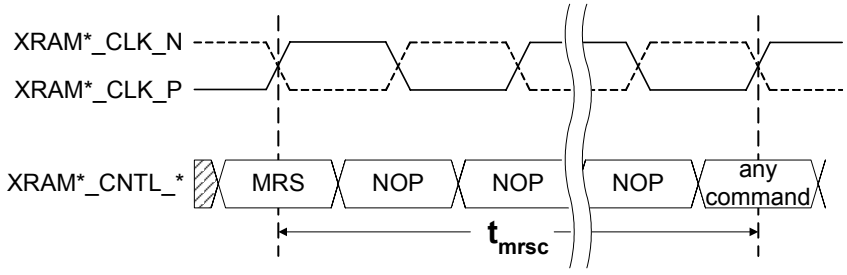


Figure 2-7 illustrates the timing characteristics when writing data to the RLDRAM.

Figure 2-7 XRAM Data Write Timing

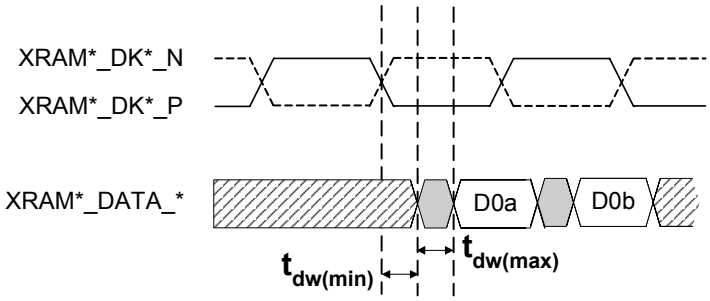


Figure 2-8 illustrates the latency when writing data to the RLDRAM and the minimum refresh time before writing to the same bank.

Figure 2-8 XRAM Write Latency

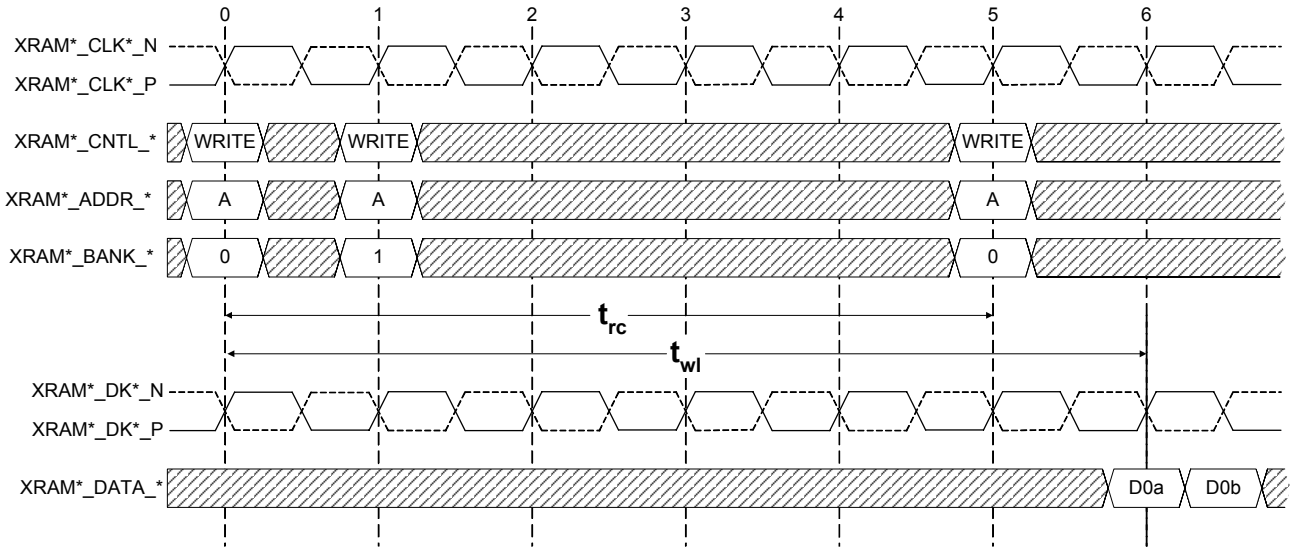


Figure 2-9 illustrates the timing characteristics when reading data from the RLDRAM.

Figure 2-9 XRAM Data Read Timing

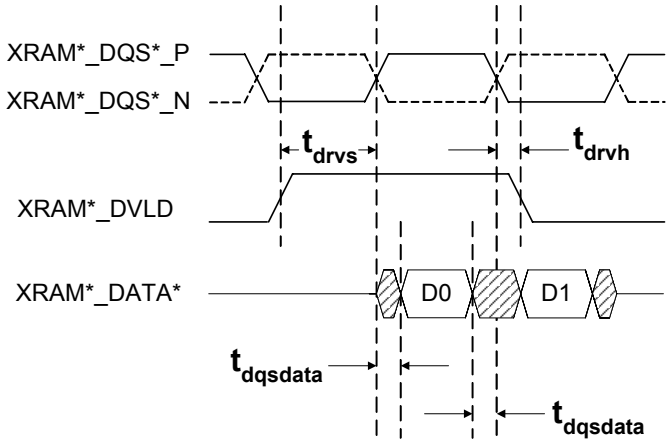
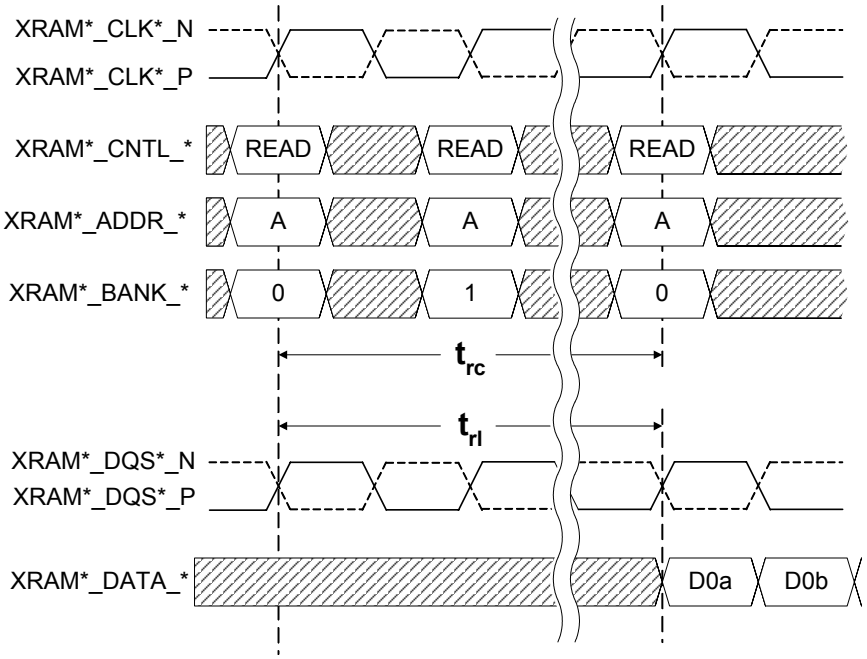


Figure 2-10 illustrates the latency when reading data from the RLDRAM and the minimum refresh time before reading from the same bank.

Figure 2-10 XRAM Read Latency



Since writing to the XRAM is one clock slower than reading from the XRAM, there must be a one clock delay for a read command after a write command, as shown in Figure 2-11. This delay is enforced by the controller even if the read command is sent immediately after the write command.

Figure 2-11 XRAM Write Followed By Read Timing

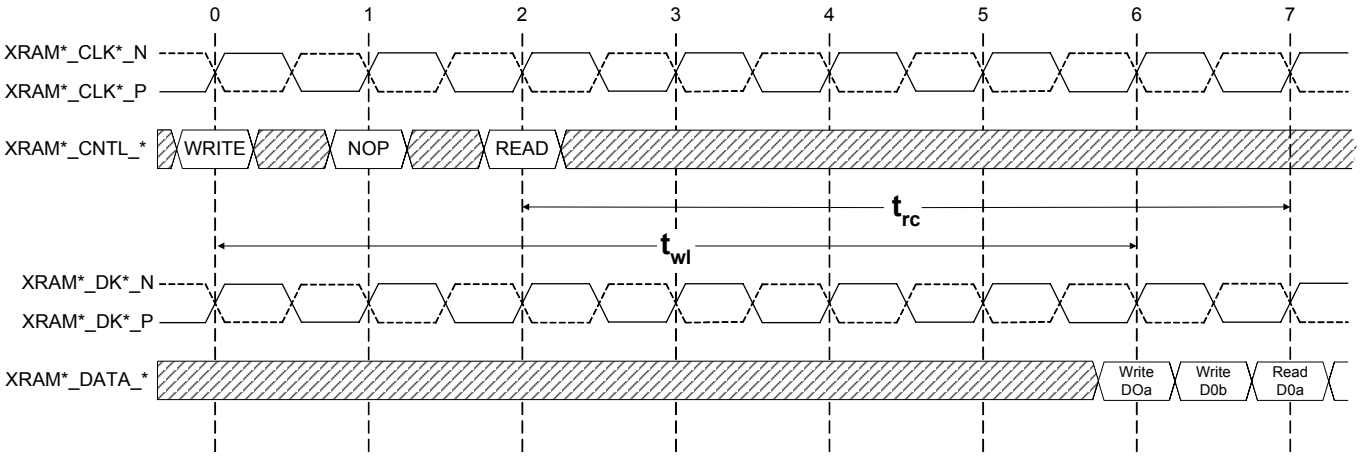


Table 2-5 XRAM Timing Characteristics

Parameter	Description	Min	Max
Clock Timing[a]			
t_{ck}, t_{dk}	Clock Cycle Time	3.76 ns (266 MHz)	5.71 ns (175 MHz)
t_{ckl}, t_{dkl}	Clock LOW Time	0.47 t_{ck}	0.53 t_{ck}
t_{ckh}, t_{dkh}	Clock HIGH Time	0.47 t_{ck}	0.53 t_{ck}
t_{ckdk}	Clock to I/O Data Clock	-300 ps	300 ps
t_{fall}	Clock Fall Time	550 ps	850 ps
t_{rise}	Clock Rise Time	500 ps	900 ps
Address & Control Timing			
t_{mrsc}	Mode Register Set Cycle Time	6 clock cycles	
t_{cov}	Address & Control Output Valid	500 ps	1600 ps

Table 2-5 XRAM Timing Characteristics (Continued)

Parameter	Description	Min	Max
Data Write Timing			
t_{dw}	Data Write Valid	300 ps	900 ps
t_{rc}	Minimum Row Cycle Time	Configuration parameter name: min_row_cycle_time[b,c] (typically 5 clocks)	
t_{wl}	Write Latency	Configuration parameter name: wr_latency[b,c] (typically 6 clocks)	
Data Read Timing			
t_{drvs}	DVLD to DQS Edge Setup		0 ps
t_{drvh}	DVLD Hold		$t_{ck}/4$ + 300 ps
$t_{dqsdata}$	DQS Edge to Data Edge	$t_{ck}/4$ - 300 ps	$t_{ck}/4$ + 300 ps
t_{rc}	Minimum Row Cycle Time	Configuration parameter name: min_row_cycle_time[b,c] (typically 5 clocks)	
t_{rl}	Read Latency	Configuration parameter name: wr_latency - 1 [b,c] (typically 5 clocks)	

a. See Chapter 8: Clock Characteristics for additional clock information.
b. See the Application Developer's Object Reference for information about configuring this parameter.
c. See the RLDRAM Data Sheet for constraints for each RLDRAM configuration.

RLDRAM Details

The following section describes some key characteristics of the RLDRAMII hardware. Visit http://www.micron.com/rldram for more information.

Configurations

The XRAM controller has been designed to directly connect to the 288 Mbit RLDRAM specification and can support one, two, or four parallel memory device configurations at the board level. Table 2-6 details these configurations.

Table 2-6 RLDRAM Configurations

Number of Devices	Component Type	Total Memory Size Per Interface	Model
1	8M x 36	36 MBytes	Micron MT49H8M36FM
2	16M x 18	72 MBytes	Micron MT49H16M18FM
4	32M x 9	144 MBytes	Micron MT49H32M9FM

Bank Selection

Once one of the eight internal banks within an RLDRAM is accessed, it cannot be accessed again for the minimum row cycle time (t_{rc}) as shown in Figure 2-8 on page 27 and Figure 2-10 on page 28. Maximum bandwidth is achieved by accessing another bank that has met its minimum row cycle time requirement. The XRAM controller automatically guarantees that minimum row cycle time is met for all memory accesses by inserting wait states as needed. For more information on optimizing RLDRAM access timing, see the Application Developer's Object Reference.

Command Codes

The following table lists the command codes available via the three control pins (XRAM*_CNTL_*). See the Application Developer's Object Reference for more information on issuing XRAM commands.

Table 2-7 RLDRAM Command Codes

Command	CNTL_2 (CS#)	CNTL_1 (WE#)	CNTL_0 (REF#)	Description
NOP	H	X	X	Device deselect / No operation. This command is used to perform no operation, which essentially deselects the chip. Operations already in progress are not affected.
MRS	L	L	L	Mode register set. This command stores the data for controlling the operating modes of the memory. It programs the burst length, test mode, and I/O options. This command can automatically be issued by the XRAM controller.
READ	L	H	H	Read. This command is used to initiate a burst read access to a bank.
WRITE	L	L	H	Write. This command is used to initiate a burst write access to a bank.
AREF	L	H	L	Auto refresh. This command is used during normal operation to refresh the memory content of a bank. The command is nonpersistent and must be issued each time a refresh is required.

NOTES:
1. H = Logic high
2. L = Logic low
3. X = "Don't care"

Initialization

The RLDRAM can be initialized automatically by the controller at startup. This option is configurable via the configuration parameter "init_rldram2[1]." The application can also initiate initialization through an XRAM controller command code. In either case, the XRAM controller performs the following initialization sequence:

1. Power is applied and the clock starts as soon as the XRAM is configured.

2. The controller waits for a time specified by the configuration parameter "init_wait_tc." This time must be at least 200 μs.

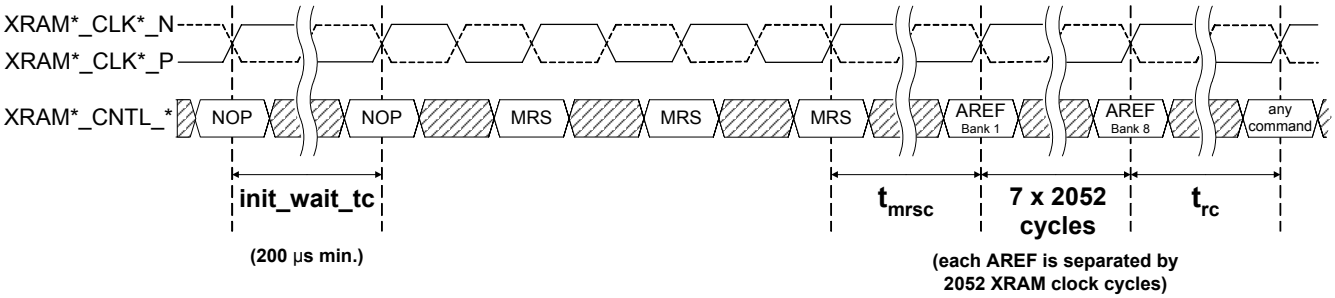
1. See the Application Developer's Object Reference for information on this and other application-controlled configuration parameters.

3. Three consecutive MRS commands are issued: two dummies plus one valid MRS[1].

4. After the mode register set cycle time (t_{mrsc} from Table 2-5 on page 29), eight AREF commands are issued, one on each bank separated by 2052 cycles.

5. After the row cycle time (t_{rc} from Table 2-5 on page 29), the chip is ready for normal operation.

Figure 2-12 RLDRAM Initialization Sequence



For manual initialization, consult the RLDRAM Data Sheet for timing considerations.

Refresh Behavior

There are several ways to configure the XRAM controller's refresh behavior:

- Auto refresh — Refresh can be performed automatically by the controller or it can be performed manually by the application. By default, automatic refresh is turned on.
- Refresh style — Refresh can occur as a burst of eight refresh commands (one for each bank), or it can occur one bank at a time. By default, refresh will occur as a burst. Additionally, burst refresh can occur one or more consecutive times. This capability is useful for applications such as video processing applications where the refresh occurs during the video synchronization period.
- Refresh interval count — Regardless or which refresh style is selected, the number of XRAM clocks between refreshes is configurable.

These values are all controlled through configuration parameters, which are described in more detail in the Application Developer's Object Reference.

1. Although the MRS value is configurable by the application developer ("rldram2_mrs"), the XRAM controller requires a burst length of two (bits[4:3] = 00) and that the RLDRAM is in non-multiplexed mode (bit[5] = 0).

Chapter 3
GPIO Hardware

Overview

The GPIO interface object facilitates communication between the FPOA and external devices. Each Arrix product provides two GPIO interfaces, one on the north side of the periphery and one on the south side. Each interface provides 48 bidirectional pins operating at LVCMOS signaling levels.

The GPIO interface on the north side is associated with the GPIO1_* pins while the interface on the south side is associated with the GPIO2_* pins. Each interface has 48 data pins, 1 clock pin, and 12 pins associated with power. The direction of the data pins (i.e. input / output) can be configured statically at initialization or dynamically at runtime. Data can be received/transmitted synchronously or asynchronously. See the Application Developer's Object Reference for more information on GPIO interface configurations.

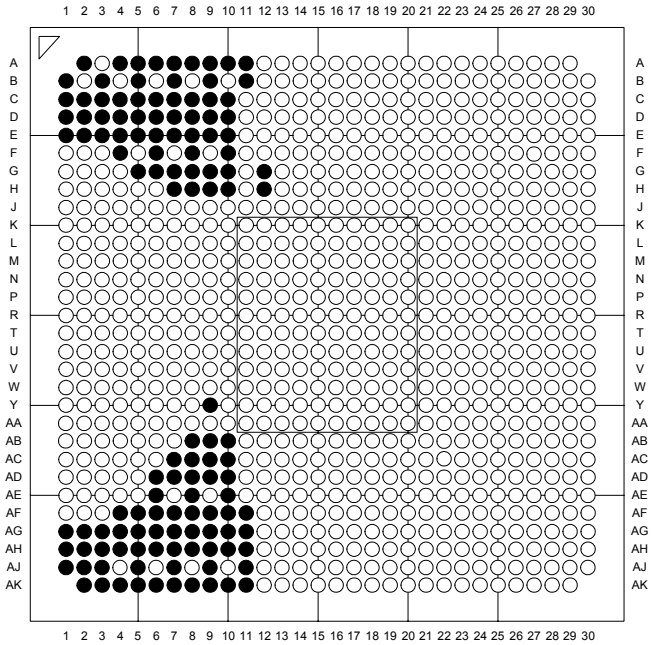
Table 3-1 GPIO General Characteristics

Characteristic	Description
Supported Frequency	0 MHz – 100 MHz See Chapter 8: Clock Characteristics for more information.
Signal Control	On a per nibble basis, GPIO signals may be configured for: ❋ Synchronous or asynchronous clocking ❋ Input, output, or bidirection operation
Signal Information	❋ 2.5 volts (LVCMOS) ❋ Inputs are 3.3 volt tolerant ❋ 16mA drive for the GPIO clocks ❋ Single-ended 50 Ω impedance ❋ No termination
Load Per Signal	❋ 10pF @ 100MHz ❋ 20pF @ 66MHz

External Pins

Table 3-2 describes the pins associated with the GPIO interface. For a list of all pins associated with the Arrix family FPOA, see Appendix A: External Pins.

Figure 3-1 Ball Pattern for GPIO (Top-down View)



NOTE: GPIO-related balls are shown in black.

Table 3-2 GPIO Pin Descriptions

Pin Number	Signal	Type	Signal Type	Notes
GPIO 1				
D1	GPIO1_0	I/O	LVCMOS	GPIO data bit
E1	GPIO1_1	I/O	LVCMOS	GPIO data bit
E3	GPIO1_2	I/O	LVCMOS	GPIO data bit
G5	GPIO1_3	I/O	LVCMOS	GPIO data bit
F4	GPIO1_4	I/O	LVCMOS	GPIO data bit
C2	GPIO1_5	I/O	LVCMOS	GPIO data bit
C1	GPIO1_6	I/O	LVCMOS	GPIO data bit
E4	GPIO1_7	I/O	LVCMOS	GPIO data bit
F6	GPIO1_8	I/O	LVCMOS	GPIO data bit
E5	GPIO1_9	I/O	LVCMOS	GPIO data bit

Table 3-2 GPIO Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
H7	GPIO1_10	I/O	LVCMOS	GPIO data bit
G7	GPIO1_11	I/O	LVCMOS	GPIO data bit
D4	GPIO1_12	I/O	LVCMOS	GPIO data bit
D3	GPIO1_13	I/O	LVCMOS	GPIO data bit
B1	GPIO1_14	I/O	LVCMOS	GPIO data bit
A2	GPIO1_15	I/O	LVCMOS	GPIO data bit
C4	GPIO1_16	I/O	LVCMOS	GPIO data bit
B3	GPIO1_17	I/O	LVCMOS	GPIO data bit
A3	GPIO1_18	I/O	LVCMOS	GPIO data bit
D5	GPIO1_19	I/O	LVCMOS	GPIO data bit
D6	GPIO1_20	I/O	LVCMOS	GPIO data bit
C6	GPIO1_21	I/O	LVCMOS	GPIO data bit
B5	GPIO1_22	I/O	LVCMOS	GPIO data bit
A4	GPIO1_23	I/O	LVCMOS	GPIO data bit
E7	GPIO1_24	I/O	LVCMOS	GPIO data bit
F8	GPIO1_25	I/O	LVCMOS	GPIO data bit
E6	GPIO1_26	I/O	LVCMOS	GPIO data bit
C8	GPIO1_27	I/O	LVCMOS	GPIO data bit
A6	GPIO1_28	I/O	LVCMOS	GPIO data bit
A5	GPIO1_29	I/O	LVCMOS	GPIO data bit
B7	GPIO1_30	I/O	LVCMOS	GPIO data bit
D8	GPIO1_31	I/O	LVCMOS	GPIO data bit
E8	GPIO1_32	I/O	LVCMOS	GPIO data bit
G9	GPIO1_33	I/O	LVCMOS	GPIO data bit
E9	GPIO1_34	I/O	LVCMOS	GPIO data bit
A8	GPIO1_35	I/O	LVCMOS	GPIO data bit
A7	GPIO1_36	I/O	LVCMOS	GPIO data bit
B9	GPIO1_37	I/O	LVCMOS	GPIO data bit
A9	GPIO1_38	I/O	LVCMOS	GPIO data bit
D9	GPIO1_39	I/O	LVCMOS	GPIO data bit
F10	GPIO1_40	I/O	LVCMOS	GPIO data bit

Table 3-2 GPIO Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
C10	GPIO1_41	I/O	LVCMOS	GPIO data bit
A10	GPIO1_42	I/O	LVCMOS	GPIO data bit
H10	GPIO1_43	I/O	LVCMOS	GPIO data bit
E10	GPIO1_44	I/O	LVCMOS	GPIO data bit
D10	GPIO1_45	I/O	LVCMOS	GPIO data bit
A11	GPIO1_46	I/O	LVCMOS	GPIO data bit
B11	GPIO1_47	I/O	LVCMOS	GPIO data bit
D7	GPIO1_CLK	I/O	LVCMOS	GPIO clock[a]
C3	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
C5	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
C7	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
C9	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
E2	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G6	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G8	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G10	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G12	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
H8	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
H9	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
H12	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
GPIO 2				
AG1	GPIO2_0	I/O	LVCMOS	GPIO data bit
AH1	GPIO2_1	I/O	LVCMOS	GPIO data bit
AJ1	GPIO2_2	I/O	LVCMOS	GPIO data bit
AG3	GPIO2_3	I/O	LVCMOS	GPIO data bit
AH2	GPIO2_4	I/O	LVCMOS	GPIO data bit
AJ2	GPIO2_5	I/O	LVCMOS	GPIO data bit
AK2	GPIO2_6	I/O	LVCMOS	GPIO data bit
AJ3	GPIO2_7	I/O	LVCMOS	GPIO data bit
AG2	GPIO2_8	I/O	LVCMOS	GPIO data bit
AG4	GPIO2_9	I/O	LVCMOS	GPIO data bit

Table 3-2 GPIO Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AH4	GPIO2_10	I/O	LVCMOS	GPIO data bit
AF5	GPIO2_11	I/O	LVCMOS	GPIO data bit
AG5	GPIO2_12	I/O	LVCMOS	GPIO data bit
AK3	GPIO2_13	I/O	LVCMOS	GPIO data bit
AC7	GPIO2_14	I/O	LVCMOS	GPIO data bit
AD7	GPIO2_15	I/O	LVCMOS	GPIO data bit
AF6	GPIO2_16	I/O	LVCMOS	GPIO data bit
AG6	GPIO2_17	I/O	LVCMOS	GPIO data bit
AB9	GPIO2_18	I/O	LVCMOS	GPIO data bit
AC9	GPIO2_19	I/O	LVCMOS	GPIO data bit
AB8	GPIO2_20	I/O	LVCMOS	GPIO data bit
AC8	GPIO2_21	I/O	LVCMOS	GPIO data bit
AE8	GPIO2_22	I/O	LVCMOS	GPIO data bit
AF8	GPIO2_23	I/O	LVCMOS	GPIO data bit
AK4	GPIO2_24	I/O	LVCMOS	GPIO data bit
AH6	GPIO2_25	I/O	LVCMOS	GPIO data bit
AJ5	GPIO2_26	I/O	LVCMOS	GPIO data bit
AK5	GPIO2_27	I/O	LVCMOS	GPIO data bit
AD9	GPIO2_28	I/O	LVCMOS	GPIO data bit
AG8	GPIO2_29	I/O	LVCMOS	GPIO data bit
AK6	GPIO2_30	I/O	LVCMOS	GPIO data bit
AH8	GPIO2_31	I/O	LVCMOS	GPIO data bit
AJ7	GPIO2_32	I/O	LVCMOS	GPIO data bit
AK7	GPIO2_33	I/O	LVCMOS	GPIO data bit
AK8	GPIO2_34	I/O	LVCMOS	GPIO data bit
AE10	GPIO2_35	I/O	LVCMOS	GPIO data bit
AF10	GPIO2_36	I/O	LVCMOS	GPIO data bit
AF9	GPIO2_37	I/O	LVCMOS	GPIO data bit
AG9	GPIO2_38	I/O	LVCMOS	GPIO data bit
AG10	GPIO2_39	I/O	LVCMOS	GPIO data bit
AH10	GPIO2_40	I/O	LVCMOS	GPIO data bit

Table 3-2 GPIO Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AK9	GPIO2_41	I/O	LVCMOS	GPIO data bit
AJ9	GPIO2_42	I/O	LVCMOS	GPIO data bit
AK10	GPIO2_43	I/O	LVCMOS	GPIO data bit
AK11	GPIO2_44	I/O	LVCMOS	GPIO data bit
AF11	GPIO2_45	I/O	LVCMOS	GPIO data bit
AG11	GPIO2_46	I/O	LVCMOS	GPIO data bit
AJ11	GPIO2_47	I/O	LVCMOS	GPIO data bit
AG7	GPIO2_CLK	I/O	LVCMOS	GPIO clock[a]
Y9	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AB10	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AC10	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AD6	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AD8	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AD10	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AE6	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AF4	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AF7	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH3	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH5	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH7	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH9	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH11	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)

a. 16mA drive for the GPIO clock

Timing Characteristics

Figure 3-2 illustrates the timing characteristics when the GPIO interface is used for input.

Figure 3-2 GPIO Input Timing (Synchronous)

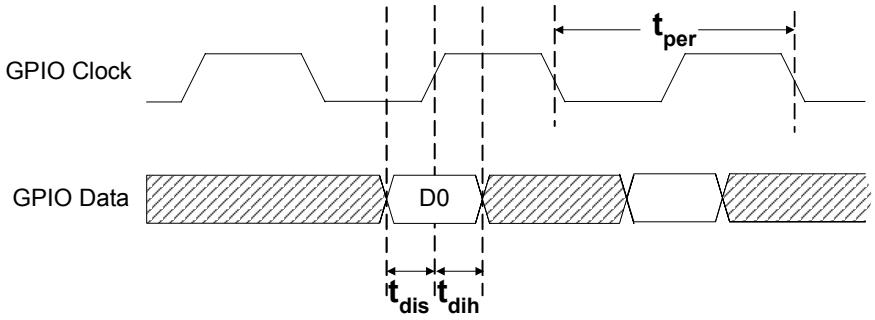


Figure 3-3 illustrates the timing characteristics when the GPIO interface is used for output.

Figure 3-3 GPIO Output Timing (Synchronous)

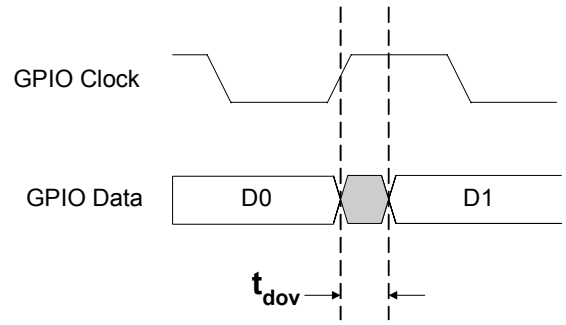
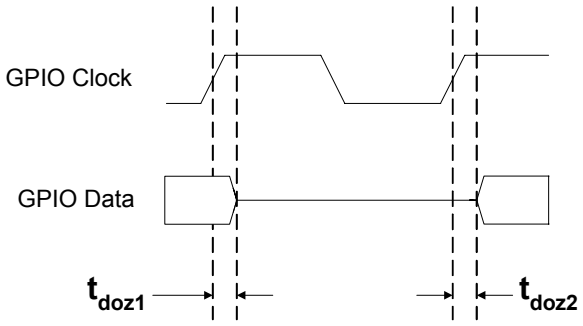


Figure 3-4 illustrates the timing characteristics when the data pins enter and leave tri-state.

Figure 3-4 GPIO Output Tri-state Timing



For information about the latency to/from the party line signals consult the Application Developer's Object Reference.

Table 3-3 GPIO Timing (using an externally-derived clock)

Parameter	Description	Min	Max
Clock Timing[a]			
t_{per}	GPIO Clock Period	10 ns	
Input Timing			
t_{dis}	Data Input Setup		0.500 ns
t_{dih}	Data Input Hold		0.500 ns
Output Timing			
t_{dov}	Data Output Valid	2.0 ns	5.0 ns
t_{doz1}	Data Output Enter Tristate	1.0 ns	2.5 ns
t_{doz2}	Data Output Exit Tristate	2.0 ns	5.0 ns

a. See Chapter 8: Clock Characteristics for additional clock information.

Table 3-4 GPIO Timing (using an internally-derived clock)

Parameter	Description	Min	Max
Clock Timing[a]			
t_{per}	GPIO Clock Period	10 ns	
Input Timing			
t_{dis}	Data Input Setup		2.0 ns
t_{dih}	Data Input Hold		0 ns
Output Timing			
t_{dov}	Data Output Valid	1.0 ns	3.0 ns
t_{doz1}	Data Output Enter Tristate	0.3 ns	1.0 ns
t_{doz2}	Data Output Exit Tristate	1.0 ns	3.0 ns

a. See Chapter 8: Clock Characteristics for additional clock information.

Chapter 4
RX Hardware

Overview

The RX interface is used for high-speed parallel LVDS input to the FPOA. Each Arrix product provides two RX interfaces, one on the east side of the periphery and one on the west side.

The RX interface on the east side is associated with the RX1_* pins while the interface on the west side is associated with the RX2_* pins. Each signal has both a negative (RX*_N) and a positive (RX*_P) pin comprising the differential pair. Each interface has 1 clock pin pair, 1 control pin pair, 16 data pin pairs, and 10 pins associated with power.

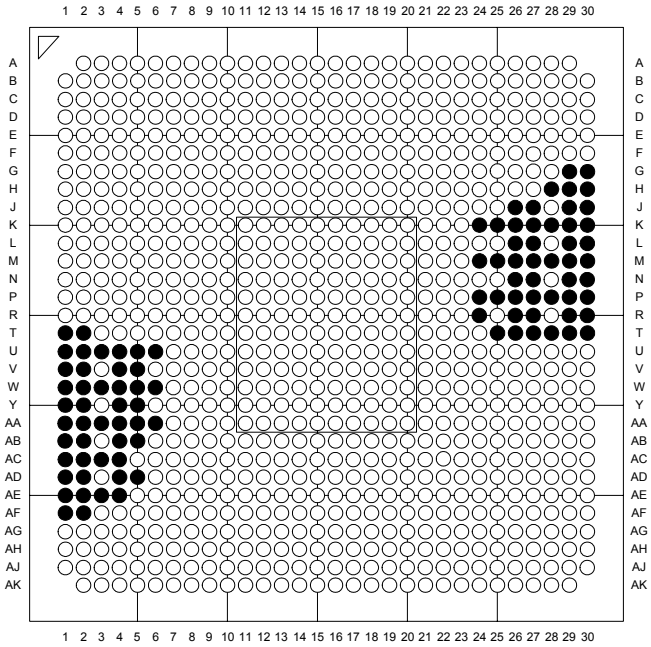
Table 4-1 RX General Characteristics

Characteristic	Description
Data Rate	SDR / DDR (programmable)
Supported Frequency	❋ 116 MHz – 500 MHz (DDR) ❋ 116 MHz – 640 MHz (SDR)
Signal Information	❋ 1.25 V (LVDS) ❋ Differential pairs, 100Ω impedance

External Pins

Table 4-2 describes the pins associated with the RX interface. For a list of all pins associated with the Arrix family FPOA, see Appendix A: External Pins.

Figure 4-1 Ball Pattern for RX (Top-down View)



NOTE: RX-related balls are shown in black.

Table 4-2 RX Pin Descriptions

Pin Number	Signal	Type	Signal Type	Notes
Receive Datapath 1				
V5	RX1_CLK1_N	I	LVDS	Receive Clock
V4	RX1_CLK1_P	I	LVDS	Receive Clock
AA5	RX1_CNTL_N	I	LVDS	Receive Control bit
AA6	RX1_CNTL_P	I	LVDS	Receive Control bit
T2	RX1_DATA_0_N	I	LVDS	Receive Data bit (LSB)
T1	RX1_DATA_0_P	I	LVDS	Receive Data bit
U2	RX1_DATA_1_N	I	LVDS	Receive Data bit
U3	RX1_DATA_1_P	I	LVDS	Receive Data bit
U5	RX1_DATA_2_N	I	LVDS	Receive Data bit

Table 4-2 RX Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
U6	RX1_DATA_2_P	I	LVDS	Receive Data bit
V2	RX1_DATA_3_N	I	LVDS	Receive Data bit
V1	RX1_DATA_3_P	I	LVDS	Receive Data bit
W2	RX1_DATA_4_N	I	LVDS	Receive Data bit
W3	RX1_DATA_4_P	I	LVDS	Receive Data bit
W6	RX1_DATA_5_N	I	LVDS	Receive Data bit
W5	RX1_DATA_5_P	I	LVDS	Receive Data bit
Y1	RX1_DATA_6_N	I	LVDS	Receive Data bit
Y2	RX1_DATA_6_P	I	LVDS	Receive Data bit
Y4	RX1_DATA_7_N	I	LVDS	Receive Data bit
Y5	RX1_DATA_7_P	I	LVDS	Receive Data bit
AA2	RX1_DATA_8_N	I	LVDS	Receive Data bit
AA3	RX1_DATA_8_P	I	LVDS	Receive Data bit
AB1	RX1_DATA_9_N	I	LVDS	Receive Data bit
AB2	RX1_DATA_9_P	I	LVDS	Receive Data bit
AC3	RX1_DATA_10_N	I	LVDS	Receive Data bit
AC2	RX1_DATA_10_P	I	LVDS	Receive Data bit
AB4	RX1_DATA_11_N	I	LVDS	Receive Data bit
AB5	RX1_DATA_11_P	I	LVDS	Receive Data bit
AD1	RX1_DATA_12_N	I	LVDS	Receive Data bit
AD2	RX1_DATA_12_P	I	LVDS	Receive Data bit
AD4	RX1_DATA_13_N	I	LVDS	Receive Data bit
AD5	RX1_DATA_13_P	I	LVDS	Receive Data bit
AE2	RX1_DATA_14_N	I	LVDS	Receive Data bit
AE3	RX1_DATA_14_P	I	LVDS	Receive Data bit
AF1	RX1_DATA_15_N	I	LVDS	Receive Data bit
AF2	RX1_DATA_15_P	I	LVDS	Receive Data bit (MSB)
U1	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
U4	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
W1	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
W4	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V

Table 4-2 RX Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AA1	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AA4	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AC1	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AC4	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AE1	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AE4	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
Receive Datapath 2				
P26	RX2_CLK1_N	I	LVDS	Receive Clock
P25	RX2_CLK1_P	I	LVDS	Receive Clock
M26	RX2_CNTL_N	I	LVDS	Receive Control bit
M25	RX2_CNTL_P	I	LVDS	Receive Control bit
T28	RX2_DATA_0_N	I	LVDS	Receive Data bit (LSB)
T29	RX2_DATA_0_P	I	LVDS	Receive Data bit
T26	RX2_DATA_1_N	I	LVDS	Receive Data bit
T25	RX2_DATA_1_P	I	LVDS	Receive Data bit
R29	RX2_DATA_2_N	I	LVDS	Receive Data bit
R30	RX2_DATA_2_P	I	LVDS	Receive Data bit
R27	RX2_DATA_3_N	I	LVDS	Receive Data bit
R26	RX2_DATA_3_P	I	LVDS	Receive Data bit
P28	RX2_DATA_4_N	I	LVDS	Receive Data bit
P29	RX2_DATA_4_P	I	LVDS	Receive Data bit
N29	RX2_DATA_5_N	I	LVDS	Receive Data bit
N30	RX2_DATA_5_P	I	LVDS	Receive Data bit
N27	RX2_DATA_6_N	I	LVDS	Receive Data bit
N26	RX2_DATA_6_P	I	LVDS	Receive Data bit
M28	RX2_DATA_7_N	I	LVDS	Receive Data bit
M29	RX2_DATA_7_P	I	LVDS	Receive Data bit
L30	RX2_DATA_8_N	I	LVDS	Receive Data bit
L29	RX2_DATA_8_P	I	LVDS	Receive Data bit
L27	RX2_DATA_9_N	I	LVDS	Receive Data bit
L26	RX2_DATA_9_P	I	LVDS	Receive Data bit

Table 4-2 RX Pin Descriptions (Continued)

Pin Number	Signal	Type	Signal Type	Notes
J30	RX2_DATA_10_N	I	LVDS	Receive Data bit
J29	RX2_DATA_10_P	I	LVDS	Receive Data bit
K28	RX2_DATA_11_N	I	LVDS	Receive Data bit
K29	RX2_DATA_11_P	I	LVDS	Receive Data bit
K25	RX2_DATA_12_N	I	LVDS	Receive Data bit
K26	RX2_DATA_12_P	I	LVDS	Receive Data bit
H29	RX2_DATA_13_N	I	LVDS	Receive Data bit
H28	RX2_DATA_13_P	I	LVDS	Receive Data bit
J27	RX2_DATA_14_N	I	LVDS	Receive Data bit
J26	RX2_DATA_14_P	I	LVDS	Receive Data bit
G29	RX2_DATA_15_N	I	LVDS	Receive Data bit
G30	RX2_DATA_15_P	I	LVDS	Receive Data bit (MSB)
H30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
K24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
K27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
K30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
M24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
M27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
M30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
P24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
P27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
P30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
R24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
T27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
T30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V

Matched Lengths

Match length tolerance is 2/3 inch maximum for each group.

Group 1	Group 2
RX1_DATA_x	RX2_DATA_x
RX1_CLK1_x	RX2_CLK1_x
RX1_CNTL_x	RX2_CNTL_x

Termination

Internal termination is 100 Ω across the differential pairs. No external termination is required.

Timing Characteristics

Figure 4-2 illustrates the timing characteristics in DDR mode when the clock is aligned with the data (i.e. in-phase). Note that these same timing parameters apply when using an inverted clock (though the clock is 180º offset).

Figure 4-2 RX DDR In-Phase Timing

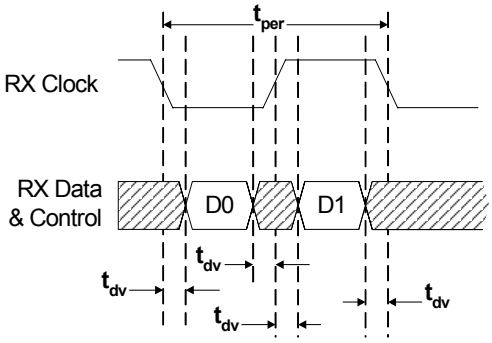


Figure 4-3 illustrates the timing characteristics in DDR mode when the clock is 90º phase-shifted with the data.

Figure 4-3 RX DDR 90º Phase-Shifted Timing

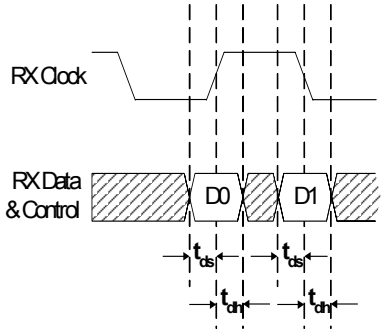


Figure 4-4 illustrates the timing characteristics in SDR mode when the clock is aligned with the data.

Figure 4-4 RX SDR In-Phase Timing

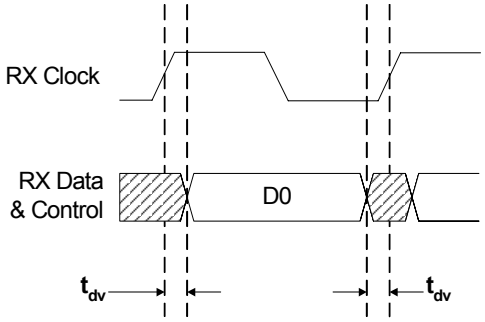


Figure 4-5 illustrates the timing characteristics in SDR mode when the clock is 90º phase-shifted with the data.

Figure 4-5 RX SDR 90º Phase-Shifted Timing

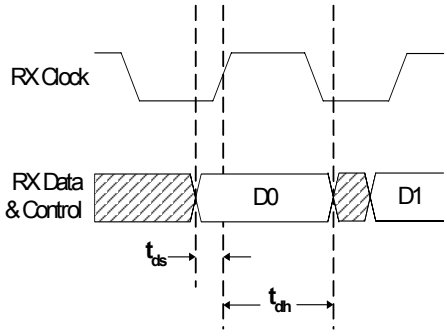


Table 4-3 RX Timing Characteristics

Parameter	Description	Min	Max
Input Timing			
t_{dv}	SDR/DDR Data Valid	$t_{per}/4$ - 175 ps	$t_{per}/4$ + 175 ps
t_{ds}	SDR/DDR 90º Phase-Shifted Data Setup		175 ps
t_{dh}	SDR/DDR 90º Phase-Shifted Data Hold		175 ps
Clock Timing[a]			
t_{per}	Clock Period	1.56 ns (640 MHz SDR) 2.0 ns (500 MHz DDR)	8.62 ns (116 MHz)
RX DLL Lock Time			1200 clocks

a. See Chapter 8: Clock Characteristics for additional clock information.

Chapter 5
TX Hardware

Overview

The TX interface is used for high-speed parallel LVDS output from the FPOA. Each Arrix product provides two TX interfaces, one on the east side of the periphery and one on the west side.

The TX interface on the east side is associated with the TX1_* pins while the interface on the west side is associated with the TX2_* pins. Each signal has both a negative (TX*_N) and a positive (TX*_P) pin comprising the differential pair. Each interface has 1 reference clock pin, 1 transmit clock pin pair, 1 control pin pair, 16 data pin pairs, and 17 pins associated with power and ground.

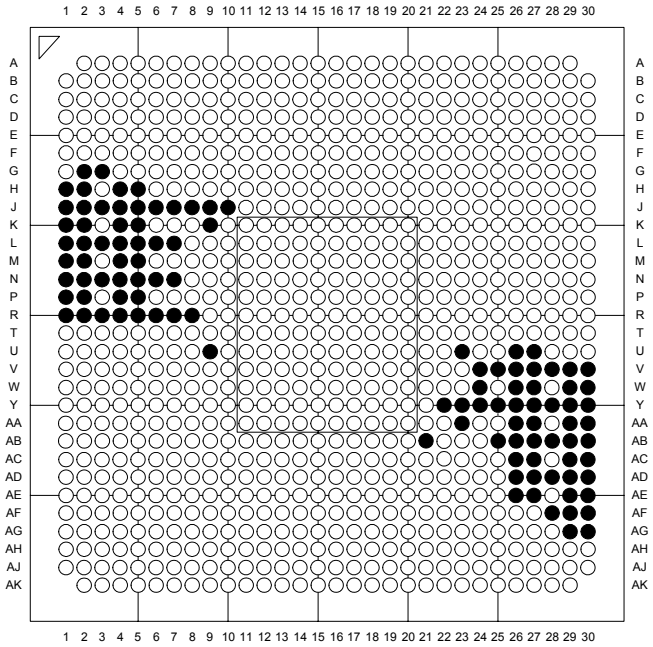
Table 5-1 TX General Characteristics

Characteristic	Description
Data Rate	SDR / DDR (programmable)
Supported Frequency	❋ 18.75 MHz – 500 MHz (DDR) ❋ 18.75 MHz – 640 MHz (SDR) See Chapter 8: Clock Characteristics for more information.
Signal Information	❋ 1.25 V (LVDS) ❋ Differential pairs, 100Ω impedance

External Pins

Table 5-2 describes the pins associated with the TX interface. For a list of all pins associated with the Arrix family FPOA, see Appendix A: External Pins.

Figure 5-1 Ball Pattern for TX (Top-down View)



NOTE: TX-related balls are shown in black.

Table 5-2 TX Pins

Pin Number	Signal	Type	Signal Type	Notes
Transmit Datapath 1				
K9	TPLL1_AVDD	PWR	Analog	Connect to Analog 2.5V See "PLL Power Characteristics" on page 74 for more information.
J10	TPLL1_AVSS	GND	Analog	Connect to Analog Ground See "PLL Power Characteristics" on page 74 for more information.
J8	TPLL1_CAP	I	Analog	Do not connect
J9	TPLL1_REF	I	LVCMOS	18.75 - 37.5Mhz reference clock input for Transmit PLL
N2	TX1_CLK1_N	O	LVDS	Transmit Clock
N3	TX1_CLK1_P	O	LVDS	Transmit Clock

Table 5-2 TX Pins (Continued)

Pin Number	Signal	Type	Signal Type	Notes
L5	TX1_CNTL_N	O	LVDS	Transmit Control bit
L6	TX1_CNTL_P	O	LVDS	Transmit Control bit
R3	TX1_DATA_0_N	O	LVDS	Transmit Data bit (LSB)
R2	TX1_DATA_0_P	O	LVDS	Transmit Data bit
R5	TX1_DATA_1_N	O	LVDS	Transmit Data bit
R6	TX1_DATA_1_P	O	LVDS	Transmit Data bit
P1	TX1_DATA_2_N	O	LVDS	Transmit Data bit
P2	TX1_DATA_2_P	O	LVDS	Transmit Data bit
P4	TX1_DATA_3_N	O	LVDS	Transmit Data bit
P5	TX1_DATA_3_P	O	LVDS	Transmit Data bit
N5	TX1_DATA_4_N	O	LVDS	Transmit Data bit
N6	TX1_DATA_4_P	O	LVDS	Transmit Data bit
M1	TX1_DATA_5_N	O	LVDS	Transmit Data bit
M2	TX1_DATA_5_P	O	LVDS	Transmit Data bit
M4	TX1_DATA_6_N	O	LVDS	Transmit Data bit
M5	TX1_DATA_6_P	O	LVDS	Transmit Data bit
L2	TX1_DATA_7_N	O	LVDS	Transmit Data bit
L3	TX1_DATA_7_P	O	LVDS	Transmit Data bit
K2	TX1_DATA_8_N	O	LVDS	Transmit Data bit
K1	TX1_DATA_8_P	O	LVDS	Transmit Data bit
K4	TX1_DATA_9_N	O	LVDS	Transmit Data bit
K5	TX1_DATA_9_P	O	LVDS	Transmit Data bit
J3	TX1_DATA_10_N	O	LVDS	Transmit Data bit
J2	TX1_DATA_10_P	O	LVDS	Transmit Data bit
J5	TX1_DATA_11_N	O	LVDS	Transmit Data bit
J6	TX1_DATA_11_P	O	LVDS	Transmit Data bit
H1	TX1_DATA_12_N	O	LVDS	Transmit Data bit
H2	TX1_DATA_12_P	O	LVDS	Transmit Data bit
H4	TX1_DATA_13_N	O	LVDS	Transmit Data bit
H5	TX1_DATA_13_P	O	LVDS	Transmit Data bit
G2	TX1_DATA_14_N	O	LVDS	Transmit Data bit

Table 5-2 TX Pins (Continued)

Pin Number	Signal	Type	Signal Type	Notes
G3	TX1_DATA_14_P	O	LVDS	Transmit Data bit
F1	TX1_DATA_15_N	O	LVDS	Transmit Data bit
F2	TX1_DATA_15_P	O	LVDS	Transmit Data bit (MSB)
G1	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
G4	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
J1	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
J4	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
J7	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
L1	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
L4	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
L7	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
N1	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
N4	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
N7	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R1	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R4	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R7	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R8	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
U09	TX1_VREF	I	1.2V Analog	LVDS TX1 Analog 1.2V common mode voltage reference
Transmit Datapath 2				
Y23	TPLL2_AVDD	PWR	Analog	Connect to Analog 2.5V See "PLL Power Characteristics" on page 74 for more information.
Y22	TPLL2_AVSS	GND	Analog	Connect to Analog Ground See "PLL Power Characteristics" on page 74 for more information.
AA23	TPLL2_CAP	I	Analog	Do not connect
AC21	TPLL2_REF	I	LVCMOS	18.75 - 37.5MHz reference clock input for Transmit PLL
W27	TX2_CLK1_N	O	LVDS	Transmit Clock
W26	TX2_CLK1_P	O	LVDS	Transmit Clock
AB29	TX2_CNTL_N	O	LVDS	Transmit Control bit

Table 5-2 TX Pins (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AB28	TX2_CNTL_P	O	LVDS	Transmit Control bit
U27	TX2_DATA_0_N	O	LVDS	Transmit Data bit (LSB)
U26	TX2_DATA_0_P	O	LVDS	Transmit Data bit
V28	TX2_DATA_1_N	O	LVDS	Transmit Data bit
V29	TX2_DATA_1_P	O	LVDS	Transmit Data bit
V26	TX2_DATA_2_N	O	LVDS	Transmit Data bit
V25	TX2_DATA_2_P	O	LVDS	Transmit Data bit
W30	TX2_DATA_3_N	O	LVDS	Transmit Data bit
W29	TX2_DATA_3_P	O	LVDS	Transmit Data bit
Y29	TX2_DATA_4_N	O	LVDS	Transmit Data bit
Y28	TX2_DATA_4_P	O	LVDS	Transmit Data bit
Y26	TX2_DATA_5_N	O	LVDS	Transmit Data bit
Y25	TX2_DATA_5_P	O	LVDS	Transmit Data bit
AA30	TX2_DATA_6_N	O	LVDS	Transmit Data bit
AA29	TX2_DATA_6_P	O	LVDS	Transmit Data bit
AA26	TX2_DATA_7_N	O	LVDS	Transmit Data bit
AA27	TX2_DATA_7_P	O	LVDS	Transmit Data bit
AB25	TX2_DATA_8_N	O	LVDS	Transmit Data bit
AB26	TX2_DATA_8_P	O	LVDS	Transmit Data bit
AC29	TX2_DATA_9_N	O	LVDS	Transmit Data bit
AC30	TX2_DATA_9_P	O	LVDS	Transmit Data bit
AC27	TX2_DATA_10_N	O	LVDS	Transmit Data bit
AC26	TX2_DATA_10_P	O	LVDS	Transmit Data bit
AD28	TX2_DATA_11_N	O	LVDS	Transmit Data bit
AD29	TX2_DATA_11_P	O	LVDS	Transmit Data bit
AE27	TX2_DATA_12_N	O	LVDS	Transmit Data bit
AE26	TX2_DATA_12_P	O	LVDS	Transmit Data bit
AE30	TX2_DATA_13_N	O	LVDS	Transmit Data bit
AE29	TX2_DATA_13_P	O	LVDS	Transmit Data bit
AF29	TX2_DATA_14_N	O	LVDS	Transmit Data bit
AF28	TX2_DATA_14_P	O	LVDS	Transmit Data bit

Table 5-2 TX Pins (Continued)

Pin Number	Signal	Type	Signal Type	Notes
AG30	TX2_DATA_15_N	O	LVDS	Transmit Data bit
AG29	TX2_DATA_15_P	O	LVDS	Transmit Data bit (MSB)
V24	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
V27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
V30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
W24	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
Y24	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
Y27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
Y30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AB27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AB30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AD26	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AD27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AD30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AF30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
U23	TX2_VREF	I	1.2V Analog	LVDS TX2 Analog 1.2V common mode voltage reference

Matched Lengths

Match length tolerance is 2/3 inch maximum for each group.

Group 1	Group 2
TX1_DATA_x	TX2_DATA_x
TX1_CLK1_x	TX2_CLK1_x
TX1_CNTL_x	TX2_CNTL_x

Termination

External termination is 100 Ω across the differential pairs at load.

Timing Characteristics

Figure 5-2 illustrates the timing characteristics in DDR mode when the clock is aligned with the data (i.e. in-phase). Note that these same timing parameters apply when using an inverted clock (though the clock is 180º offset).

Figure 5-2 TX DDR In-Phase Timing

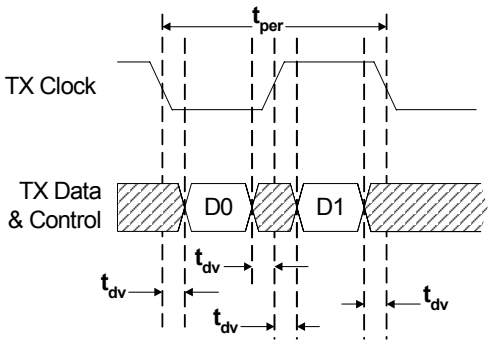


Figure 5-3 illustrates the timing characteristics in DDR mode when the clock is 90º phase-shifted with the data.

Figure 5-3 TX DDR 90º Phase-Shifted Timing

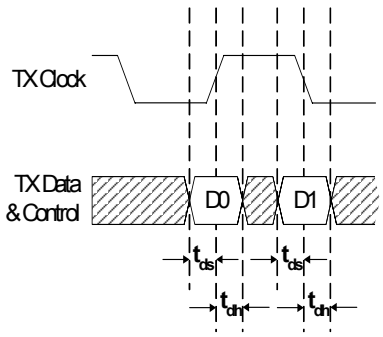


Figure 5-4 illustrates the timing characteristics in SDR mode when the clock is aligned with the data.

Figure 5-4 TX SDR In-Phase Timing

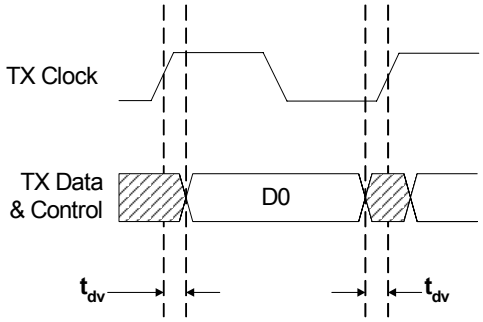


Figure 5-5 illustrates the timing characteristics in SDR mode when the clock is 90º phase-shifted with the data.

Figure 5-5 TX SDR 90º Phase-Shifted Timing

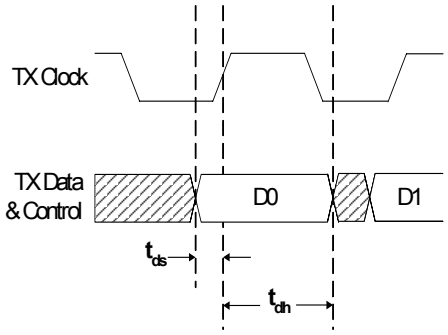


Table 5-3 TX Timing Characteristics

Parameter	Description	Min	Max
Input Timing			
t_{dv}	SDR/DDR Data Valid	-175 ps	175 ps
t_{ds}	SDR/DDR 90º Phase-Shifted Data Setup	t_{per}/4.5 - 175 ps	
t_{dh}	SDR/DDR 90º Phase-Shifted Data Hold		t_{per}/4.5 - 175 ps
Clock Timing[a]			
t_{per}	Clock Period	1.56 ns (640 MHz SDR) 2.0 ns (500 MHz DDR)	53.33 ns (18.75 MHz)
PLL Lock Time			15 µs

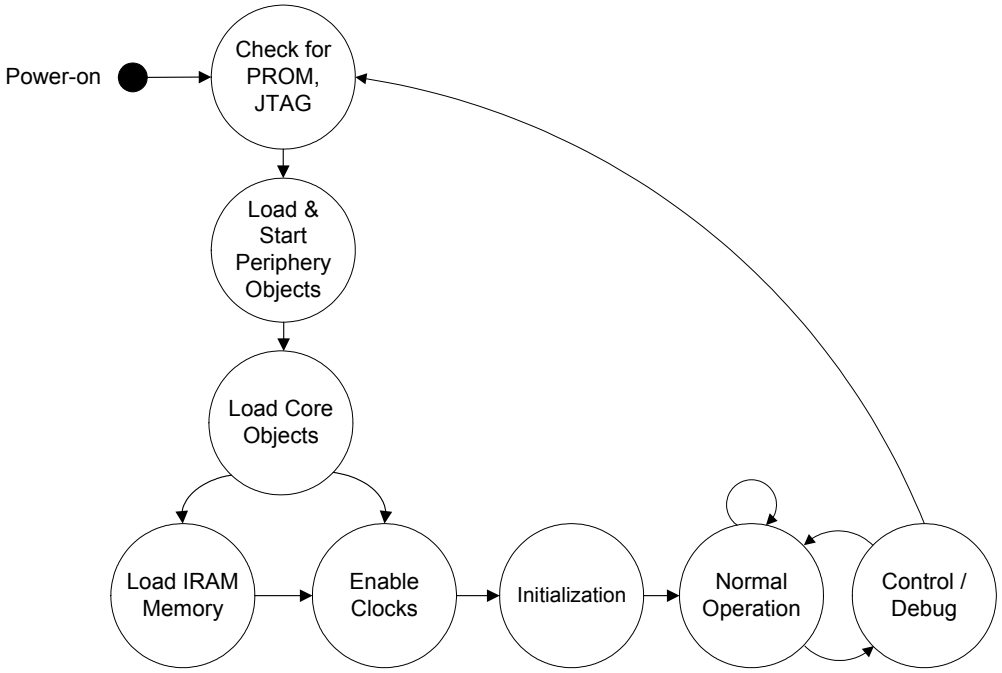
a. See Chapter 8: Clock Characteristics for additional clock information.

Chapter 6
Initialization and Control

Overview

Figure 6-1 illustrates the startup flow for the FPOA.

Figure 6-1 Startup Flow



At power-on, the PROM_DISABLE signal indicates whether a PROM is present. If deasserted, the PROM controller automatically accesses the PROM to acquire load information. If no PROM is present, the controller waits for configuration information via the JTAG controller.

The high-speed clock used in the FPOA is disabled while clocks operating at slower frequencies shift in configuration information via scan chains. (See "PROM Load Sequence" on page 65 for more information.) The periphery objects are loaded first, followed by the core objects. Note that the periphery objects start before normal operation.

After all objects are loaded (and the periphery objects are started), the clocks are enabled, chip registers initialize to their configured values, and the application begins running.

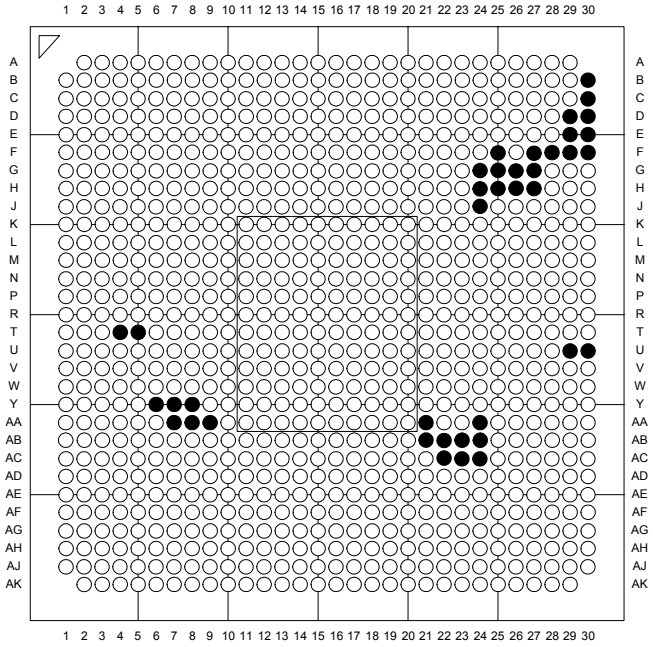
Significant current surges occur when the FPOA transitions from configuration load to initialization, and from initialization to normal operation. See "Current Fluctuations During Initialization" on page 75 for further detail.

During normal operation, the JTAG controller can assume control of the FPOA at any time. It can halt operation and observe the state of any of the objects within the FPOA. It can also reset the chip.

External Pins

Table 6-1 describes the pins associated with the PROM interface, the JTAG interface, the Core PLL, as well as other miscellaneous control pins. For a list of all pins associated with the Arrix family FPOA, see Appendix A: External Pins.

Figure 6-2 Ball Pattern for Init & Control (Top-down View)



NOTE: Initialization and Control balls are shown in black.

Table 6-1 Initialization and Control Pins

Pin Number	Signal	Type	Signal Type	Notes
PROM Interface				
G25	PROM_CEN	O	LVCMOS	PROM Chip Enable (low active)
G27	PROM_CLK	I	LVCMOS	PROM Clock Input
F29	PROM_CLKDIV	I	LVCMOS	PROM Clock Divider Input 0 = Divide by 2 1 = Divide by 4
F27	PROM_CLKO	O	LVCMOS	PROM Clock Output (PROM_CLK divided by 2 or 4, as specified by PROM_CLKDIV above)
E30	PROM_DATA_0	I	LVCMOS	PROM Data bit (LSB)
C30	PROM_DATA_1	I	LVCMOS	PROM Data bit
D29	PROM_DATA_2	I	LVCMOS	PROM Data bit
E29	PROM_DATA_3	I	LVCMOS	PROM Data bit
F28	PROM_DATA_4	I	LVCMOS	PROM Data bit
G26	PROM_DATA_5	I	LVCMOS	PROM Data bit
H26	PROM_DATA_6	I	LVCMOS	PROM Data bit
H27	PROM_DATA_7	I	LVCMOS	PROM Data bit (MSB)
H24	PROM_DISABLE	I	LVCMOS	PROM Disable Input
H25	PROM_OE	O	LVCMOS	PROM Output Enable
J24	PROM_SERIAL	I	LVCMOS	PROM Serial/Parallel mode select 0 = 8-bit connection 1 = 1-bit connection
B30	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
D30	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
F25	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
F30	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
G24	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
Core PLL				
AA8	CPLL_AVDD	PWR	Analog	Connect to Analog 2.5V See "PLL Power Characteristics" on page 74 for more information.
Y8	CPLL_AVSS	GND	Analog	Connect to Analog Ground See "PLL Power Characteristics" on page 74 for more information.

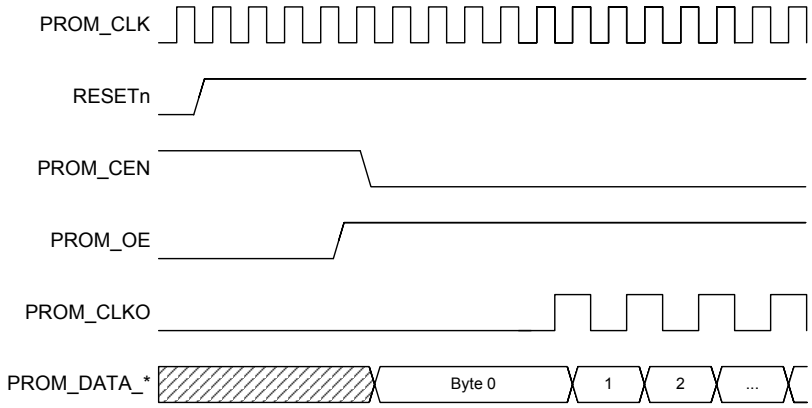
Table 6-1 Initialization and Control Pins (Continued)

Pin Number	Signal	Type	Signal Type	Notes
Y6	CPLL_CAP	I	Analog	Do not connect
AA9	CPLL_REF	I	LVCMOS	18.75 - 37.5 MHz reference clock input for Core PLL
Test & Reset				
AA7	CLOCK_N	I	LVDS	Core clock bypass input
Y7	CLOCK_P	I	LVDS	Core clock bypass input
AA21	JTAG_VDD_PST	PWR	2.5V	Connect to 2.5V
AB21	JTAG_VDD_PST	PWR	2.5V	Connect to 2.5V
AC22	RESETn	I	LVCMOS	FPOA Reset (low active)
AB24	TCLK	I	LVCMOS	JTAG Test Clock Input This input has a built-in pullup resistor.
AC23	TDI	I	LVCMOS	JTAG Test Data Input This input has a built-in pullup resistor.
AB23	TDO	O	LVCMOS	JTAG Test Data Output
AC24	TESTMODE	I	LVCMOS	Connect to ground This input has a built-in pulldown resistor.
AB22	TMS	I	LVCMOS	JTAG Test Mode Select This input has a built-in pullup resistor.
AA24	TRSTn	I	LVCMOS	JTAG Test Reset (low active) This input has a built-in pullup resistor.
T4	TX1_TEST_N	O	LVDS	Production test pin - do not connect
T5	TX1_TEST_P	O	LVDS	Production test pin - do not connect
U29	TX2_TEST_N	O	LVDS	Production test pin - do not connect
U30	TX2_TEST_P	O	LVDS	Production test pin - do not connect

PROM Load Sequence

Figure 6-3 illustrates the sequence of events that occurs during PROM load.

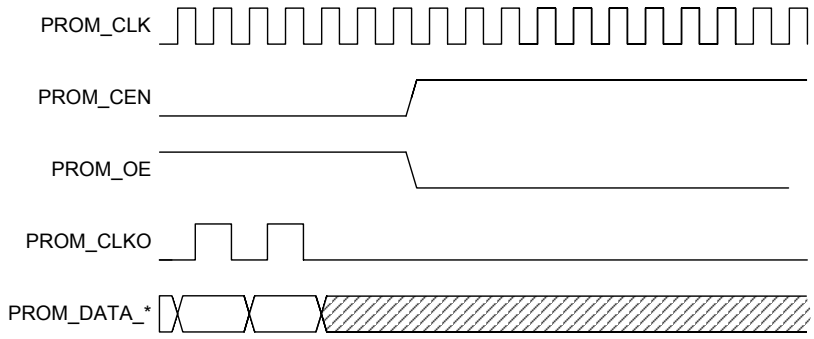
Figure 6-3 Start of PROM Load Sequence



The reset signal (RESETn) initiates the loading process. Reset forces the output enable signal (PROM_OE) low in order to initialize the PROM. The chip enable signal (PROM_CEN) goes active low and the output enable signal goes active high to enable the PROM device to be read. The PROM clock begins, causing the PROM to shift read data into the FPOA.

When the PROM controller detects that the load sequence is completed, the signals PROM_CEN and PROM_OE deactivate. Figure 6-4 illustrates this sequence. The controller then takes the FPOA through its final initialization stage and onto normal operation.

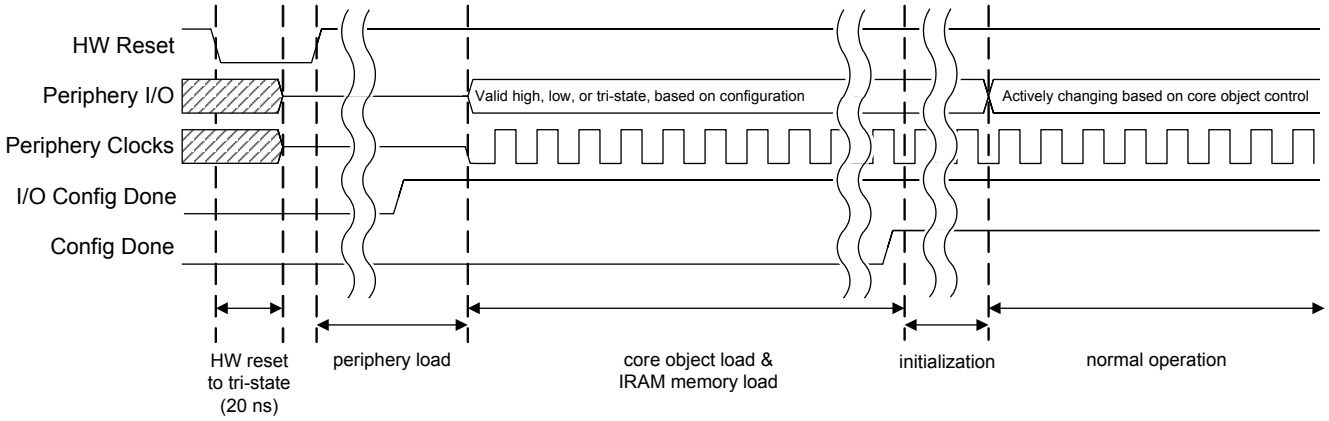
Figure 6-4 Completion of PROM Load Sequence



Initialization and Reset Sequence

Figure 6-5 illustrates the startup sequence after reset is signaled (RESETn, pin #AC22).

Figure 6-5 Reset Timing



Breakpoint Behavior

After a breakpoint is signaled (either via the JTAG interface or via the application), each periphery object behaves as described in Table 6-2. Once the chip is halted, it cannot resume.

Table 6-2 Breakpoint behavior

Periphery Object	Breakpoint behavior
XRAM	❋ The command FIFO is processed until it is empty. ❋ Read data is discarded. ❋ Refresh operations continue.
GPIO	❋ All GPIO bits enter tri-state.
RX	❋ Data reception continues and data is discarded.
TX	❋ Data transmission continues until the TX FIFO empties. Then, based on configuration: ❋ Last data value is retransmitted, or ❋ A configurable underflow pattern is transmitted.

Timing Considerations

Figure 6-6 illustrates the timing considerations for the JTAG interface.

Figure 6-6 JTAG Timing

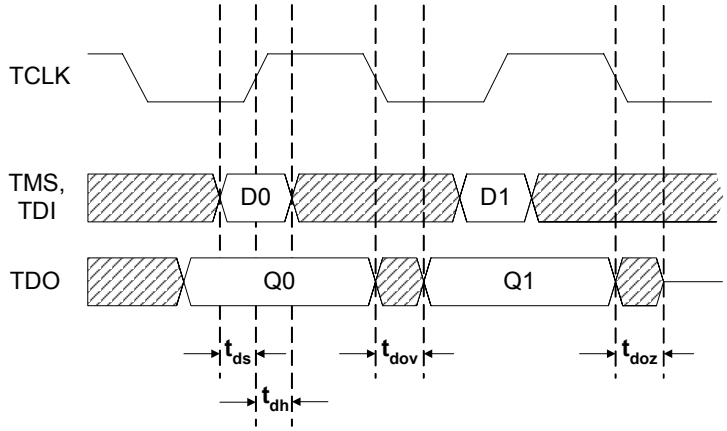


Figure 6-7 illustrates the setup and hold time for the PROM interface.

Figure 6-7 PROM Timing

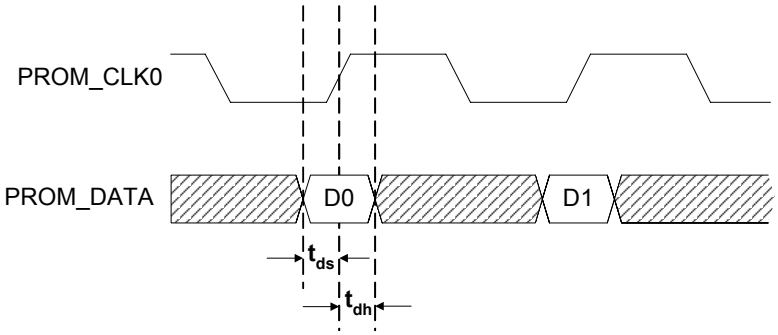


Table 6-3 JTAG & PROM Timing Characteristics

Parameter	Description	Min	Max
JTAG Timing			
t_{ds}	Data Setup		2.0 ns
t_{dh}	Data Hold		0.5 ns (12.0 ns[a])
t_{dov}	Data Output Valid	2.0 ns	5.5 ns
t_{doz}	Data Output Enter Tri-State	2.0 ns	5.5 ns
PROM Timing			
t_{ds}	Data Setup		5.5 ns
t_{dh}	Data Hold		0.0 ns

a. Hold on TDI for access to boundary scan chain only.

Supported JTAG and PROM Products

JTAG Products

- Macraigor Raven
- Macraigor usb2Sprite

PROM Products

Product Brand	Model Number	Frequency	Density	Configuration
Atmel	AT17LV010, AT17LV002, AT17LV040	12.5 MHz	1 MB, 2 MB, 4 MB	Serial
Xilinx	XC18V01, XC18V02, XC18V04	33 MHz	1 MB, 2 MB, 4 MB	Serial or Byte
Xilinx	XC17V01, XC17V02, XC17V04	33 MHz	1 MB, 2 MB, 4 MB	Serial or Byte

Chapter 7
Electrical Characteristics

Overview

This chapter describes the electrical characteristics of the Arrix family FPOA. Specifically, the following tables are included: "Power Supply Requirements" on page 69, "Absolute Minimum and Maximum Ratings" on page 71, "Operating Conditions" on page 72, and "External Pins" on page 77.

Power Supply Requirements

There are three main voltages that need to be supplied to the Arrix family FPOA: 1.2 V core voltage, 1.8 V RLDRAM voltage, and 2.5 V I/O voltage. All voltages have a ± 5% tolerance. In addition to the three main supply voltages, there are two reference voltages: 0.9 V for the two RLDRAM interfaces and 1.25 V for the two LVDS TX interfaces.

Table 7-1 Power Supply Requirements[a]

Voltage	Notes	Voltage Supply	Current / Power Load
VDD	Core supply (106 pins)	1.2 V ± 5%	35-40 A [b]
XRAM1_VDD_PST	XRAM HSTL (19 pins)	1.8 V ± 5%	740 mA
XRAM2_VDD_PST	XRAM HSTL (18 pins)	1.8 V ± 5%	740 mA
XRAM1_VREF	XRAM HSTL (3 pins)	XRAM1_VDD_PST / 2 ± 1%	100 µA
XRAM2_VREF	XRAM HSTL (3 pins)	XRAM1_VDD_PST / 2 ± 1%	100 µA
GPIO1_VDD_PST	2.5 v supply for GPIO 1 (12 pins)	2.5 V ± 5%	700 mA
GPIO2_VDD_PST	2.5 v supply for GPIO 2 (14 pins)	2.5 V ± 5%	700 mA
RX1_VDD_PST	LVDS (10 pins)	2.5 V ± 5%	100 mA

Table 7-1 Power Supply Requirements[a] (Continued)

Voltage	Notes	Voltage Supply	Current / Power Load
RX2_VDD_PST	LVDS (10 pins)	2.5 V ± 5%	100 mA
TX1_VDD_PST	LVDS (15 pins)	2.5 V ± 5%	340 mA
TX2_VDD_PST	LVDS (15 pins)	2.5 V ± 5%	340 mA
TX1_VREF	Sets common mode output voltage for TX1 driver	1.25 V ± 5%	100 µA
TX2_VREF	Sets common mode output voltage for TX2 driver	1.25 V ± 5%	100 µA
PROM_VDD_PST	PROM (5 pins)	2.5 V ± 5%	100 mA
JTAG_VDD_PST	JTAG (2 pins)	2.5 V ± 5%	80 mA
TPLL1_AVDD TPLL1_AVSS	Analog (2 pins)	2.5 V ± 5%	6 mA
TPLL2_AVDD TPLL2_AVSS	Analog (2 pins)	2.5 V ± 5%	6 mA
CPLL_AVDD CPLL_AVSS	Core PLL analog supply	2.5 V ± 5%	6 mA

a. These values are based on pre-silicon estimates. They will be updated once tested with real silicon.
b. A large design running at 1 GHz and using every object in the FPOA could in theory draw as much as 50A of core power. In practice, typical designs running at 1GHz tend to max out at 40A. The max amperage decreases with relationship to the number of objects used and at lower core clock frequencies. A design using less than two-thirds of the FPOA objects running at 800 Mhz should not exceed 30A.

Absolute Minimum and Maximum Ratings

Table 7-2 Absolute Minimum and Maximum Ratings

Parameter	Description	Min	Max
T_J	Junction Temperature	-40º C	+125º C[a]
T_S	Storage Temperature	-65º C	150º C
V_{DD}	Core Supply Voltage	-0.3 V	+1.68 V
V_{DD} LVCMOS	LVCMOS I/O Supply Voltage	-0.3 V	+3.5 V
V_{DD} HSTL	HSTL I/O Supply Voltage	-0.3 V	+2.75 V
V_{DD} LVDS	LVDS I/O	-0.3 V	+3.5 V
V_{DD} PLL	PLL Analog Supply Voltage	-0.3 V	+3.5 V
Note: Long-term exposure to absolute ratings may affect device reliability and permanent damage may occur if ratings are exceeded. The device should be operated under recommended operating conditions.			

a. Operating life at various frequencies and temperatures:
1 GHz @ 125º C = 4.0 years
1 GHz @ 85º C = 11.4 years
800 MHz @ 125º C = 6.25 years

Operating Conditions

The input waveform illustrated in Figure 7-1 is used for some of the operating conditions specified in Table 7-3:

Figure 7-1 Input Waveform

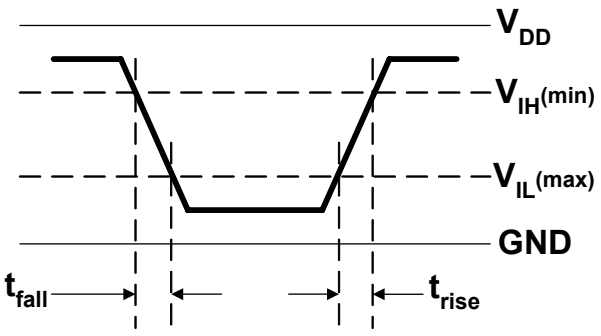


Table 7-3 Operating Conditions

Parameter	Description	Min	Nom	Max
Temperature				
T_J	Junction Temperature[a]	-40° C		125° C
Core Supply				
V_{DD}	Core Supply Voltage	1.14 V	1.2 V	1.26 V
I_{VDD}	V_{DD} Supply Current	Application dependent.		
LVCMOS I/O	**GPIO, PROM, JTAG, PLL Reference Clock[b]**			
V_{DD}	I/O Supply Voltage	2.375 V	2.5 V	2.625 V
V_{IL}	Input Low Voltage	-0.3 V		0.7 V
V_{IH}	Input High Voltage	1.7 V		3.6 V
V_{OL}	Output Low voltage			0.7 V
V_{OH}	Output High voltage	1.7 V		
I_I	Input leakage current @VI=V_{DD} or 0V			± 10 µA
I_{OZ}	Tri-state output leakage current @Vo=V_{DD} or 0V			± 10 µA
I_{OL} for 8mA drivers	Low level output current	10.8 mA	18.3 mA	26.3 mA
I_{OH} for 8mA drivers	High level output current	11.5 mA	22.8 mA	37.0 mA
I_{OL} for 16mA GPIO clock drivers	Low level output current	21.7 mA	36.6 mA	52.5 mA
I_{OH} for 16mA GPIO clock drivers	High level output current	22.9 mA	45.7 mA	73.9 mA
C_O	I/O Capacitance			3.9 pF
HSTL I/O	**XRAM Hardware[b]**			
V_{DD}	I/O Supply Voltage	1.71 V	1.8 V	1.89 V
V_{REF}	Threshold point	0.855 V	0.9 V	0.945 V
V_{IL}	Input Low Voltage			V_{REF} - 0.20 V
V_{IH}	Input High Voltage	V_{REF} + 0.20 V		

Table 7-3 Operating Conditions (Continued)

Parameter	Description	Min	Nom	Max
t_{rise}	Output Rise Time	550 ps	750 ps	850 ps
t_{fall}	Output Fall Time	500 ps	750 ps	900 ps
V_{OL}	Output low voltage			V_{REF} - 0.40 V
V_{OH}	Output high voltage	V_{REF} + 0.40 V		
I_{OL}	Low level output current	8 mA		
I_{OH}	High level output current	-8 mA		
C_O	I/O Capacitance			3.7 pF
LVDS I/O	**RX Hardware**[b]			
V_{DD}	I/O Supply Voltage	2.375 V	2.5 V	2.625 V
V_{IL}	Differential Input Low Voltage	-0.100 V		
V_{IH}	Differential Input High Voltage	0.100 V		
R_{IN}	Differential Input Impedance	80 Ω	100 Ω	120 Ω
C_O	I/O Capacitance			2.5 pF
LVDS I/O	**TX Hardware**[b]			
V_{DD}	I/O Supply Voltage	2.375 V	2.5 V	2.625 V
t_{rise}	Output Rise Time	100 ps		300 ps
t_{fall}	Output Fall Time	100 ps		300 ps
V_{COM}	Common Mode Voltage	1.125 V	1.25 V	1.275 V
V_{OD}	Output Differential Voltage	± 250 mV	± 350 mV	± 400 mV
I_O	Output Current	± 2.0 mA	± 3.5 mA	± 5.0 mA
C_O	I/O Capacitance			2.2 pF
PLL/DLL Analog Supply				
V_{AVDD}	PLL/DLL Analog Supply Voltage	2.25 V	2.5 V	2.75 V
I_{AVDD}	V_{AVDD} Supply Current		4 mA	6 mA

a. See Chapter 9: Thermal Considerations.
b. Values are specified per pin.

PLL Power Characteristics

- CORE_PLL_AVDD – Isolate 2.5 volts through filter choke. Decouple with 1μF capacitor to AGND.
- TPLL1_VDD – Isolate 2.5 volts through filter choke. Decouple with 1μF capacitor to AGND.
- TPLL2_AVDD – Isolate 2.5 volts through filter choke. Decouple with 1μF capacitor to AGND.

Power Sequencing

The power supplies should be sequenced so the 2.5 volt supply (including the analog PLL supplies) comes up first, then the 1.8 volt supply, followed by the 1.2 volt supply.

The 2.5 volt supply should lead the 1.8 volt supply by a minimum of 700 mv rise. The 1.8 volt supply should lead the 1.2 volt supply by a minimum of 700 mv rise.

TX_VREF should come up after the 2.5 volt supply. XRAM_VREF should come up after the 1.8 volt supply.

Power-up Reset

FPOA Reset should be held active during a power-up until all voltages and clocks are stable plus a minimum of 32 PROM clock (PROM_CLK) cycles.

Decoupling Capacitors

Recommended for the FPOA:

- 1.2 V supply
  - Cap. 220µF Tantilum - QTY 10 (min)
  - Cap. 10µF Ceramic - QTY 10 (min)
  - Cap. 0.10µF Ceramic - QTY 40 (min)
  - Cap. 0.01µF Ceramic - QTY 40 (min)
- 1.8 V supply
  - Cap. 220µF Tantilum - QTY 6 (min)
  - Cap. 10µF Ceramic - QTY 6 (min)
  - Cap. 0.10µF Ceramic - QTY 20 (min)
  - Cap. 0.01µF Ceramic - QTY 20 (min)
- 2.5 V supply
  - Cap. 220µF Tantilum - QTY 6 (min)
  - Cap. 10µF Ceramic - QTY 6 (min)
  - Cap. 0.10µF Ceramic - QTY 20 (min)
  - Cap. 0.01µF Ceramic - QTY 20 (min)

Place 0.10µF and 0.01µF capacitors as close as possible around the FPOA, intermixing the different voltages.

Current Fluctuations During Initialization

After JTAG or PROM load of the FPOA, the clocks are enabled. However, communication registers are held at initial values. The core supply current will instantaneously jump a certain amount during this period (I_2 amps, as specified in Table 7-4). The supply voltage (measured at the chip pin) must not drop more than 20% below nominal.

After a configurable number of clock cycles (t_{id} PROM clocks, as specified in Table 7-4), communication registers are released and the chip will start running. The core supply current will increase further (I_3 amps, as specified in Table 7-4). At this point, the supply voltage must not drop more than 5% below nominal.

Figure 7-2 Current Surge at Startup

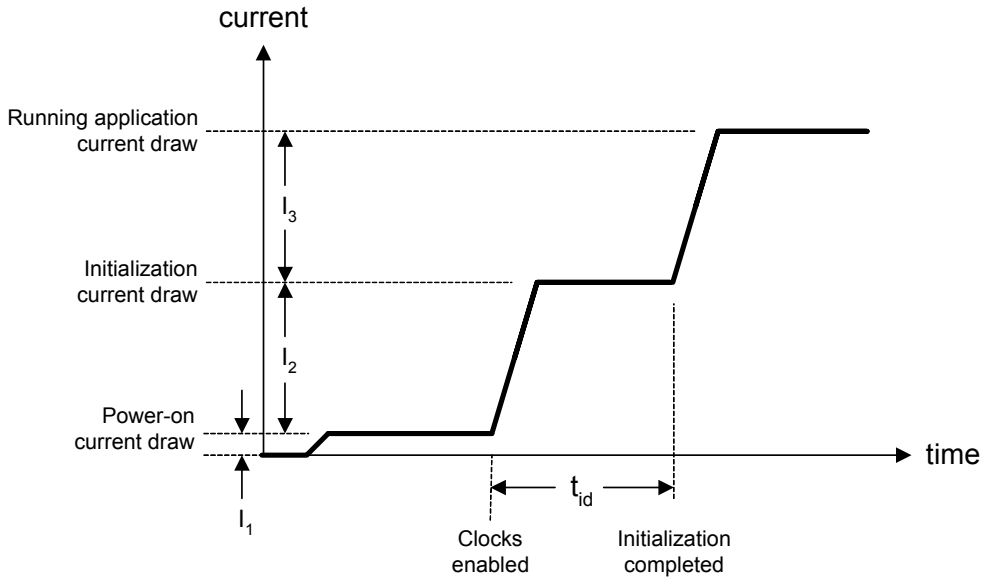


Table 7-4 Current Surge Values

Parameter	Description	Min	Max
I_1	Power-on current draw[a]	1.0 amps	3.0 amps
I_2	Initialization current draw[b]	1.0 amps	25.0 amps
I_3	Application current draw[c]	0.55 amps	14 amps
t_{id}	Initialization Duration	When loading from the PROM, this is a 16-bit value which specifies the number of PROM clocks. This value can be set via a configuration parameter when running the OC (Object Compiler) software.	

a. Power-on includes enabling of the PLLs.
b. The initialization current surge is dependent on clock frequency and number of objects used by the application.
c. The application start up current surge is dependent on clock frequency and application data activity.

External Pins

Table 7-5 describes the pins associated with core power and core I/O ground. I/O power pins are documented with their corresponding periphery object. For a list of all pins associated with the Arrix family FPOA, see Appendix A: External Pins.

Table 7-5 Voltage and Ground Pins

Pin Number	Signal	Type	Signal Type	Notes
Core VDD				
See below	VDD	PWR	1.2v	Core power supply
The following pins should be connected to the core power supply: H18, H20, H22, J11, J13, J17, J19, J21, J23, K10, K12, K14, K16, K18, K20, K22, L9, L11, L13, L15, L17, L19, L21, L23, L24, M8, M10, M12, M14, M16, M18, M20, M22, N9, N11, N13, N15, N17, N19, N21, N23, N24, P8, P10, P12, P14, P16, P18, P20, P22, R11, R13, R15, R17, R19, R21, T10, T12, T14, T16, T18, T20, U11, U13, U15, U17, U19, U21, V7, V8, V9, V10, V12, V14, V16, V18, V20, V22, W7, W8, W9, W11, W13, W15, W17, W19, W21, W23, Y10, Y12, Y14, Y16, Y18, Y20, AA11, AA13, AA15, AA17, AA19, AB12, AB14, AB16, AB18, AB20, AC17, AC19.				
Core & I/O VSS				
See below	VSS	GND	0V	Core and I/O ground
The following pins should be connected to ground: B2, B4, B6, B8, B10, B13, B14, B16, B18, B20, B22, B24, B26, B28, D2, D12, D28, F3, F5, F7, F9, F11, F13, F15, F17, F19, F21, F23, G13, G28, H3, H6, H13, H17, H19, H21, H23, J12, J14, J20, J22, J25, J28, K3, K6, K7, K11, K13, K15, K17, K19, K21, K23, L8, L10, L12, L14, L16, L18, L20, L22, L25, L28, M3, M6, M7, M9, M11, M13, M15, M17, M19, M21, M23, N8, N10, N12, N14, N16, N18, N20, N22, N25, N28, P3, P6, P7, P9, P11, P13, P15, P17, P19, P21, P23, R10, R12, R14, R16, R18, R20, R25, R28, T3, T6, T7, T11, T13, T15, T17, T19, T21, T23, T24, U10, U12, U14, U16, U18, U20, U25, U28, V3, V6, V11, V13, V15, V17, V19, V21, V23, W10, W12, W14, W16, W18, W20, W25, W28, Y3, Y11, Y13, Y15, Y17, Y19, Y21, AA10, AA12, AA14, AA16, AA18, AA20, AA22, AA25, AA28, AB3, AB6, AB11, AB13, AB15, AB17, AB19, AC5, AC6, AC12, AC14, AC16, AC20, AC28, AD3, AD11, AE5, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE25, AE28, AF3, AG12, AG28, AJ4, AJ6, AJ8, AJ10, AJ16, AJ18, AJ20, AJ22, AJ24, AJ26, AJ28, AK12.				

Chapter 8
Clock Characteristics

Core Reference Clock Characteristics

Table 8-1 Core Reference Clock Characteristics

Characteristic	Description
Reference Clock Frequency Range	18.75 MHz – 37.5 MHz
Reference Clock Duty Cycle	20 / 80
Reference Clock Jitter	± 200 ps
Reference Clock Impedance & Termination	50 Ω single-ended impedance. No termination.
Reference Clock Routing	Route as clock signal. Ensure proper spacing away from all other signals.
Output Clock Multiplier Values	1, 2, 4, 8, 16, 32
Output Clock Frequency Range	18.75 MHz – 1 GHz
PLL Lock Time	15 µs

XRAM Clock Characteristics

Table 8-2 XRAM Clock Characteristics

Characteristic	Description
Clock Frequency Range	175 MHz – 266 MHz
Duty Cycle	47 / 53
Jitter	± 5%
Impedance & Termination	50 Ω single-ended trace impedance. 50 Ω termination to VTT.
Routing	Route clock P/N signal pair as a differential route.

GPIO Clock Characteristics

The GPIO interface can use either an externally-supplied clock (Table 8-3), or it can use the core clock (Table 8-4).

Table 8-3 GPIO Externally-Supplied Clock Characteristics

Characteristic	Description
Clock Frequency Range	0 – 100 MHz
Duty Cycle	40 / 60
Jitter	± 5%
Impedance & Termination	50 Ω single-ended impedance. No termination.

Table 8-4 GPIO Internally-Supplied Clock Characteristics

Characteristic	Description
Input Clock	Core clock
Clock Divisor Values	3 – 511
Output Clock Frequency Range	0 – 100 MHz
Output Duty Cycle	45 / 55
Jitter	± 5%
Impedance & Termination	50 Ω single-ended impedance. No termination.
Other	Note that there is a 16mA drive for the GPIO clock.

RX Clock Characteristics

Table 8-5 RX Clock Characteristics

Characteristic	Description
Clock Frequency Range	116 MHz – 500 MHz (DDR) 116 MHz – 640 MHz (SDR)
Duty Cycle	47 / 53
Input Jitter	± 2%
Impedance & Termination	100 Ω differential impedance. 100 Ω termination built in to the receiver (termination variation is 80 - 120 Ω).

TX Clock Characteristics

Table 8-6 TX Clock Characteristics

Characteristic	Description
Reference Clock Frequency Range	18.75 MHz – 37.5 MHz
Reference Clock Duty Cycle	20 / 80
Reference Clock Jitter	± 200 ps
Reference Clock Impedance & Termination	50 Ω single-ended impedance. No termination.
Output Clock Multiplier Values	1, 2, 4, 8, 16, 32
Output Clock Frequency Range	18.75 MHz – 500 MHz (DDR) 18.75 MHz – 640 MHz (SDR)
Output Clock Duty Cycle	For PLL multiplier value of 32 – 45 / 55. For all other PLL values – 48 / 52.
Output Clock Jitter	± 50 ps
Output Clock Impedance & Termination	100 Ω differential impedance. 100 Ω termination between P/N signal pairs.
PLL Lock Time	15 µs

PROM Clock Characteristics

Table 8-7 PROM Clock Characteristics

Characteristic	Description
Clock Frequency Range	0 – 100 MHz
Duty Cycle	40 / 60
Jitter	± 5%
Impedance & Termination	50 Ω single-ended impedance. No termination.

Chapter 9
Thermal Considerations

General Considerations

- A heat sink and fan should be selected according to the expected power of the 1.2 V core voltage.
- Power will depend on the core clock speed and the number of objects used in the design.
- For maximum power, select a heat sink with a 45 º C/watt rating.
- For a list of recommended heat sinks, see Appendix B: Recommended Heat Sinks.

Junction Temperature

The Arrix family FPOA is rated for a junction temperature (T_J) between -40° C and 125° C. In order to keep the junction temperature in this range, a system design may need to incorporate air flow and/or a heat sink on the device. The type of heat sink required is dependent on many system parameters including the expected power dissipation of the application once it is programmed into the Arrix family FPOA.

Definition of Terms

When designed into a system, the Arrix family FPOA may or may not need additional thermal enhancements in the form of a passive or active heat sink. The performance and type of heat sink needed (if one is needed) is determined by several operating parameters. These are defined below.

- T_J: The junction temperature of the semiconductor device, as measured on the die. Measured in °C.
- T_C: The case temperature as measured on the top of the package. Measured in °C.
- T_A: The ambient temperature of the air immediately above the package and heat sink. Measured in °C.
- θ_{JC}: The thermal resistance between the junction and the case/package of the device. Measured in °C/Watt.
- θ_{CS}: The thermal resistance of the adhesive between the case/package and the heat sink. Measured in °C/Watt.
- θ_{SA}: The thermal resistance between the heat sink and the ambient air. Measured in °C/Watt.
- θ_{JA}: The thermal resistance between the device junction and the ambient air. $\theta_{JA}=\theta_{JC}+\theta_{CS}+\theta_{SA}$. Measured in °C/Watt.
- Air Flow: The air flow in the system, usually measured in linear feet per minute (LFM) or meters per second (m/s).
- P: The power dissipation of the device. Measured in Watts.

Thermal resistance θ is a measure of how well heat transfers between two entities. A lower value means better heat transfer.

Forced Convection

There are two system conditions for which a heat sink may be required. natural convection (also called still air) and forced convection (by using either an active heat sink or system fan). The calculation for a forced convection heat sink is the most straightforward and will be covered first.

q_{JA} is the main parameter that will define which heat sink should be used. The equation that determines the required θ_{JA} for a heat sink in a forced convection environment is as follows:

$$\theta_{JA} = (T_J - T_A) / P$$

θ_{JA} can be calculated depending on the power that needs to be dissipated, the ambient temperature in the system, and the desired junction temperature. The θ_{SA} for the heat sink itself can then be calculated from the following equation:

$$\theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS}$$

For example: Assume an FPOA application that dissipates 25 watts in a system that has an ambient temperature of 40° C. The junction temperature for the FPOA is desired to be 85° C. Calculating θ_{JA} for this scenario:

$$\theta_{JA} = (85 - 40) / 25 = 1.8 \text{ °C/watt}$$

And further calculating θ_{SA}:

$$\theta_{SA} = 1.8 - 0.45 - 0.1 = 1.35 \text{ °C/watt}$$

Using this value, one can find various heat sinks that meet this thermal performance requirement (a heat sink's θ_{SA} must be equal to or less than the calculated value) at different air flow rates. In this example, the ThermaFlo EH1126 is rated at 0.73 in an air flow of 250 LFM. Since 0.73 is less than the desired 1.35, this heat sink will achieve the desired thermal performance.

If the T_J, T_A, and power consumption are known, the list of heat sinks in Appendix B can be used to reference heat sink options for that specific design.

Natural Convection

Natural convection occurs when there is no externally induced air flow and heat transfer relies solely on the free buoyant flow of air surrounding the heat sink. Natural convection is often a very demanding system design challenge and is usually interesting when the overall power consumption of the system is low and/or the desired noise output of the system is low.

The equation that determines the required θ_{JA} for a heat sink in a natural convection environment is more complicated because the ambient temperature is also a function of the device power. This means a non-linear equation must be solved in order to arrive at the desired value of θ_{JA}. This calculation is started by going to the heat sink vendor's web

site and looking up that heat sink's specifications for temperature rise in °C versus heat dissipated in watts. This is often shown in a graphical format. Once the temperature rise is determined, this must be added to the ambient temperature in the equations to determine the desired θ_{JA}. After this, the calculation is similar to the forced air example.

For example: Assume an FPOA application that dissipates 20 watts in a system and has a still-air ambient temperature of 40 °C. For this example, assume the allowable junction temperature for the FPOA is 115 °C. At this point, a speculative heat sink must be selected so the ambient temperature rise can be determined as a function of the power. In this case, a ThermaFlo E3180 is chosen and by looking at the temperature rise versus power chart, a 24 °C value is found for 20 Watts dissipated. This is added to the ambient temperature and θ_{JA} is calculated. For this scenario:

$$\theta_{JA} = (115 - (40 + 24)) / 20 = 2.55 \text{ °C/Watt}$$

And further calculating θ_{SA}:

$$\theta_{SA} = 2.55 - 0.45 - 0.1 = 1.8 \text{ °C/Watt}$$

Checking the ThermaFlo heat sink's rated θ_{SA} for 20 watts, we find a value of 1.35 °C/watt. Since this value is lower (better) than 1.8, we know this heat sink will work in this example.

Natural convection is a difficult system environment in which to design. Since the heat dissipation performance of the heat sink is a function of the heat sink surface area, often a very large and heavy heat sink is required. Many times, the trade-off of adding a system fan, even with the added expense, is much more cost-effective than the natural convection approach.

If the T_J, T_A, and power consumption are known, the list of heat sinks in Appendix B can be used to reference heat sink options for that specific design.

Chapter 10
Packaging Information

Overview

The Arrix product family package is an 896-pin high-performance Flip-Chip Ball Grid Array (HFCBGA). This package provides a large number of solder-ball interconnects and excellent thermal characteristics with a top-mounted heat spreader.

Package Dimensions

The following diagrams detail the dimensions of the Arrix product family FPOA. Values for each symbol are specified in Table 10-1 on page 89.

Figure 10-1 Package Dimensions – Top View

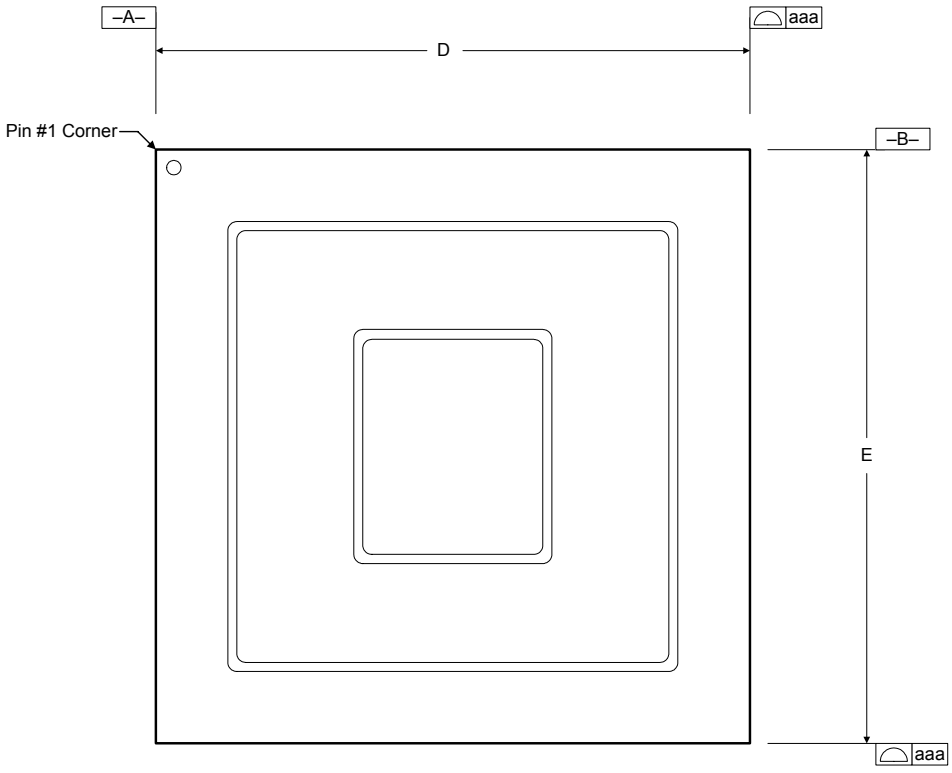


Figure 10-2 Package Dimensions – Side View

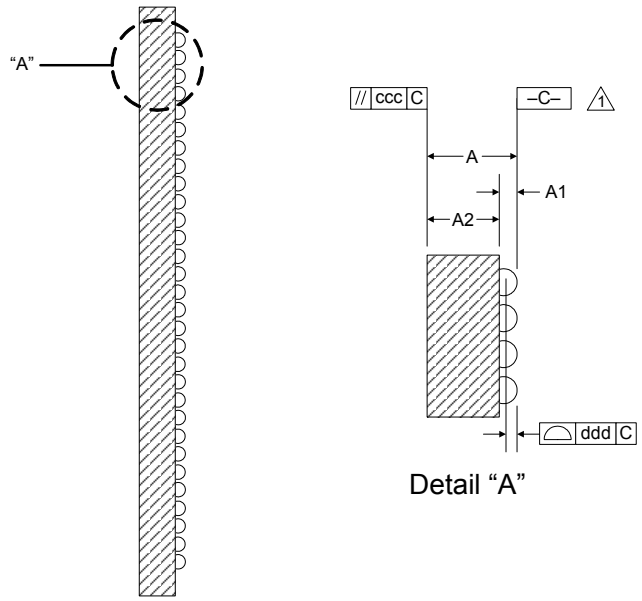
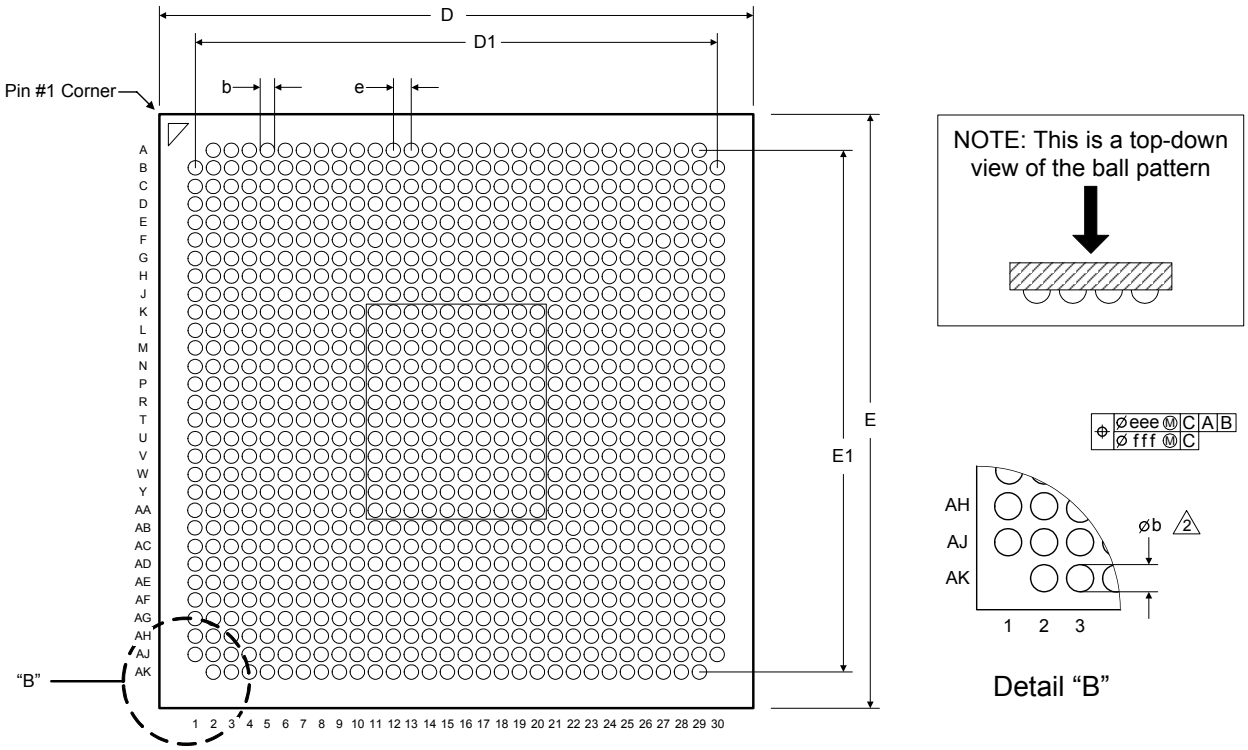


Figure 10-3 Package Dimensions – Bottom View



NOTES:

1. Primary Datum C and seating plane are defined by the spherical crowns of the solder balls.
2. Dimension b is measured at the maximum solder ball diameter, parallel to primary Datum C.
3. There should be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.
4. The tilt of the heat sink should be within 0.254 mm (vertical position).

Table 10-1 Package Dimensions

Symbol	Description	Dimensions in millimeters		
		Min	Nom	Max
A	Distance from the seating plane to the highest point of the package.	2.60	3.00	3.40
A1	Ball height.	0.40	0.50	0.60
A2	Thickness of the package body, exclusive of the ball height.	2.20	2.50	2.80
D	Length of the body measured at the outermost extremes.	30.80	31.00	31.20
D1	Distance between centerlines of the first and last ball on the long axis of the package.	---	29.00	---
E	Width of the body measured at the outermost extremes.	30.80	31.00	31.20
E1	Distance between centerlines of the first and last ball on the short axis of the package.	---	29.00	---
b	Diameter of a single ball.	0.50	0.60	0.70
e	Centerline to centerline spacing of the ball.	---	1.00	---
aaa	Bilateral profile tolerance zone that controls the size and orientation of the sides of the carrier body.	---	0.20	---
ccc	Bilateral tolerance zone for parallelism of the lid surface with respect to the seating plane (Datum C).	---	0.25	---
ddd	Unidirectional profile tolerance zone that extends upward from the seating plane (Datum C).	---	0.20	---
eee	Tolerance of position that controls the matrix pattern of balls as a whole with respect to Datums A and B.	---	0.30	---
fff	Tolerance of position that controls the relationship of the balls with respect to each other within the pattern.	---	0.10	---

Ball Pattern

The FPOA ball pattern is a 30 x 30 array of balls. For a description of each pin sorted by ball position, see Appendix A: External Pins. For a description of each pin associated with its respective component, refer to the following chapters:

- Chapter 2: XRAM Hardware
  This chapter describes all pins associated with the XRAM controller.
- Chapter 3: GPIO Hardware
  This chapter describes all pins associated with the GPIO interface.
- Chapter 4: RX Hardware
  This chapter describes all pins associated with the RX interface.
- Chapter 5: TX Hardware
  This chapter describes all pins associated with the TX interface.
- Chapter 6: Initialization and Control
  This chapter describes all pins associated with the initialization and control periphery objects (JTAG interface, PROM interface, PLL, Debug, etc.).
- Chapter 7: Electrical Characteristics
  This chapter describes all pins associated with power and ground.

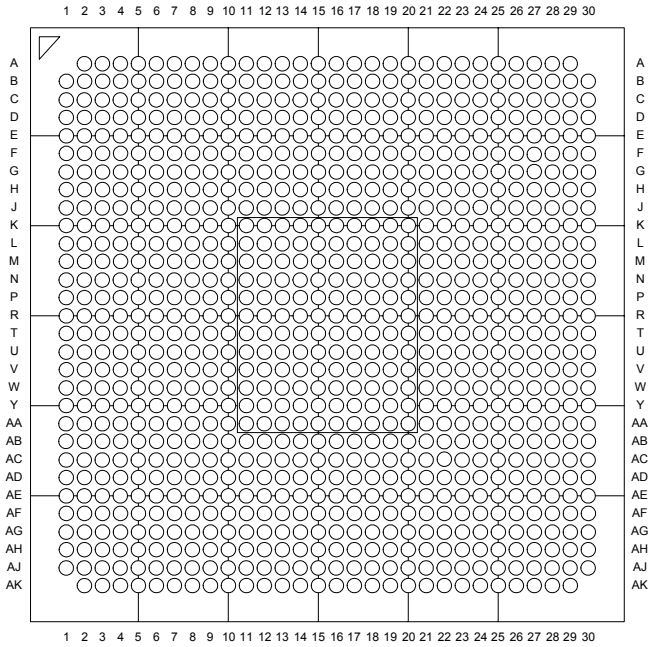
Recommended PC Board Characteristics

Characteristic	Value
Layers	12
Signal Layers	6
1.2 volt power supplies	1
1.8 volt power supplies	1
2.5 volt power supplies	1
Ground Layers	2
Analog Ground Layers	1
Impedance Characteristics	❋ Single ended: 50 Ω ❋ Differential pairs: 100 Ω

Appendix A: External Pins

This chapter describes each pin (sorted by ball position) on the Arrix family FPOA shown in Figure 11-1.

Figure 11-1 Ball Pattern for FPOA (Top-down View)



For a description of each pin sorted by hardware type, refer to the chapter for that particular hardware.

Table 11-1 External Pins

Pin Number	Signal	Type	Signal Type	Description
A01	None	N/A	N/A	No ball
A02	GPIO1_15	I/O	LVCMOS	GPIO data bit
A03	GPIO1_18	I/O	LVCMOS	GPIO data bit
A04	GPIO1_23	I/O	LVCMOS	GPIO data bit
A05	GPIO1_29	I/O	LVCMOS	GPIO data bit
A06	GPIO1_28	I/O	LVCMOS	GPIO data bit
A07	GPIO1_36	I/O	LVCMOS	GPIO data bit
A08	GPIO1_35	I/O	LVCMOS	GPIO data bit
A09	GPIO1_38	I/O	LVCMOS	GPIO data bit
A10	GPIO1_42	I/O	LVCMOS	GPIO data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
A11	GPIO1_46	I/O	LVCMOS	GPIO data bit
A12	XRAM1_DQS2_P	I	HSTL	XRAM Differential Input strobe (bits 18-26)
A13	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
A14	XRAM1_DATA_0	I/O	HSTL	XRAM Data bit (LSB)
A15	XRAM1_DATA_5	I/O	HSTL	XRAM Data bit
A16	XRAM1_DATA_11	I/O	HSTL	XRAM Data bit
A17	XRAM1_DATA_13	I/O	HSTL	XRAM Data bit
A18	XRAM1_DATA_19	I/O	HSTL	XRAM Data bit
A19	XRAM1_DATA_20	I/O	HSTL	XRAM Data bit
A20	XRAM1_DATA_24	I/O	HSTL	XRAM Data bit
A21	XRAM1_DATA_27	I/O	HSTL	XRAM Data bit
A22	XRAM1_DATA_28	I/O	HSTL	XRAM Data bit
A23	XRAM1_CNTL_0	O	HSTL	XRAM Control bit
A24	XRAM1_ADDR_0	O	HSTL	XRAM Address bit (LSB)
A25	XRAM1_ADDR_2	O	HSTL	XRAM Address bit
A26	XRAM1_ADDR_6	O	HSTL	XRAM Address bit
A27	XRAM1_ADDR_9	O	HSTL	XRAM Address bit
A28	XRAM1_ADDR_12	O	HSTL	XRAM Address bit
A29	XRAM1_ADDR_20	O	HSTL	XRAM Address bit (MSB)
A30	None	N/A	N/A	No ball
B01	GPIO1_14	I/O	LVCMOS	GPIO data bit
B02	VSS	GND	0V	Core and I/O ground
B03	GPIO1_17	I/O	LVCMOS	GPIO data bit
B04	VSS	GND	0V	Core and I/O ground
B05	GPIO1_22	I/O	LVCMOS	GPIO data bit
B06	VSS	GND	0V	Core and I/O ground
B07	GPIO1_30	I/O	LVCMOS	GPIO data bit
B08	VSS	GND	0V	Core and I/O ground
B09	GPIO1_37	I/O	LVCMOS	GPIO data bit
B10	VSS	GND	0V	Core and I/O ground
B11	GPIO1_47	I/O	LVCMOS	GPIO data bit
B12	XRAM1_DQS2_N	I	HSTL	XRAM Differential Input strobe (bits 18-26)
B13	VSS	GND	0V	Core and I/O ground

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
B14	VSS	GND	0V	Core and I/O ground
B15	XRAM1_DK0_N	O	HSTL	XRAM Differential Output clock (bits 0-8)
B16	VSS	GND	0V	Core and I/O ground
B17	XRAM1_DATA_12	I/O	HSTL	XRAM Data bit
B18	VSS	GND	0V	Core and I/O ground
B19	XRAM1_DATA_25	I/O	HSTL	XRAM Data bit
B20	VSS	GND	0V	Core and I/O ground
B21	XRAM1_DATA_31	I/O	HSTL	XRAM Data bit
B22	VSS	GND	0V	Core and I/O ground
B23	XRAM1_CNTL_2	O	HSTL	XRAM Control bit
B24	VSS	GND	0V	Core and I/O ground
B25	XRAM1_ADDR_1	O	HSTL	XRAM Address bit
B26	VSS	GND	0V	Core and I/O ground
B27	XRAM1_ADDR_8	O	HSTL	XRAM Address bit
B28	VSS	GND	0V	Core and I/O ground
B29	XRAM1_ADDR_19	O	HSTL	XRAM Address bit
B30	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
C01	GPIO1_6	I/O	LVCMOS	GPIO data bit
C02	GPIO1_5	I/O	LVCMOS	GPIO data bit
C03	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
C04	GPIO1_16	I/O	LVCMOS	GPIO data bit
C05	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
C06	GPIO1_21	I/O	LVCMOS	GPIO data bit
C07	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
C08	GPIO1_27	I/O	LVCMOS	GPIO data bit
C09	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
C10	GPIO1_41	I/O	LVCMOS	GPIO data bit
C11	XRAM1_DQS0_P	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
C12	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C13	XRAM1_DQS3_P	I	HSTL	XRAM Differential Input strobe (bits 27-35)
C14	XRAM1_DATA_4	I/O	HSTL	XRAM Data bit
C15	XRAM1_DK0_P	O	HSTL	XRAM Differential Output clock (bits 0-8)
C16	XRAM1_DK1_N	O	HSTL	XRAM Differential Output clock (bits 9-17)

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
C17	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C18	XRAM1_DATA_18	I/O	HSTL	XRAM Data bit
C19	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C20	XRAM1_DK2_P	O	HSTL	XRAM Differential Output clock (bits 18-26)
C21	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C22	XRAM1_DATA_35	I/O	HSTL	XRAM Data bit (MSB)
C23	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C24	XRAM1_CLK_N	O	HSTL	XRAM Differential output command clock
C25	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C26	XRAM1_ADDR_10	O	HSTL	XRAM Address bit
C27	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C28	XRAM1_ADDR_18	O	HSTL	XRAM Address bit
C29	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
C30	PROM_DATA_1	I	LVCMOS	PROM Data bit
D01	GPIO1_0	I/O	LVCMOS	GPIO data bit
D02	VSS	GND	0V	Core and I/O ground
D03	GPIO1_13	I/O	LVCMOS	GPIO data bit
D04	GPIO1_12	I/O	LVCMOS	GPIO data bit
D05	GPIO1_19	I/O	LVCMOS	GPIO data bit
D06	GPIO1_20	I/O	LVCMOS	GPIO data bit
D07	GPIO1_CLK	I/O	LVCMOS	GPIO clock[a]
D08	GPIO1_31	I/O	LVCMOS	GPIO data bit
D09	GPIO1_39	I/O	LVCMOS	GPIO data bit
D10	GPIO1_45	I/O	LVCMOS	GPIO data bit
D11	XRAM1_DQS0_N	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
D12	VSS	GND	0V	Core and I/O ground
D13	XRAM1_DQS3_N	I	HSTL	XRAM Differential Input strobe (bits 27-35)
D14	XRAM1_DATA_3	I/O	HSTL	XRAM Data bit
D15	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
D16	XRAM1_DK1_P	O	HSTL	XRAM Differential Output clock (bits 9-17)
D17	XRAM1_DATA_16	I/O	HSTL	XRAM Data bit
D18	XRAM1_DATA_23	I/O	HSTL	XRAM Data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
D19	XRAM1_DK3_N	O	HSTL	XRAM Differential Output clock (bits 27-35)
D20	XRAM1_DK2_N	O	HSTL	XRAM Differential Output clock (bits 18-26)
D21	XRAM1_DATA_33	I/O	HSTL	XRAM Data bit
D22	XRAM1_DATA_34	I/O	HSTL	XRAM Data bit
D23	XRAM1_CNTL_1	O	HSTL	XRAM Control bit
D24	XRAM1_CLK_P	O	HSTL	XRAM Command clock
D25	XRAM1_ADDR_7	O	HSTL	XRAM Address bit
D26	XRAM1_ADDR_11	O	HSTL	XRAM Address bit
D27	XRAM1_ADDR_13	O	HSTL	XRAM Address bit
D28	VSS	GND	0V	Core and I/O ground
D29	PROM_DATA_2	I	LVCMOS	PROM Data bit
D30	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
E01	GPIO1_1	I/O	LVCMOS	GPIO data bit
E02	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
E03	GPIO1_2	I/O	LVCMOS	GPIO data bit
E04	GPIO1_7	I/O	LVCMOS	GPIO data bit
E05	GPIO1_9	I/O	LVCMOS	GPIO data bit
E06	GPIO1_26	I/O	LVCMOS	GPIO data bit
E07	GPIO1_24	I/O	LVCMOS	GPIO data bit
E08	GPIO1_32	I/O	LVCMOS	GPIO data bit
E09	GPIO1_34	I/O	LVCMOS	GPIO data bit
E10	GPIO1_44	I/O	LVCMOS	GPIO data bit
E11	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
E12	XRAM1_DQS1_P	I	HSTL	XRAM Differential Input strobe (bits 9-17)
E13	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
E14	XRAM1_DATA_2	I/O	HSTL	XRAM Data bit
E15	XRAM1_DVLD	I	HSTL	XRAM Data Valid Input This pin should come from the RLDRAM devices associated with XRAM_DATA[8:0].
E16	XRAM1_DATA_10	I/O	HSTL	XRAM Data bit
E17	XRAM1_DATA_15	I/O	HSTL	XRAM Data bit
E18	XRAM1_DATA_22	I/O	HSTL	XRAM Data bit
E19	XRAM1_DK3_P	O	HSTL	XRAM Differential Output clock (bits 27-35)

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
E20	XRAM1_DATA_30	I/O	HSTL	XRAM Data bit
E21	XRAM1_DATA_32	I/O	HSTL	XRAM Data bit
E22	XRAM1_BANK_2	O	HSTL	XRAM Bank bit
E23	XRAM1_ADDR_5	O	HSTL	XRAM Address bit
E24	XRAM1_ADDR_4	O	HSTL	XRAM Address bit
E25	XRAM1_ADDR_16	O	HSTL	XRAM Address bit
E26	XRAM1_ADDR_14	O	HSTL	XRAM Address bit
E27	XRAM1_ADDR_17	O	HSTL	XRAM Address bit
E28	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
E29	PROM_DATA_3	I	LVCMOS	PROM Data bit
E30	PROM_DATA_0	I	LVCMOS	PROM Data bit (LSB)
F01	TX1_DATA_15_N	O	LVDS/HSTL	Transmit Data bit
F02	TX1_DATA_15_P	O	LVDS/HSTL	Transmit Data bit (MSB)
F03	VSS	GND	0V	Core and I/O ground
F04	GPIO1_4	I/O	LVCMOS	GPIO data bit
F05	VSS	GND	0V	Core and I/O ground
F06	GPIO1_8	I/O	LVCMOS	GPIO data bit
F07	VSS	GND	0V	Core and I/O ground
F08	GPIO1_25	I/O	LVCMOS	GPIO data bit
F09	VSS	GND	0V	Core and I/O ground
F10	GPIO1_40	I/O	LVCMOS	GPIO data bit
F11	VSS	GND	0V	Core and I/O ground
F12	XRAM1_DQS1_N	I	HSTL	XRAM Differential Input strobe (bits 9-17)
F13	VSS	GND	0V	Core and I/O ground
F14	XRAM1_DATA_1	I/O	HSTL	XRAM Data bit
F15	VSS	GND	0V	Core and I/O ground
F16	XRAM1_DATA_9	I/O	HSTL	XRAM Data bit
F17	VSS	GND	0V	Core and I/O ground
F18	XRAM1_DATA_21	I/O	HSTL	XRAM Data bit
F19	VSS	GND	0V	Core and I/O ground
F20	XRAM1_DATA_29	I/O	HSTL	XRAM Data bit
F21	VSS	GND	0V	Core and I/O ground
F22	XRAM1_BANK_1	O	HSTL	XRAM Bank bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
F23	VSS	GND	0V	Core and I/O ground
F24	XRAM1_ADDR_3	O	HSTL	XRAM Address bit
F25	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
F26	XRAM1_ADDR_15	O	HSTL	XRAM Address bit
F27	PROM_CLKO	O	LVCMOS	PROM Clock Output
F28	PROM_DATA_4	I	LVCMOS	PROM Data bit
F29	PROM_CLKDIV	I	LVCMOS	PROM Clock Divider Input 0 = Divide by 2 1 = Divide by 4
F30	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
G01	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
G02	TX1_DATA_14_N	O	LVDS/HSTL	Transmit Data bit
G03	TX1_DATA_14_P	O	LVDS/HSTL	Transmit Data bit
G04	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
G05	GPIO1_3	I/O	LVCMOS	GPIO data bit
G06	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G07	GPIO1_11	I/O	LVCMOS	GPIO data bit
G08	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G09	GPIO1_33	I/O	LVCMOS	GPIO data bit
G10	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G11	NC12	N/A	N/A	No Connect
G12	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
G13	VSS	GND	0V	Core and I/O ground
G14	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G15	XRAM1_DATA_7	I/O	HSTL	XRAM Data bit
G16	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G17	XRAM1_DATA_14	I/O	HSTL	XRAM Data bit
G18	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G19	XRAM1_DATA_26	I/O	HSTL	XRAM Data bit
G20	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G21	XRAM1_BANK_0	O	HSTL	XRAM Bank bit
G22	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
G23	XRAM1_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
G24	PROM_VDD_PST	PWR	2.5V	Connect to 2.5V
G25	PROM_CEN	O	LVCMOS	PROM Chip Enable (low active)
G26	PROM_DATA_5	I	LVCMOS	PROM Data bit
G27	PROM_CLK	I	LVCMOS	PROM Clock Input
G28	VSS	GND	0V	Core and I/O ground
G29	RX2_DATA_15_N	I	LVDS/HSTL	Receive Data bit
G30	RX2_DATA_15_P	I	LVDS/HSTL	Receive Data bit (MSB)
H01	TX1_DATA_12_N	O	LVDS/HSTL	Transmit Data bit
H02	TX1_DATA_12_P	O	LVDS/HSTL	Transmit Data bit
H03	VSS	GND	0V	Core and I/O ground
H04	TX1_DATA_13_N	O	LVDS/HSTL	Transmit Data bit
H05	TX1_DATA_13_P	O	LVDS/HSTL	Transmit Data bit
H06	VSS	GND	0V	Core and I/O ground
H07	GPIO1_10	I/O	LVCMOS	GPIO data bit
H08	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
H09	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
H10	GPIO1_43	I/O	LVCMOS	GPIO data bit
H11	NC13	N/A	N/A	No Connect
H12	GPIO1_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
H13	VSS	GND	0V	Core and I/O ground
H14	XRAM1_DATA_6	I/O	HSTL	XRAM Data bit
H15	XRAM1_DATA_8	I/O	HSTL	XRAM Data bit
H16	XRAM1_DATA_17	I/O	HSTL	XRAM Data bit
H17	VSS	GND	0V	Core and I/O ground
H18	VDD	PWR	1.2v	Core power supply
H19	VSS	GND	0V	Core and I/O ground
H20	VDD	PWR	1.2v	Core power supply
H21	VSS	GND	0V	Core and I/O ground
H22	VDD	PWR	1.2v	Core power supply
H23	VSS	GND	0V	Core and I/O ground
H24	PROM_DISABLE	I	LVCMOS	PROM Disable Input
H25	PROM_OE	O	LVCMOS	PROM Output Enable
H26	PROM_DATA_6	I	LVCMOS	PROM Data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
H27	PROM_DATA_7	I	LVCMOS	PROM Data bit (MSB)
H28	RX2_DATA_13_P	I	LVDS/HSTL	Receive Data bit
H29	RX2_DATA_13_N	I	LVDS/HSTL	Receive Data bit
H30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
J01	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
J02	TX1_DATA_10_P	O	LVDS/HSTL	Transmit Data bit
J03	TX1_DATA_10_N	O	LVDS/HSTL	Transmit Data bit
J04	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
J05	TX1_DATA_11_N	O	LVDS/HSTL	Transmit Data bit
J06	TX1_DATA_11_P	O	LVDS/HSTL	Transmit Data bit
J07	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
J08	TPLL1_CAP	I	Analog	Do not connect
J09	TPLL1_REF	I	LVCMOS	18.75 - 37.5Mhz reference clock input for Transmit PLL
J10	TPLL1_AVSS	GND	Analog	Connect to Analog Ground See "PLL Power Characteristics" on page 74 for more information.
J11	VDD	PWR	1.2v	Core power supply
J12	VSS	GND	0V	Core and I/O ground
J13	VDD	PWR	1.2v	Core power supply
J14	VSS	GND	0V	Core and I/O ground
J15	XRAM1_VREF1	I	Analog	Connect to XRAM reference voltage (0.9V)
J16	XRAM1_VREF2	I	Analog	Connect to XRAM reference voltage (0.9V)
J17	VDD	PWR	1.2v	Core power supply
J18	XRAM1_VREF3	I	Analog	Connect to XRAM reference voltage (0.9V)
J19	VDD	PWR	1.2v	Core power supply
J20	VSS	GND	0V	Core and I/O ground
J21	VDD	PWR	1.2v	Core power supply
J22	VSS	GND	0V	Core and I/O ground
J23	VDD	PWR	1.2v	Core power supply
J24	PROM_SERIAL	I	LVCMOS	PROM Serial/Parallel mode select 0 = 8-bit connection 1 = 1-bit connection
J25	VSS	GND	0V	Core and I/O ground
J26	RX2_DATA_14_P	I	LVDS/HSTL	Receive Data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
J27	RX2_DATA_14_N	I	LVDS/HSTL	Receive Data bit
J28	VSS	GND	0V	Core and I/O ground
J29	RX2_DATA_10_P	I	LVDS/HSTL	Receive Data bit
J30	RX2_DATA_10_N	I	LVDS/HSTL	Receive Data bit
K01	TX1_DATA_8_P	O	LVDS/HSTL	Transmit Data bit
K02	TX1_DATA_8_N	O	LVDS/HSTL	Transmit Data bit
K03	VSS	GND	0V	Core and I/O ground
K04	TX1_DATA_9_N	O	LVDS/HSTL	Transmit Data bit
K05	TX1_DATA_9_P	O	LVDS/HSTL	Transmit Data bit
K06	VSS	GND	0V	Core and I/O ground
K07	VSS	GND	0V	Core and I/O ground
K08	NC6	N/A	N/A	No Connect
K09	TPLL1_AVDD	PWR	Analog	Connect to Analog 2.5V See "PLL Power Characteristics" on page 74 for more information.
K10	VDD	PWR	1.2v	Core power supply
K11	VSS	GND	0V	Core and I/O ground
K12	VDD	PWR	1.2v	Core power supply
K13	VSS	GND	0V	Core and I/O ground
K14	VDD	PWR	1.2v	Core power supply
K15	VSS	GND	0V	Core and I/O ground
K16	VDD	PWR	1.2v	Core power supply
K17	VSS	GND	0V	Core and I/O ground
K18	VDD	PWR	1.2v	Core power supply
K19	VSS	GND	0V	Core and I/O ground
K20	VDD	PWR	1.2v	Core power supply
K21	VSS	GND	0V	Core and I/O ground
K22	VDD	PWR	1.2v	Core power supply
K23	VSS	GND	0V	Core and I/O ground
K24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
K25	RX2_DATA_12_N	I	LVDS/HSTL	Receive Data bit
K26	RX2_DATA_12_P	I	LVDS/HSTL	Receive Data bit
K27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
K28	RX2_DATA_11_N	I	LVDS/HSTL	Receive Data bit
K29	RX2_DATA_11_P	I	LVDS/HSTL	Receive Data bit
K30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
L01	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
L02	TX1_DATA_7_N	O	LVDS/HSTL	Transmit Data bit
L03	TX1_DATA_7_P	O	LVDS/HSTL	Transmit Data bit
L04	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
L05	TX1_CNTL_N	O	LVDS/HSTL	Transmit Control bit
L06	TX1_CNTL_P	O	LVDS/HSTL	Transmit Control bit
L07	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
L08	VSS	GND	0V	Core and I/O ground
L09	VDD	PWR	1.2v	Core power supply
L10	VSS	GND	0V	Core and I/O ground
L11	VDD	PWR	1.2v	Core power supply
L12	VSS	GND	0V	Core and I/O ground
L13	VDD	PWR	1.2v	Core power supply
L14	VSS	GND	0V	Core and I/O ground
L15	VDD	PWR	1.2v	Core power supply
L16	VSS	GND	0V	Core and I/O ground
L17	VDD	PWR	1.2v	Core power supply
L18	VSS	GND	0V	Core and I/O ground
L19	VDD	PWR	1.2v	Core power supply
L20	VSS	GND	0V	Core and I/O ground
L21	VDD	PWR	1.2v	Core power supply
L22	VSS	GND	0V	Core and I/O ground
L23	VDD	PWR	1.2v	Core power supply
L24	VDD	PWR	1.2v	Core power supply
L25	VSS	GND	0V	Core and I/O ground
L26	RX2_DATA_9_P	I	LVDS/HSTL	Receive Data bit
L27	RX2_DATA_9_N	I	LVDS/HSTL	Receive Data bit
L28	VSS	GND	0V	Core and I/O ground
L29	RX2_DATA_8_P	I	LVDS/HSTL	Receive Data bit
L30	RX2_DATA_8_N	I	LVDS/HSTL	Receive Data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
M01	TX1_DATA_5_N	O	LVDS/HSTL	Transmit Data bit
M02	TX1_DATA_5_P	O	LVDS/HSTL	Transmit Data bit
M03	VSS	GND	0V	Core and I/O ground
M04	TX1_DATA_6_N	O	LVDS/HSTL	Transmit Data bit
M05	TX1_DATA_6_P	O	LVDS/HSTL	Transmit Data bit
M06	VSS	GND	0V	Core and I/O ground
M07	VSS	GND	0V	Core and I/O ground
M08	VDD	PWR	1.2v	Core power supply
M09	VSS	GND	0V	Core and I/O ground
M10	VDD	PWR	1.2v	Core power supply
M11	VSS	GND	0V	Core and I/O ground
M12	VDD	PWR	1.2v	Core power supply
M13	VSS	GND	0V	Core and I/O ground
M14	VDD	PWR	1.2v	Core power supply
M15	VSS	GND	0V	Core and I/O ground
M16	VDD	PWR	1.2v	Core power supply
M17	VSS	GND	0V	Core and I/O ground
M18	VDD	PWR	1.2v	Core power supply
M19	VSS	GND	0V	Core and I/O ground
M20	VDD	PWR	1.2v	Core power supply
M21	VSS	GND	0V	Core and I/O ground
M22	VDD	PWR	1.2v	Core power supply
M23	VSS	GND	0V	Core and I/O ground
M24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
M25	RX2_CNTL_P	I	LVDS/HSTL	Receive Control bit
M26	RX2_CNTL_N	I	LVDS/HSTL	Receive Control bit
M27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
M28	RX2_DATA_7_N	I	LVDS/HSTL	Receive Data bit
M29	RX2_DATA_7_P	I	LVDS/HSTL	Receive Data bit
M30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
N01	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
N02	TX1_CLK1_N	O	LVDS/HSTL	Transmit Clock
N03	TX1_CLK1_P	O	LVDS/HSTL	Transmit Clock

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
N04	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
N05	TX1_DATA_4_N	O	LVDS/HSTL	Transmit Data bit
N06	TX1_DATA_4_P	O	LVDS/HSTL	Transmit Data bit
N07	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
N08	VSS	GND	0V	Core and I/O ground
N09	VDD	PWR	1.2v	Core power supply
N10	VSS	GND	0V	Core and I/O ground
N11	VDD	PWR	1.2v	Core power supply
N12	VSS	GND	0V	Core and I/O ground
N13	VDD	PWR	1.2v	Core power supply
N14	VSS	GND	0V	Core and I/O ground
N15	VDD	PWR	1.2v	Core power supply
N16	VSS	GND	0V	Core and I/O ground
N17	VDD	PWR	1.2v	Core power supply
N18	VSS	GND	0V	Core and I/O ground
N19	VDD	PWR	1.2v	Core power supply
N20	VSS	GND	0V	Core and I/O ground
N21	VDD	PWR	1.2v	Core power supply
N22	VSS	GND	0V	Core and I/O ground
N23	VDD	PWR	1.2v	Core power supply
N24	VDD	PWR	1.2v	Core power supply
N25	VSS	GND	0V	Core and I/O ground
N26	RX2_DATA_6_P	I	LVDS/HSTL	Receive Data bit
N27	RX2_DATA_6_N	I	LVDS/HSTL	Receive Data bit
N28	VSS	GND	0V	Core and I/O ground
N29	RX2_DATA_5_N	I	LVDS/HSTL	Receive Data bit
N30	RX2_DATA_5_P	I	LVDS/HSTL	Receive Data bit
P01	TX1_DATA_2_N	O	LVDS/HSTL	Transmit Data bit
P02	TX1_DATA_2_P	O	LVDS/HSTL	Transmit Data bit
P03	VSS	GND	0V	Core and I/O ground
P04	TX1_DATA_3_N	O	LVDS/HSTL	Transmit Data bit
P05	TX1_DATA_3_P	O	LVDS/HSTL	Transmit Data bit
P06	VSS	GND	0V	Core and I/O ground

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
P07	VSS	GND	0V	Core and I/O ground
P08	VDD	PWR	1.2v	Core power supply
P09	VSS	GND	0V	Core and I/O ground
P10	VDD	PWR	1.2v	Core power supply
P11	VSS	GND	0V	Core and I/O ground
P12	VDD	PWR	1.2v	Core power supply
P13	VSS	GND	0V	Core and I/O ground
P14	VDD	PWR	1.2v	Core power supply
P15	VSS	GND	0V	Core and I/O ground
P16	VDD	PWR	1.2v	Core power supply
P17	VSS	GND	0V	Core and I/O ground
P18	VDD	PWR	1.2v	Core power supply
P19	VSS	GND	0V	Core and I/O ground
P20	VDD	PWR	1.2v	Core power supply
P21	VSS	GND	0V	Core and I/O ground
P22	VDD	PWR	1.2v	Core power supply
P23	VSS	GND	0V	Core and I/O ground
P24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
P25	RX2_CLK1_P	I	LVDS/HSTL	Receive Clock
P26	RX2_CLK1_N	I	LVDS/HSTL	Receive Clock
P27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
P28	RX2_DATA_4_N	I	LVDS/HSTL	Receive Data bit
P29	RX2_DATA_4_P	I	LVDS/HSTL	Receive Data bit
P30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
R01	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R02	TX1_DATA_0_P	O	LVDS/HSTL	Transmit Data bit
R03	TX1_DATA_0_N	O	LVDS/HSTL	Transmit Data bit (LSB)
R04	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R05	TX1_DATA_1_N	O	LVDS/HSTL	Transmit Data bit
R06	TX1_DATA_1_P	O	LVDS/HSTL	Transmit Data bit
R07	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R08	TX1_VDD_PST	PWR	2.5V	LVDS 2.5V
R09	NC8	N/A	N/A	No Connect

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
R10	VSS	GND	0V	Core and I/O ground
R11	VDD	PWR	1.2v	Core power supply
R12	VSS	GND	0V	Core and I/O ground
R13	VDD	PWR	1.2v	Core power supply
R14	VSS	GND	0V	Core and I/O ground
R15	VDD	PWR	1.2v	Core power supply
R16	VSS	GND	0V	Core and I/O ground
R17	VDD	PWR	1.2v	Core power supply
R18	VSS	GND	0V	Core and I/O ground
R19	VDD	PWR	1.2v	Core power supply
R20	VSS	GND	0V	Core and I/O ground
R21	VDD	PWR	1.2v	Core power supply
R22	NC17	N/A	N/A	No Connect
R23	NC10	N/A	N/A	No Connect
R24	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
R25	VSS	GND	0V	Core and I/O ground
R26	RX2_DATA_3_P	I	LVDS/HSTL	Receive Data bit
R27	RX2_DATA_3_N	I	LVDS/HSTL	Receive Data bit
R28	VSS	GND	0V	Core and I/O ground
R29	RX2_DATA_2_N	I	LVDS/HSTL	Receive Data bit
R30	RX2_DATA_2_P	I	LVDS/HSTL	Receive Data bit
T01	RX1_DATA_0_P	I	LVDS/HSTL	Receive Data bit
T02	RX1_DATA_0_N	I	LVDS/HSTL	Receive Data bit (LSB)
T03	VSS	GND	0V	Core and I/O ground
T04	TX1_TEST_N	O	LVDS/HSTL	Production test pin - do not connect
T05	TX1_TEST_P	O	LVDS/HSTL	Production test pin - do not connect
T06	VSS	GND	0V	Core and I/O Ground
T07	VSS	GND	0V	Core and I/O Ground
T08	NC16	N/A	N/A	No Connect
T09	NC1	N/A	N/A	No Connect
T10	VDD	PWR	1.2v	Core power supply
T11	VSS	GND	0V	Core and I/O ground
T12	VDD	PWR	1.2v	Core power supply

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
T13	VSS	GND	0V	Core and I/O ground
T14	VDD	PWR	1.2v	Core power supply
T15	VSS	GND	0V	Core and I/O ground
T16	VDD	PWR	1.2v	Core power supply
T17	VSS	GND	0V	Core and I/O ground
T18	VDD	PWR	1.2v	Core power supply
T19	VSS	GND	0V	Core and I/O ground
T20	VDD	PWR	1.2v	Core power supply
T21	VSS	GND	0V	Core and I/O ground
T22	NC11	N/A	N/A	No Connect
T23	VSS	GND	0V	Core and I/O ground
T24	VSS	GND	0V	Core and I/O ground
T25	RX2_DATA_1_P	I	LVDS/HSTL	Receive Data bit
T26	RX2_DATA_1_N	I	LVDS/HSTL	Receive Data bit
T27	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
T28	RX2_DATA_0_N	I	LVDS/HSTL	Receive Data bit (LSB)
T29	RX2_DATA_0_P	I	LVDS/HSTL	Receive Data bit
T30	RX2_VDD_PST	PWR	2.5V	Connect to 2.5V
U01	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
U02	RX1_DATA_1_N	I	LVDS/HSTL	Receive Data bit
U03	RX1_DATA_1_P	I	LVDS/HSTL	Receive Data bit
U04	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
U05	RX1_DATA_2_N	I	LVDS/HSTL	Receive Data bit
U06	RX1_DATA_2_P	I	LVDS/HSTL	Receive Data bit
U07	NC2	N/A	N/A	No Connect
U08	NC9	N/A	N/A	No Connect
U09	TX1_VREF	I	1.2V Analog	LVDS TX1 Analog 1.2V common mode voltage reference
U10	VSS	GND	0V	Core and I/O ground
U11	VDD	PWR	1.2v	Core power supply
U12	VSS	GND	0V	Core and I/O ground
U13	VDD	PWR	1.2v	Core power supply
U14	VSS	GND	0V	Core and I/O ground

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
U15	VDD	PWR	1.2v	Core power supply
U16	VSS	GND	0V	Core and I/O ground
U17	VDD	PWR	1.2v	Core power supply
U18	VSS	GND	0V	Core and I/O ground
U19	VDD	PWR	1.2v	Core power supply
U20	VSS	GND	0V	Core and I/O ground
U21	VDD	PWR	1.2v	Core power supply
U22	NC3	N/A	N/A	No Connect
U23	TX2_VREF	I	Analog	LVDS TX2 Analog 1.2V common mode voltage reference
U24	NC4	N/A	N/A	No Connect
U25	VSS	GND	0V	Core and I/O ground
U26	TX2_DATA_0_P	O	LVDS/HSTL	Transmit Data bit
U27	TX2_DATA_0_N	O	LVDS/HSTL	Transmit Data bit (LSB)
U28	VSS	GND	0V	Core and I/O ground
U29	TX2_TEST_N	O	LVDS/HSTL	Production test pin - do not connect
U30	TX2_TEST_P	O	LVDS/HSTL	Production test pin - do not connect
V01	RX1_DATA_3_P	I	LVDS/HSTL	Receive Data bit
V02	RX1_DATA_3_N	I	LVDS/HSTL	Receive Data bit
V03	VSS	GND	0V	Core and I/O ground
V04	RX1_CLK1_P	I	LVDS/HSTL	Receive Clock
V05	RX1_CLK1_N	I	LVDS/HSTL	Receive Clock
V06	VSS	GND	0V	Core and I/O ground
V07	VDD	PWR	1.2v	Core power supply
V08	VDD	PWR	1.2v	Core power supply
V09	VDD	PWR	1.2v	Core power supply
V10	VDD	PWR	1.2v	Core power supply
V11	VSS	GND	0V	Core and I/O ground
V12	VDD	PWR	1.2v	Core power supply
V13	VSS	GND	0V	Core and I/O ground
V14	VDD	PWR	1.2v	Core power supply
V15	VSS	GND	0V	Core and I/O ground
V16	VDD	PWR	1.2v	Core power supply

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
V17	VSS	GND	0V	Core and I/O ground
V18	VDD	PWR	1.2v	Core power supply
V19	VSS	GND	0V	Core and I/O ground
V20	VDD	PWR	1.2v	Core power supply
V21	VSS	GND	0V	Core and I/O ground
V22	VDD	PWR	1.2v	Core power supply
V23	VSS	GND	0V	Core and I/O ground
V24	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
V25	TX2_DATA_2_P	O	LVDS/HSTL	Transmit Data bit
V26	TX2_DATA_2_N	O	LVDS/HSTL	Transmit Data bit
V27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
V28	TX2_DATA_1_N	O	LVDS/HSTL	Transmit Data bit
V29	TX2_DATA_1_P	O	LVDS/HSTL	Transmit Data bit
V30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
W01	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
W02	RX1_DATA_4_N	I	LVDS/HSTL	Receive Data bit
W03	RX1_DATA_4_P	I	LVDS/HSTL	Receive Data bit
W04	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
W05	RX1_DATA_5_P	I	LVDS/HSTL	Receive Data bit
W06	RX1_DATA_5_N	I	LVDS/HSTL	Receive Data bit
W07	VDD	PWR	1.2v	Core power supply
W08	VDD	PWR	1.2v	Core power supply
W09	VDD	PWR	1.2v	Core power supply
W10	VSS	GND	0V	Core and I/O ground
W11	VDD	PWR	1.2v	Core power supply
W12	VSS	GND	0V	Core and I/O ground
W13	VDD	PWR	1.2v	Core power supply
W14	VSS	GND	0V	Core and I/O ground
W15	VDD	PWR	1.2v	Core power supply
W16	VSS	GND	0V	Core and I/O ground
W17	VDD	PWR	1.2v	Core power supply
W18	VSS	GND	0V	Core and I/O ground
W19	VDD	PWR	1.2v	Core power supply

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
W20	VSS	GND	0V	Core and I/O ground
W21	VDD	PWR	1.2v	Core power supply
W22	NC7	N/A	N/A	No Connect
W23	VDD	PWR	1.2v	Core power supply
W24	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
W25	VSS	GND	0V	Core and I/O ground
W26	TX2_CLK1_P	O	LVDS/HSTL	Transmit Clock
W27	TX2_CLK1_N	O	LVDS/HSTL	Transmit Clock
W28	VSS	GND	0V	Core and I/O ground
W29	TX2_DATA_3_P	O	LVDS/HSTL	Transmit Data bit
W30	TX2_DATA_3_N	O	LVDS/HSTL	Transmit Data bit
Y01	RX1_DATA_6_N	I	LVDS/HSTL	Receive Data bit
Y02	RX1_DATA_6_P	I	LVDS/HSTL	Receive Data bit
Y03	VSS	GND	0V	Core and I/O ground
Y04	RX1_DATA_7_N	I	LVDS/HSTL	Receive Data bit
Y05	RX1_DATA_7_P	I	LVDS/HSTL	Receive Data bit
Y06	CPLL_CAP	I	Analog	Do not connect
Y07	CLOCK_P	I	LVDS	Core clock bypass input
Y08	CPLL_AVSS	GND	Analog	Connect to Analog Ground See "PLL Power Characteristics" on page 74 for more information.
Y09	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
Y10	VDD	PWR	1.2v	Core power supply
Y11	VSS	GND	0V	Core and I/O ground
Y12	VDD	PWR	1.2v	Core power supply
Y13	VSS	GND	0V	Core and I/O ground
Y14	VDD	PWR	1.2v	Core power supply
Y15	VSS	GND	0V	Core and I/O ground
Y16	VDD	PWR	1.2v	Core power supply
Y17	VSS	GND	0V	Core and I/O ground
Y18	VDD	PWR	1.2v	Core power supply
Y19	VSS	GND	0V	Core and I/O ground
Y20	VDD	PWR	1.2v	Core power supply

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
Y21	VSS	GND	0V	Core and I/O ground
Y22	TPLL2_AVSS	GND	Analog	Connect to Analog Ground See "PLL Power Characteristics" on page 74 for more information.
Y23	TPLL2_AVDD	PWR	Analog	Connect to Analog 2.5V See "PLL Power Characteristics" on page 74 for more information.
Y24	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
Y25	TX2_DATA_5_P	O	LVDS/HSTL	Transmit Data bit
Y26	TX2_DATA_5_N	O	LVDS/HSTL	Transmit Data bit
Y27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
Y28	TX2_DATA_4_P	O	LVDS/HSTL	Transmit Data bit
Y29	TX2_DATA_4_N	O	LVDS/HSTL	Transmit Data bit
Y30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AA01	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AA02	RX1_DATA_8_N	I	LVDS/HSTL	Receive Data bit
AA03	RX1_DATA_8_P	I	LVDS/HSTL	Receive Data bit
AA04	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AA05	RX1_CNTL_N	I	LVDS/HSTL	Receive Control bit
AA06	RX1_CNTL_P	I	LVDS/HSTL	Receive Control bit
AA07	CLOCK_N	I	LVDS	Core clock bypass input
AA08	CPLL_AVDD	PWR	Analog	Connect to Analog 2.5V See "PLL Power Characteristics" on page 74 for more information.
AA09	CPLL_REF	I	LVCMOS	18.75 - 37.5 MHz reference clock input for Core PLL
AA10	VSS	GND	0V	Core and I/O ground
AA11	VDD	PWR	1.2v	Core power supply
AA12	VSS	GND	0V	Core and I/O ground
AA13	VDD	PWR	1.2v	Core power supply
AA14	VSS	GND	0V	Core and I/O ground
AA15	VDD	PWR	1.2v	Core power supply
AA16	VSS	GND	0V	Core and I/O ground
AA17	VDD	PWR	1.2v	Core power supply
AA18	VSS	GND	0V	Core and I/O ground
AA19	VDD	PWR	1.2v	Core power supply

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AA20	VSS	GND	0V	Core and I/O ground
AA21	JTAG_VDD_PST	PWR	2.5V	Connect to 2.5V
AA22	VSS	GND	0V	Core and I/O ground
AA23	TPLL2_CAP	I	Analog	Do not connect
AA24	TRSTn	I	LVCMOS	JTAG Test Reset (low active) This input has a built-in pullup resistor.
AA25	VSS	GND	0V	Core and I/O ground
AA26	TX2_DATA_7_N	O	LVDS/HSTL	Transmit Data bit
AA27	TX2_DATA_7_P	O	LVDS/HSTL	Transmit Data bit
AA28	VSS	GND	0V	Core and I/O ground
AA29	TX2_DATA_6_P	O	LVDS/HSTL	Transmit Data bit
AA30	TX2_DATA_6_N	O	LVDS/HSTL	Transmit Data bit
AB01	RX1_DATA_9_N	I	LVDS/HSTL	Receive Data bit
AB02	RX1_DATA_9_P	I	LVDS/HSTL	Receive Data bit
AB03	VSS	GND	0V	Core and I/O ground
AB04	RX1_DATA_11_N	I	LVDS/HSTL	Receive Data bit
AB05	RX1_DATA_11_P	I	LVDS/HSTL	Receive Data bit
AB06	VSS	GND	0V	Core and I/O ground
AB07	NC5	N/A	N/A	No Connect
AB08	GPIO2_20	I/O	LVCMOS	GPIO data bit
AB09	GPIO2_18	I/O	LVCMOS	GPIO data bit
AB10	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AB11	VSS	GND	0V	Core and I/O ground
AB12	VDD	PWR	1.2v	Core power supply
AB13	VSS	GND	0V	Core and I/O ground
AB14	VDD	PWR	1.2v	Core power supply
AB15	VSS	GND	0V	Core and I/O ground
AB16	VDD	PWR	1.2v	Core power supply
AB17	VSS	GND	0V	Core and I/O ground
AB18	VDD	PWR	1.2v	Core power supply
AB19	VSS	GND	0V	Core and I/O ground
AB20	VDD	PWR	1.2v	Core power supply
AB21	JTAG_VDD_PST	PWR	2.5V	Connect to 2.5V

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AB22	TMS	I	LVCMOS	JTAG Test Mode Select This input has a built-in pullup resistor.
AB23	TDO	O	LVCMOS	JTAG Test Data Output
AB24	TCLK	I	LVCMOS	JTAG Test Clock Input This input has a built-in pullup resistor.
AB25	TX2_DATA_8_N	O	LVDS/HSTL	Transmit Data bit
AB26	TX2_DATA_8_P	O	LVDS/HSTL	Transmit Data bit
AB27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AB28	TX2_CNTL_P	O	LVDS/HSTL	Transmit Control bit
AB29	TX2_CNTL_N	O	LVDS/HSTL	Transmit Control bit
AB30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AC01	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AC02	RX1_DATA_10_P	I	LVDS/HSTL	Receive Data bit
AC03	RX1_DATA_10_N	I	LVDS/HSTL	Receive Data bit
AC04	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AC05	VSS	GND	0V	Core and I/O ground
AC06	VSS	GND	0V	Core and I/O ground
AC07	GPIO2_14	I/O	LVCMOS	GPIO data bit
AC08	GPIO2_21	I/O	LVCMOS	GPIO data bit
AC09	GPIO2_19	I/O	LVCMOS	GPIO data bit
AC10	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AC11	NC15	N/A	N/A	No Connect
AC12	VSS	GND	0V	Core and I/O ground
AC13	NC14	N/A	N/A	No Connect
AC14	VSS	GND	0V	Core and I/O ground
AC15	XRAM2_VREF1	I	Analog	Connect to XRAM reference voltage (0.9V)
AC16	VSS	GND	0V	Core and I/O ground
AC17	VDD	PWR	1.2v	Core power supply
AC18	XRAM2_VREF2	I	Analog	Connect to XRAM reference voltage (0.9V)
AC19	VDD	PWR	1.2v	Core power supply
AC20	VSS	GND	0V	Core and I/O ground
AC21	TPLL2_REF	I	LVCMOS	18.75 - 37.5Mhz reference clock input for Transmit PLL
AC22	RESETn	I	LVCMOS	FPOA Reset (low active)

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AC23	TDI	I	LVCMOS	JTAG Test Data Input This input has a built-in pullup resistor.
AC24	TESTMODE	I	LVCMOS	Connect to ground This input has a built-in pulldown resistor.
AC25	XRAM2_ADDR_10	O	HSTL	XRAM Address bit
AC26	TX2_DATA_10_P	O	LVDS/HSTL	Transmit Data bit
AC27	TX2_DATA_10_N	O	LVDS/HSTL	Transmit Data bit
AC28	VSS	GND	0V	Core and I/O ground
AC29	TX2_DATA_9_N	O	LVDS/HSTL	Transmit Data bit
AC30	TX2_DATA_9_P	O	LVDS/HSTL	Transmit Data bit
AD01	RX1_DATA_12_N	I	LVDS/HSTL	Receive Data bit
AD02	RX1_DATA_12_P	I	LVDS/HSTL	Receive Data bit
AD03	VSS	GND	0V	Core and I/O ground
AD04	RX1_DATA_13_N	I	LVDS/HSTL	Receive Data bit
AD05	RX1_DATA_13_P	I	LVDS/HSTL	Receive Data bit
AD06	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AD07	GPIO2_15	I/O	LVCMOS	GPIO data bit
AD08	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AD09	GPIO2_28	I/O	LVCMOS	GPIO data bit
AD10	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AD11	VSS	GND	0V	Core and I/O ground
AD12	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD13	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD14	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD15	XRAM2_DATA_9	I/O	HSTL	XRAM Data bit
AD16	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD17	XRAM2_DATA_16	I/O	HSTL	XRAM Data bit
AD18	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD19	XRAM2_VREF3	I	Analog	Connect to XRAM reference voltage (0.9V)
AD20	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD21	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD22	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD23	XRAM2_ADDR_4	O	HSTL	XRAM Address bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AD24	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AD25	XRAM2_ADDR_11	O	HSTL	XRAM Address bit
AD26	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AD27	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AD28	TX2_DATA_11_N	O	LVDS/HSTL	Transmit Data bit
AD29	TX2_DATA_11_P	O	LVDS/HSTL	Transmit Data bit
AD30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AE01	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AE02	RX1_DATA_14_N	I	LVDS/HSTL	Receive Data bit
AE03	RX1_DATA_14_P	I	LVDS/HSTL	Receive Data bit
AE04	RX1_VDD_PST	PWR	2.5V	Connect to 2.5V
AE05	VSS	GND	0V	Core and I/O ground
AE06	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AE07	VSS	GND	0V	Core and I/O ground
AE08	GPIO2_22	I/O	LVCMOS	GPIO data bit
AE09	VSS	GND	0V	Core and I/O ground
AE10	GPIO2_35	I/O	LVCMOS	GPIO data bit
AE11	VSS	GND	0V	Core and I/O ground
AE12	XRAM2_DQS0_P	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
AE13	VSS	GND	0V	Core and I/O ground
AE14	XRAM2_DATA_6	I/O	HSTL	XRAM Data bit
AE15	VSS	GND	0V	Core and I/O ground
AE16	XRAM2_DATA_13	I/O	HSTL	XRAM Data bit
AE17	VSS	GND	0V	Core and I/O ground
AE18	XRAM2_DATA_20	I/O	HSTL	XRAM Data bit
AE19	VSS	GND	0V	Core and I/O ground
AE20	XRAM2_DK2_P	O	HSTL	XRAM Differential Output clock (bits 18-26)
AE21	VSS	GND	0V	Core and I/O ground
AE22	XRAM2_DATA_34	I/O	HSTL	XRAM Data bit
AE23	VSS	GND	0V	Core and I/O ground
AE24	XRAM2_ADDR_3	O	HSTL	XRAM Address bit
AE25	VSS	GND	0V	Core and I/O ground
AE26	TX2_DATA_12_P	O	LVDS/HSTL	Transmit Data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AE27	TX2_DATA_12_N	O	LVDS/HSTL	Transmit Data bit
AE28	VSS	GND	0V	Core and I/O ground
AE29	TX2_DATA_13_P	O	LVDS/HSTL	Transmit Data bit
AE30	TX2_DATA_13_N	O	LVDS/HSTL	Transmit Data bit
AF01	RX1_DATA_15_N	I	LVDS/HSTL	Receive Data bit
AF02	RX1_DATA_15_P	I	LVDS/HSTL	Receive Data bit (MSB)
AF03	VSS	GND	0V	Core and I/O ground
AF04	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AF05	GPIO2_11	I/O	LVCMOS	GPIO data bit
AF06	GPIO2_16	I/O	LVCMOS	GPIO data bit
AF07	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AF08	GPIO2_23	I/O	LVCMOS	GPIO data bit
AF09	GPIO2_37	I/O	LVCMOS	GPIO data bit
AF10	GPIO2_36	I/O	LVCMOS	GPIO data bit
AF11	GPIO2_45	I/O	LVCMOS	GPIO data bit
AF12	XRAM2_DQS0_N	I	HSTL	XRAM Differential Input strobe (bits 0-8, DVLD)
AF13	XRAM2_DQS2_P	I	HSTL	XRAM Differential Input strobe (bits 18-26)
AF14	XRAM2_DATA_0	I/O	HSTL	XRAM Data bit (LSB)
AF15	XRAM2_DATA_7	I/O	HSTL	XRAM Data bit
AF16	XRAM2_DATA_14	I/O	HSTL	XRAM Data bit
AF17	XRAM2_DATA_17	I/O	HSTL	XRAM Data bit
AF18	XRAM2_DATA_21	I/O	HSTL	XRAM Data bit
AF19	XRAM2_DATA_22	I/O	HSTL	XRAM Data bit
AF20	XRAM2_DK2_N	O	HSTL	XRAM Differential Output clock (bits 18-26)
AF21	XRAM2_DATA_28	I/O	HSTL	XRAM Data bit
AF22	XRAM2_DATA_35	I/O	HSTL	XRAM Data bit (MSB)
AF23	XRAM2_ADDR_0	O	HSTL	XRAM Address bit (LSB)
AF24	XRAM2_ADDR_5	O	HSTL	XRAM Address bit
AF25	XRAM2_ADDR_6	O	HSTL	XRAM Address bit
AF26	XRAM2_ADDR_12	O	HSTL	XRAM Address bit
AF27	XRAM2_ADDR_19	O	HSTL	XRAM Address bit
AF28	TX2_DATA_14_P	O	LVDS/HSTL	Transmit Data bit
AF29	TX2_DATA_14_N	O	LVDS/HSTL	Transmit Data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AF30	TX2_VDD_PST	PWR	2.5V	LVDS 2.5V
AG01	GPIO2_0	I/O	LVCMOS	GPIO data bit
AG02	GPIO2_8	I/O	LVCMOS	GPIO data bit
AG03	GPIO2_3	I/O	LVCMOS	GPIO data bit
AG04	GPIO2_9	I/O	LVCMOS	GPIO data bit
AG05	GPIO2_12	I/O	LVCMOS	GPIO data bit
AG06	GPIO2_17	I/O	LVCMOS	GPIO data bit
AG07	GPIO2_CLK	I/O	LVCMOS	GPIO clock[a]
AG08	GPIO2_29	I/O	LVCMOS	GPIO data bit
AG09	GPIO2_38	I/O	LVCMOS	GPIO data bit
AG10	GPIO2_39	I/O	LVCMOS	GPIO data bit
AG11	GPIO2_46	I/O	LVCMOS	GPIO data bit
AG12	VSS	GND	0V	Core and I/O ground
AG13	XRAM2_DQS2_N	I	HSTL	XRAM Differential Input strobe (bits 18-26)
AG14	XRAM2_DATA_1	I/O	HSTL	XRAM Data bit
AG15	XRAM2_DVLD	I	HSTL	XRAM Data Valid Input This pin should come from the RLDRAM devices associated with XRAM_DATA[8:0].
AG16	XRAM2_DK1_P	O	HSTL	XRAM Differential Output clock (bits 9-17)
AG17	XRAM2_DATA_15	I/O	HSTL	XRAM Data bit
AG18	XRAM2_DATA_19	I/O	HSTL	XRAM Data bit
AG19	XRAM2_DATA_23	I/O	HSTL	XRAM Data bit
AG20	XRAM2_DK3_N	O	HSTL	XRAM Differential Output clock (bits 27-35)
AG21	XRAM2_DATA_29	I/O	HSTL	XRAM Data bit
AG22	XRAM2_DATA_31	I/O	HSTL	XRAM Data bit
AG23	XRAM2_DATA_30	I/O	HSTL	XRAM Data bit
AG24	XRAM2_ADDR_1	O	HSTL	XRAM Address bit
AG25	XRAM2_ADDR_7	O	HSTL	XRAM Address bit
AG26	XRAM2_CLK_N	O	HSTL	XRAM Differential output command clock
AG27	XRAM2_ADDR_20	O	HSTL	XRAM Address bit (MSB)
AG28	VSS	GND	0V	Core and I/O ground
AG29	TX2_DATA_15_P	O	LVDS/HSTL	Transmit Data bit (MSB)
AG30	TX2_DATA_15_N	O	LVDS/HSTL	Transmit Data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AH01	GPIO2_1	I/O	LVCMOS	GPIO data bit
AH02	GPIO2_4	I/O	LVCMOS	GPIO data bit
AH03	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH04	GPIO2_10	I/O	LVCMOS	GPIO data bit
AH05	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH06	GPIO2_25	I/O	LVCMOS	GPIO data bit
AH07	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH08	GPIO2_31	I/O	LVCMOS	GPIO data bit
AH09	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH10	GPIO2_40	I/O	LVCMOS	GPIO data bit
AH11	GPIO2_VDD_PST	PWR	2.5V	Connect to GPIO power (2.5V)
AH12	XRAM2_DQS1_N	I	HSTL	XRAM Differential Input strobe (bits 9-17)
AH13	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH14	XRAM2_DATA_3	I/O	HSTL	XRAM Data bit
AH15	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH16	XRAM2_DK1_N	O	HSTL	XRAM Differential Output clock (bits 9-17)
AH17	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH18	XRAM2_DATA_18	I/O	HSTL	XRAM Data bit
AH19	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH20	XRAM2_DK3_P	O	HSTL	XRAM Differential Output clock (bits 27-35)
AH21	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH22	XRAM2_DATA_33	I/O	HSTL	XRAM Data bit
AH23	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH24	XRAM2_ADDR_2	O	HSTL	XRAM Address bit
AH25	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH26	XRAM2_CLK_P	O	HSTL	XRAM Command clock
AH27	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH28	XRAM2_ADDR_13	O	HSTL	XRAM Address bit
AH29	XRAM2_VDD_PST	PWR	1.8V	Connect to XRAM I/O Power (1.8V)
AH30	XRAM2_ADDR_16	O	HSTL	XRAM Address bit
AJ01	GPIO2_2	I/O	LVCMOS	GPIO data bit
AJ02	GPIO2_5	I/O	LVCMOS	GPIO data bit
AJ03	GPIO2_7	I/O	LVCMOS	GPIO data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AJ04	VSS	GND	0V	Core and I/O ground
AJ05	GPIO2_26	I/O	LVCMOS	GPIO data bit
AJ06	VSS	GND	0V	Core and I/O ground
AJ07	GPIO2_32	I/O	LVCMOS	GPIO data bit
AJ08	VSS	GND	0V	Core and I/O ground
AJ09	GPIO2_42	I/O	LVCMOS	GPIO data bit
AJ10	VSS	GND	0V	Core and I/O ground
AJ11	GPIO2_47	I/O	LVCMOS	GPIO data bit
AJ12	XRAM2_DQS1_P	I	HSTL	XRAM Differential Input strobe (bits 9-17)
AJ13	XRAM2_DQS3_P	I	HSTL	XRAM Differential Input strobe (bits 27-35)
AJ14	XRAM2_DATA_2	I/O	HSTL	XRAM Data bit
AJ15	XRAM2_DATA_8	I/O	HSTL	XRAM Data bit
AJ16	VSS	GND	0V	Core and I/O ground
AJ17	XRAM2_DATA_10	I/O	HSTL	XRAM Data bit
AJ18	VSS	GND	0V	Core and I/O ground
AJ19	XRAM2_DATA_24	I/O	HSTL	XRAM Data bit
AJ20	VSS	GND	0V	Core and I/O ground
AJ21	XRAM2_DATA_26	I/O	HSTL	XRAM Data bit
AJ22	VSS	GND	0V	Core and I/O ground
AJ23	XRAM2_CNTL_1	O	HSTL	XRAM Control bit
AJ24	VSS	GND	0V	Core and I/O ground
AJ25	XRAM2_BANK_1	O	HSTL	XRAM Bank bit
AJ26	VSS	GND	0V	Core and I/O ground
AJ27	XRAM2_ADDR_8	O	HSTL	XRAM Address bit
AJ28	VSS	GND	0V	Core and I/O ground
AJ29	XRAM2_ADDR_14	O	HSTL	XRAM Address bit
AJ30	XRAM2_ADDR_17	O	HSTL	XRAM Address bit
AK01	None	N/A	N/A	No ball
AK02	GPIO2_6	I/O	LVCMOS	GPIO data bit
AK03	GPIO2_13	I/O	LVCMOS	GPIO data bit
AK04	GPIO2_24	I/O	LVCMOS	GPIO data bit
AK05	GPIO2_27	I/O	LVCMOS	GPIO data bit
AK06	GPIO2_30	I/O	LVCMOS	GPIO data bit

Table 11-1 External Pins (Continued)

Pin Number	Signal	Type	Signal Type	Description
AK07	GPIO2_33	I/O	LVCMOS	GPIO data bit
AK08	GPIO2_34	I/O	LVCMOS	GPIO data bit
AK09	GPIO2_41	I/O	LVCMOS	GPIO data bit
AK10	GPIO2_43	I/O	LVCMOS	GPIO data bit
AK11	GPIO2_44	I/O	LVCMOS	GPIO data bit
AK12	VSS	GND	0V	Core and I/O ground
AK13	XRAM2_DQS3_N	I	HSTL	XRAM Differential Input strobe (bits 27-35)
AK14	XRAM2_DATA_5	I/O	HSTL	XRAM Data bit
AK15	XRAM2_DATA_4	I/O	HSTL	XRAM Data bit
AK16	XRAM2_DK0_N	O	HSTL	XRAM Differential Output clock (bits 0-8)
AK17	XRAM2_DK0_P	O	HSTL	XRAM Differential Output clock (bits 0-8)
AK18	XRAM2_DATA_12	I/O	HSTL	XRAM Data bit
AK19	XRAM2_DATA_11	I/O	HSTL	XRAM Data bit
AK20	XRAM2_DATA_25	I/O	HSTL	XRAM Data bit
AK21	XRAM2_DATA_27	I/O	HSTL	XRAM Data bit
AK22	XRAM2_DATA_32	I/O	HSTL	XRAM Data bit
AK23	XRAM2_CNTL_2	O	HSTL	XRAM Control bit
AK24	XRAM2_CNTL_0	O	HSTL	XRAM Control bit
AK25	XRAM2_BANK_2	O	HSTL	XRAM Bank bit
AK26	XRAM2_BANK_0	O	HSTL	XRAM Bank bit
AK27	XRAM2_ADDR_9	O	HSTL	XRAM Address bit
AK28	XRAM2_ADDR_15	O	HSTL	XRAM Address bit
AK29	XRAM2_ADDR_18	O	HSTL	XRAM Address bit
AK30	None	N/A	N/A	No ball

a. 16 mA drive for the GPIO clock

Appendix B: Recommended Heat Sinks

CAUTION: *Always check with the specific heat sink supplier for the latest information on their products. This section may not have the latest information. All names & trademarks are the property of their respective owners.*

Table 12-1 Forced Convection Heat Sink Options

T_J	T_A	Power	qJA	qJC	qCS	Max qSA	Heat Sink Example
°C	°C	watts	°C/watt	°C/watt	°C/watt	°C/watt	
250 LFM							
85	40	10	4.5	0.45	0.1	3.95	ThermaFlo B35351500000
85	40	20	2.25	0.45	0.1	1.7	ThermaFlo EH1126
85	40	25	1.8	0.45	0.1	1.25	ThermaFlo EH1126
85	40	30	1.5	0.45	0.1	0.95	ThermaFlo EH1126
115	40	10	7.5	0.45	0.1	6.95	ThermaFlo B35351500000
115	40	20	3.75	0.45	0.1	3.2	ThermaFlo EH1126
115	40	25	3	0.45	0.1	2.45	ThermaFlo EH1126
115	40	30	2.5	0.45	0.1	1.95	ThermaFlo EH1126
85	55	10	3	0.45	0.1	2.45	ThermaFlo EH1126
85	55	20	1.5	0.45	0.1	0.95	ThermaFlo EH1126
85	55	25	1.2	0.45	0.1	0.65	ThermaFlo P817151B00002
85	55	30	1	0.45	0.1	0.45	Tyco 1-1542007-3
115	55	10	6	0.45	0.1	5.45	ThermaFlo EH1126
115	55	20	3	0.45	0.1	2.45	ThermaFlo EH1126
115	55	25	2.4	0.45	0.1	1.85	ThermaFlo EH1126
115	55	30	2	0.45	0.1	1.45	ThermaFlo EH1126
500 LFM							
85	40	10	4.5	0.45	0.1	3.95	ThermaFlo B35351500000
85	40	20	2.25	0.45	0.1	1.7	ThermaFlo EH1126
85	40	25	1.8	0.45	0.1	1.25	ThermaFlo EH1126
85	40	30	1.5	0.45	0.1	0.95	ThermaFlo EH1126
115	40	10	7.5	0.45	0.1	6.95	ThermaFlo B35351500000
115	40	20	3.75	0.45	0.1	3.2	ThermaFlo EH1126

Table 12-1 Forced Convection Heat Sink Options (Continued)

T_J	T_A	Power	qJA	qJC	qCS	Max qSA	Heat Sink Example
°C	°C	watts	°C/watt	°C/watt	°C/watt	°C/watt	
115	40	25	3	0.45	0.1	2.45	ThermaFlo EH1126
115	40	30	2.5	0.45	0.1	1.95	ThermaFlo EH1126
85	55	10	3	0.45	0.1	2.45	ThermaFlo EH1126
85	55	20	1.5	0.45	0.1	0.95	ThermaFlo EH1126
85	55	25	1.2	0.45	0.1	0.65	ThermaFlo EH1126
85	55	30	1	0.45	0.1	0.45	ThermaFlo P817151B00002
115	55	10	6	0.45	0.1	5.45	ThermaFlo EH1126
115	55	20	3	0.45	0.1	2.45	ThermaFlo EH1126
115	55	25	2.4	0.45	0.1	1.85	ThermaFlo EH1126
115	55	30	2	0.45	0.1	1.45	ThermaFlo EH1126
750 LFM							
85	40	10	4.5	0.45	0.1	3.95	ThermaFlo B35351500000
85	40	20	2.25	0.45	0.1	1.7	ThermaFlo EH1126
85	40	25	1.8	0.45	0.1	1.25	ThermaFlo EH1126
85	40	30	1.5	0.45	0.1	0.95	ThermaFlo EH1126
115	40	10	7.5	0.45	0.1	6.95	ThermaFlo B35351500000
115	40	20	3.75	0.45	0.1	3.2	ThermaFlo EH1126
115	40	25	3	0.45	0.1	2.45	ThermaFlo EH1126
115	40	30	2.5	0.45	0.1	1.95	ThermaFlo EH1126
85	55	10	3	0.45	0.1	2.45	ThermaFlo EH1126
85	55	20	1.5	0.45	0.1	0.95	ThermaFlo EH1126
85	55	25	1.2	0.45	0.1	0.65	ThermaFlo EH1126
85	55	30	1	0.45	0.1	0.45	ThermaFlo EH1127
115	55	10	6	0.45	0.1	5.45	ThermaFlo EH1126
115	55	20	3	0.45	0.1	2.45	ThermaFlo EH1126
115	55	25	2.4	0.45	0.1	1.85	ThermaFlo EH1126
115	55	30	2	0.45	0.1	1.45	ThermaFlo EH1126
1000 LFM							
85	40	10	4.5	0.45	0.1	3.95	ThermaFlo B35351500000

Table 12-1 Forced Convection Heat Sink Options (Continued)

T_J	T_A	Power	qJA	qJC	qCS	Max qSA	Heat Sink Example
°C	°C	watts	°C/watt	°C/watt	°C/watt	°C/watt	
85	40	20	2.25	0.45	0.1	1.7	ThermaFlo EH1126
85	40	25	1.8	0.45	0.1	1.25	ThermaFlo EH1126
85	40	30	1.5	0.45	0.1	0.95	ThermaFlo EH1126
115	40	10	7.5	0.45	0.1	6.95	ThermaFlo B35351500000
115	40	20	3.75	0.45	0.1	3.2	ThermaFlo EH1126
115	40	25	3	0.45	0.1	2.45	ThermaFlo EH1126
115	40	30	2.5	0.45	0.1	1.95	ThermaFlo EH1126
85	55	10	3	0.45	0.1	2.45	ThermaFlo EH1126
85	55	20	1.5	0.45	0.1	0.95	ThermaFlo EH1126
85	55	25	1.2	0.45	0.1	0.65	ThermaFlo EH1126
85	55	30	1	0.45	0.1	0.45	ThermaFlo EH1126
115	55	10	6	0.45	0.1	5.45	ThermaFlo EH1126
115	55	20	3	0.45	0.1	2.45	ThermaFlo EH1126
115	55	25	2.4	0.45	0.1	1.85	ThermaFlo EH1126
115	55	30	2	0.45	0.1	1.45	ThermaFlo EH1126

Table 12-2 Natural Convection Heat Sink Options

T_J	T_A	Power	qJA	qJC	qCS	Max qSA	Heat Sink Example
°C	°C	watts	°C/watt	°C/watt	°C/watt	°C/watt	
85	40	10	4.5	0.45	0.1	3.95	ThermaFlo E3180
85	40	20	2.25	0.45	0.1	1.7	ThermaFlo E3180
85	40	25	1.8	0.45	0.1	1.25	ThermaFlo E3180
85	40	30	1.5	0.45	0.1	0.95	Active or Custom Passive
115	40	10	7.5	0.45	0.1	6.95	ThermaFlo E3180
115	40	20	3.75	0.45	0.1	3.2	ThermaFlo E3180
115	40	25	3	0.45	0.1	2.45	ThermaFlo E3180
115	40	30	2.5	0.45	0.1	1.95	ThermaFlo E3180

Table 12-2 Natural Convection Heat Sink Options (Continued)

T_J	T_A	Power	qJA	qJC	qCS	Max qSA	Heat Sink Example
°C	°C	watts	°C/watt	°C/watt	°C/watt	°C/watt	
85	55	10	3	0.45	0.1	2.45	ThermaFlo E3180
85	55	20	1.5	0.45	0.1	0.95	Active or Custom Passive
85	55	25	1.2	0.45	0.1	0.65	Active or Custom Passive
85	55	30	1	0.45	0.1	0.45	Active or Custom Passive
115	55	10	6	0.45	0.1	5.45	ThermaFlo E3180
115	55	20	3	0.45	0.1	2.45	ThermaFlo E3180
115	55	25	2.4	0.45	0.1	1.85	ThermaFlo E3180
115	55	30	2	0.45	0.1	1.45	ThermaFlo E3180

Appendix C: Periphery Object Naming Convention

The hardware and the software have different naming conventions when describing the periphery. The Data Sheet describes the periphery pinouts in terms of numeric values (e.g. XRAM1, XRAM2) whereas the COAST software describes the periphery objects in terms of their position on the grid (e.g. xram_9_n, xram_9_s). In order to reconcile these differences, the following table can be used:

Table 13-1 Periphery Object Naming Convention

#	Location in Periphery	Pinout Notation	COAST Notation
XRAM			
1	North side	XRAM1_*	xram_9_n
2	South side	XRAM2_*	xram_9_s
GPIO			
1	North side	GPIO1_*	gpio_11_n
2	South side	GPIO2_*	gpio_11_s
RX			
1	East side	RX1_*	rx_e_5
2	West side	RX2_*	rx_w_13
TX			
1	East side	TX1_*	tx_e_13
2	West side	TX2_*	tx_w_5
IRAM			
1	North side, east-most	N/A	iram_18_n
2	North side	N/A	iram_16_n
3	North side	N/A	iram_13_n
4	North side	N/A	iram_7_n
5	North side	N/A	iram_4_n
6	North side, west-most	N/A	iram_1_n
7	South side, east-most	N/A	iram_18_s
8	South side	N/A	iram_16_s
9	South side	N/A	iram_13_s
10	South side	N/A	iram_7_s

Table 13-1 Periphery Object Naming Convention (Continued)

#	Location in Periphery	Pinout Notation	COAST Notation
11	South side	N/A	iram_4_s
12	South side, west-most	N/A	iram_1_s
Control Object			
1	West side	N/A	fpoa_control_w_19