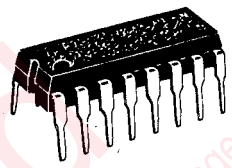
MN4021B/MN4021BS

8-Bit Static Shift Register

■ Outline

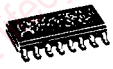
The MN4031B/S consisting of eight register cells which respectively have parallel inputs is an 8-bit static shift register to enable both clock synchronizing series input/series output conversion and parallel input/series output conversion by control of the parallel/series control input (PL).

P-3



16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

■ Trush Table

Serial operation

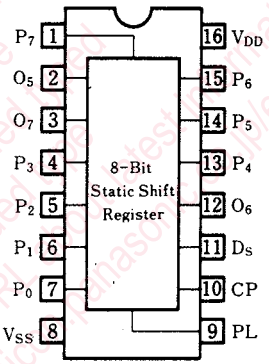
	Input			Output		
n	CP	Ds	PL	O_5	O_6	O_7
1	↑	D_1	L	×	×	×
2	↑	D_2	L	×	×	×
3	↑	D_3	L	×	×	×
6	↑	×	L	D_1	×	×
7	↑	×	L	D_2	D_1	×
8	↑	×	L	D_3	D_2	D_1
	↓	×	L	no change		

Parallel operation

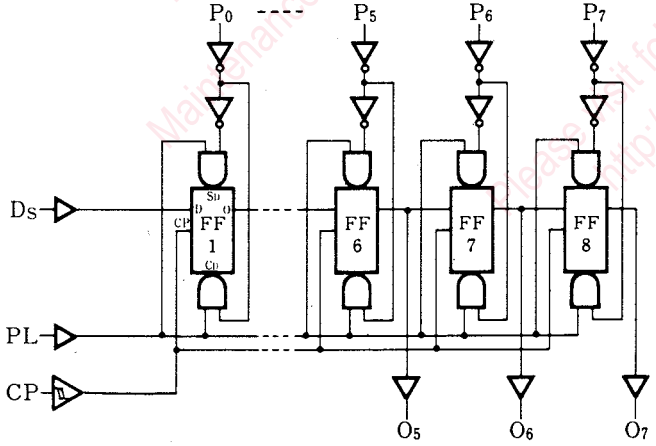
	Input			Output		
n	CP	Ds	PL	O_5	O_6	O_7
	×	×	H	P_5	P_6	P_7

Note) × : don't care
Dn : H or L
n : Number of clock pulse

Pin Configuration



■ Logic Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.5～+18	V
Input voltage		V_I	−0.5～V_{DD}+0.5*	V
Output pin voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=−40～+60°C	P_D	max. 400	mW
	Ta=+60～+80°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	−40～+85	°C
Storage temperature		T_{stg}	−65～+150	°C

* V_{DD}+0.5V should be lower than 18V.

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Condition		Ta=−40°C min.	Ta=−40°C max.	Ta=25°C min.	Ta=25°C max.	Ta=85°C min.	Ta=85°C max.	Unit
Static supply current	5	I_{DD}	$V_I=V_{SS}$ or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output voltage low level	5	V_{OL}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V_{OH}	$V_I=V_{SS}$ or V_{DD}, $\|I_O\|<1\mu A$		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V_{IL}	$\|I_O\|<1\mu A$	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input voltage high level	5	V_{IH}	$\|I_O\|<1\mu A$	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output current low level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

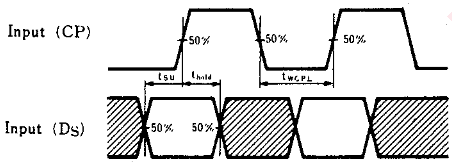
■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	

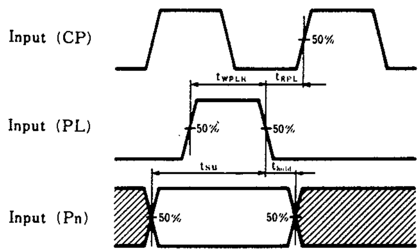
■ Switching Characteristics (cont.)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Propagation time CP→On (H→L)	5	t_{PHL}	—	170	510	ns
	10		—	65	195	
	15		—	45	135	
Propagation time CP→On (L→H)	5	t_{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation time PL→On (H→L)	5	t_{PHL}	—	240	720	ns
	10		—	90	270	
	15		—	60	180	
Propagation time PL→On (L→H)	5	t_{PLH}	—	175	525	ns
	10		—	70	210	
	15		—	50	150	
Set-up time D_S→CP	5	t_{su}	—	45	135	ns
	10		—	15	45	
	15		—	10	30	
Set-up time Pn→PL	5	t_{su}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Hold time D_S→CP	5	t_{hold}	—	20	60	ns
	10		—	10	30	
	15		—	8	24	
Hold time Pn→PL	5	t_{hold}	—	−10	24	ns
	10		—	0	24	
	15		—	0	24	
Minimum clock pulse width	5	t_{WCPL}	—	55	165	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL pulse width	5	t_{WPLH}	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
PL recovery time	5	t_{RPL}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Maximum clock frequency	5	f_{max}	4	9	—	MHz
	10		12	25	—	
	15		18	37	—	
Input capacitance		C_I	—	—	7.5	pF

- Switching waveforms



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D_S.



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

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