□ MN103S33N

Туре		MN103S33N
Command ROM	l (×64-bit)	512 K-byte
Data RAM (×32	-bit)	24 K-byte
Package		MBGA360-C-1313A *Lead-free
Minimum Instru Execution Time		24.3 ns (at 2.3 V to 2.7 V, 41 MHz)
Interrupts		• RESET • IRQ × 15 • NMI • Key input • Timer × 44 • Input capture × 16 • PWM × 8 • SIF × 25 • DMA × 12 • WDT • A/D • System error
Timer Counter	•	8-bit timer × 12 Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer)
		8-bit timer with PWM × 8 Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) PWM generating function
		Reload-down count Cascade connection possible (usable as a 16-bit to 32-bit timer) PWM generating function 16-bit timer × 6 Up-down count Input capture function PWM generating function Compare/capture register 2-ch. 16-bit timer × 6 Reload-down count Watchdog timer × 1 Number of channels. 4 Unit of transfer: 8/16/32 bits Max. Transfer cycles: 65535
	•	16-bit timer × 6 Reload-down count Watchdog timer × 1 about to the second seco
DMA Controller	2	Number of channels: 4 Unit of transfer: 8/16/32 bits Max. Transfer cycles: 65535 Staring factor: external interrupt, timer factor, PWM factor, serial transmission/reception factor, A/D conversion finish, software factor Transfer method: 2-bus cycle transfer
		Adressing modes: fixed, increment, decrement Transfer modes: word transfer, burst transfer, intermittent transfer
Serial Interface		Serial 0, 1, 3 to 8, A, B: start-stop synchronization/synchronization/I ² C commonly used, 10 lines Serial 2, 9: 2 lines for start-stop synchronization only, serial 2: 10 bytes containing receive FIFO
I/O Pins	I/O	169 Common use
	Input	25 • Common use
A/D Inputs		10-bit × 25-ch.
PWM		12-, 14-bit resolution \times 5-ch. output waveform value load control function provided 16-bit resolution \times 2-ch.
ICR		28-bit × 13-ch. + 16-bit × 6-ch. (common with timer)
OCR		16-bit × 12-ch. (common with timer)
Timer Synchro	nous Output	4-bit (synchronous output) × 2-ch.
ROM Collection	-	4-ch.

Panasonic

Pin Assignment

								Pe	rspect ↓	ive								
N.D.	N.D.	TDI	PF3, TM25IOB	PF1, TM24IOB	VDD2	PD5, TM15IO	PD2, TM12IO	PC6, SY1OT2, SBT8	PC4, SY1OT0, SBI8	VSS	PB2, IRQ14	PA2, SBT6	P91, ICR9	P87, ICR7	P83, ICR3	P81, ICR1	N.D.	N.D.
N.D.	N.D.	TCK	PF2, TM25IOA	PE0, TM20IOA	PE5, TM22IOB	PE3, TM21IOB	PD3, TM13IO	VDD2	PC2, SY0OT2	PB4, BR	PA4, SBO7	PA0, SBI6	VSS	P85, ICR5	P60, IRQ8	P80, ICR0	N.D.	N.D.
TDO	PV2, SBTA	PV1, SBOA	PE6, TM23IOA	PE2, TM21IOA	PD4, TM14IO	PD1, TM11IO	PC7, SY1OT3	PC1, SY0OT1	PB5, BG	PB1, IRQ13	PA5, SBT7	PA3, SBI7	P92, ICR10	P86, ICR6	vss	P62, IRQ10	P63, IRQ11	P61, IRQ9
PV0, SBIA	PG6, AN6	VREFL	TMS	PF0, TM24IOA	PE4, TM22IOA	PE7, TM23IOB	PE1, TM20IOB	PD0, TM10IO	PC0, SY0OT0	PB0, IRQ12	P93, ICR11	P94, ICR12	VDD2	P82, ICR2	P84, ICR4	P54, IRO4	P33, D27, SBT2	N.C.*2 (VDDF)
PV3,	vss	PG2, AN2	VDD	TRST	N.D.	VDD	N.C.*1 (VSS)	VSS	PC5, SY1OT1, SBO8	PC3, SY0OT3	PB3, WDOVF	PA1, SBO6	N.C.*1 (VSS)	P90, ICR8	P56, IRQ6	P34, D28, SBI3	P25, D21, SBT0	P57, IRQ7
PG3, AN3	AVDD	PG4, AN4	VREFH	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P52, IRQ2	P43, PWM4	P53, IRQ3	P51, IRQ1
PG7, AN7	PG5, AN5	PH2, AN10	PG1, AN1	PG0, AN0	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P50, IRQ0	P55, IRQ5	P41, PWM2, TM1IO	vss	P40, PWM1, TM0IO
PH5, AN13	PH3, AN11	PH4, AN12	PH1, AN9	PH0, AN8	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P36, D30, SBT3	P42, PWM3, TM2IO	P37, D31, PWM0	VDDH	P35, D29, SBO3
PI5, AN21	PI3, AN19	PH7, AN15	PI1, AN17	PI0, AN16	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P27, D23, SBO1	VSS	P31, D25, SBI2	P32, D26, SBO2	P30, D24, SBT1
AVSS	PI7, AN23	PH6, AN14	PI4, AN20	PI6, AN22	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P21, D17, SBOB	P24, D20, SBO0	P23, D19, SBI0	P22, D18, SBTB	P26, D22, SB11
VSS	PM1, CS1	PI2, AN18	VDDB	P70, AN24	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P12, D10	P16, D14	N.C.*1 (VSS)	P20; D16, SBIB	vss
PM3, CS3	PN0, WE0, SDQM0	$\frac{PM0}{CS0}$	PM4, CS4	VSS	N.D.	N.D.	N.D.	N.D.	N.Đ.	N.D.	N.D.	N.D.	N.D.	P10	VDDH	D15	P13, D11	N.C.*2 (VDDF)
PN2, YSCLK	VSS	PM5, RWSEL	PN4,	VDD	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	P02, D2	Vss	P15, D13	P07, D7	P11, D9
PO0, ADM0, A0	VDD	$\frac{PM2}{CS2}$	PŃ5, AS	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D	N.D.	Vss	P00, D0	P06, D6	P03, D3	P05, D5
VDDB	PO5, ADM5, A5	PN1, WE1, SDQM1	PO1, ADM1, A1	VSS	N.D.	PVSS	MMOD1	VSS	РК3, ТМ33ІО	PL2, TM5IO	PR1, A20, K11	PR7, KI7, PWM5	n (D.	PT1, SBO9	VOUT	P04, D4	P14, D12	P01, D1
PO3, ADM3, A3	PO2, ADM2, A2	PN3,	PO7, ADM7, A7	vss	RST	VDDH	CKSEL	VDD	PK4, TM34IO	PL3. TM6IO	PR2; A21, <u>KI2,</u> SWE	PS0 SBI4	vss	PS5, SBT5	PS3, SBI5	VDDH	VOUT	electrode (pin) none
PO6, ADM6, A6	VDDB	PP2, ADM10, A10	PO4, ADM4, A4	PP4, ADM12, A12	PK1, TM31IO	PK5, TM35IO	РК7, ТМ37Ю	PK0, TM30IO	PL1, TM410	PL4, TM7IO	PQ0,	PQ2, A18	VDDH	PR4, A23, KI4, SDCLKO	PU0, WE2, SCAS	NMIRQ	VDDH	VSS
N.D.	N.D.	PP6, ADM14, A14	PJ0, EXMOD0	ADM11, A11	PP7, ADM15, A15	рл, exmodi	FRQS	РК2, ТМ32Ю	PK6, TM36IO	PL 5. PWM6	PR0, A19, KI0	PR5, A24, KI5, SDCLKI	PS2, SBT4	PT0, SBI9	PS1, SBO4	LON	N.D.	N.D.
N.D.	N.D.	PP0, ADM8, A8	PP1, ADM9, A9	PP5, ADM13, A13	PVDD	MMOD0	osco	OSCI	PL0, TM3IO	vss	PQ1, A17	PR3, A22, KI3, SCKE	PR6, A25, KI6	PS4, SBO5	PT2, SBT9	PU1, WE3, SRAS	N.D.	N.D.
19	18	17	16	15	14	13	42		90	9	8	7	6	5	4	3	2	1

* N.D. has an electrode (pin) but N.C. is not quaranteed. Please design so as not to cause short circuit with other wiring on the user board.

* Each of VDDH, VDD, VDDB, VDDF, VDD2, and VSS has multiple electrodes (pins). Connect the same electrode names to the same power supply.

*1: Connect the J3, R6, and R12 pins to the VSS for the MN103SF33N.

*2: Connect the H1 and T1 pins to the VDDF power for the MN103SF33N.

Support Tool

	PX-ICE103S33	Not applicable to MBGA360-C-1313A
n-board Development Tools	PX-ODB103S-O	
lash Memory Built-in Type	Туре	MN103SF33N
	Command ROM (× 64-bit)	512 K-byte
	Data RAM (× 32-bit)	24 K-byte
	Minimum instruction execution time	24.3 ns (at 2.3 V to 2.7 V, 41 MHz)
	Package	MBGA360-C-1313A *Lead-free
		URL about latest information.

MN103S33N 🗆



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