MN103L09/10/11/12/13/14/15/16/17/18/19/20/21/22/23/24/25/26/27 Series

32-bit Single-chip Microcontroller

■ Overview

The MN103LF series of 32-bit single-chip microcomputers have multiple types of peripheral functions. This LSI series is well suited for camera, TV, VCR, AV, printer, telephone, FAX machine, air-conditioner, music instrument and other applications.

This LSI series has flexible and optimized hardware configurations and simple efficient instruction set. This LSI series incorporates an internal ROM of 1048 KB (maximum) and RAM of 76 KB (maximum), 11 external interrupts, 96 internal interrupts including non-maskable interrupt, 26 timer counters, 14 sets of serial interfaces, A/D converter, D/A converter, 2 sets of watchdog timer, DMA, CAN, and IEBus interface.

In addition, this LSI series has 5 oscillation circuits (external high frequency: 4 MHz to 20 MHz/ external low frequency:32.768 kHz/ internal high frequency: 20 MHz/ internal low frequency: 30 kHz/ PLL: frequency multiplier of high or low frequency).
The internal clock can be switched to four oscillation clock except the internal low oscillation. The internal clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming.

A machine cycle (minimum instruction execution time) is 25 ns (internal operating condition: 1.8 V, 40 MHz).

■ Product Summary

This datasheet describes the following model.

Series	Model	Pin Number	ROM Size	RAM Size *1	In-vehicle LAN	Package
MN103L09	MN103LF09R	144	1048 KB	76 KB	CAN/IEBus	LQFP144-P-2020D
	MN103LF09Q		792 KB			
MN103L10/ MN103L13	MN103LF13R	100	1048 KB	76 KB	IEBus	LQFP100-P-1414C
	MN103LF13Q		792 KB			
	MN103LF10R		1048 KB	64 KB		
	MN103LF10Q		792 KB			
	MN103LF10N		536 KB	40 KB		
	MN103LF10M		408 KB	32 KB		
	MN103LF10K		280 KB	20 KB		
MN103L11/ MN103L14	MN103LF14R	128	1048 KB	76 KB		LQFP128-P-1818F
	MN103LF14Q		792 KB			
	MN103LF11R		1048 KB	64 KB		
	MN103LF11Q		792 KB			
	MN103LF11N		536 KB	40 KB		
	MN103LF11M		408 KB	32 KB		
	MN103LF11K		280 KB	20 KB		
MN103L12/ MN103L15	MN103LF15R	144	1048 KB	76 KB		LQFP144-P-2020D
	MN103LF15Q		792 KB			
	MN103LF12R		1048 KB	64 KB		
	MN103LF12Q		792 KB			
	MN103LF12N		536 KB	40 KB		
MN103L16/ MN103L19	MN103LF19R	100	1048 KB	76 KB	—	LQFP100-P-1414C
	MN103LF19Q		792 KB			
	MN103LF16R		1048 KB	64 KB		
	MN103LF16Q		792 KB			
	MN103LF16N		536 KB	40 KB		
	MN103LF16M		408 KB	32 KB		
	MN103LF16K		280 KB	20 KB		

Note) *1: When using On-Chip Debug function, the debugger take over 500 Byte in size

■ Product Summary (continued)

This datasheet describes the following model.

Series	Model	Pin Number	ROM Size	RAM Size *1	In-vehicle LAN	Package
MN103L17/ MN103L20	MN103LF20R	128	1048 KB	76 KB	—	LQFP128-P-1818F
	MN103LF20Q		792 KB			
	MN103LF17R		1048 KB	64 KB		
	MN103LF17Q		792 KB			
	MN103LF17N		536 KB	40 KB		
	MN103LF17M		408 KB	32 KB		
	MN103LF17K		280 KB	20 KB		
MN103L18/ MN103L21	MN103LF21R	144	1048 KB	76 KB		LQFP144-P-2020D
	MN103LF21Q		792 KB			
	MN103LF18R		1048 KB	64 KB		
	MN103LF18Q		792 KB			
	MN103LF18N		536 KB	40 KB		
MN103L22/ MN103L25	MN103LF25R	100	1048 KB	76 KB	CAN	LQFP100-P-1414C
	MN103LF25Q		792 KB			
	MN103LF22R		1048 KB	64 KB		
	MN103LF22Q		792 KB			
	MN103LF22N		536 KB	40 KB		
	MN103LF22M		408 KB	32 KB		
	MN103LF22K		280 KB	20 KB		
MN103L23/ MN103L26	MN103LF26R	128	1048 KB	76 KB		LQFP128-P-1818F
	MN103LF26Q		792 KB			
	MN103LF23R		1048 KB	64 KB		
	MN103LF23Q		792 KB			
	MN103LF23N		536 KB	40 KB		
	MN103LF23M		408 KB	32 KB		
	MN103LF23K		280 KB	20 KB		
MN103L24/ MN103L27	MN103LF27R	144	1048 KB	76 KB		LQFP144-P-2020D
	MN103LF27Q		792 KB			
	MN103LF24R		1048 KB	64 KB		
	MN103LF24Q		792 KB			
	MN103LF24N		536 KB	40 KB		

Note) *1: When using On-Chip Debug function, the debugger take over 500 Byte in size

■ Features

- CPU core

MN103L core (The instruction set is compatible MN103S series)
Memory space 4 GB (instruct/data common use)
LOAD-STORE architecture (3-stage pipeline)
Machine cycle
High-speed mode 25 ns/ 40 MHz (Max)
Low-speed mode 30.3 μs/ 33 kHz (Max)

- Operation mode

NORMAL mode (CPU clock operation, Peripheral circuit clock operation mode)
SLOW mode (CPU clock operation, Peripheral circuit clock operation mode)
HALT mode (CPU clock stop, Peripheral circuit clock operation mode)
STOP mode (All clocks stop mode)

- Clock oscillation circuit : 5 circuits

External high-speed oscillation (clkosc) : Crystal oscillator/ Ceramic oscillator
: 4 MHz to 20 MHz
External low-speed oscillation (clkx) : Crystal oscillator/ Ceramic oscillator
: 32.768 kHz
Internal high-speed oscillation (clkrc) : 20 MHz
Internal low-speed oscillation (clkrcx) : 30 kHz
PLL output (clkpll) : 60 MHz to 120 MHz

- Clock multiple circuit (PLL)

Multiplication rate : 4, 6, 8, 10, 12, 16, 20 multiplied clock of clkoscsel
2440 to 3660 multiplied clock of clkx
Clock dividing : 2, 3 divided of clkpll
PLL output dividing clock : 20 MHz to 40 MHz (clkplldiv)

- Internal operation clock: 6 types

CPU clock (clkcpu)
Frequency : 40 MHz (Max)
Clock source : clkplldiv, clkosc, clkrc, clkx
Clock dividing : 1, 2, 4, 8, 16, 32, 64 divided of clock source
Peripheral bus clock (clkbus)
Frequency : 20 MHz (Max)
Clock source : clkplldiv, clkosc, clkrc, clkx
Clock dividing : 2, 4, 8, 16, 32, 64, 128 divided of clock source
(This setting is independent from the dividing clock setting of clkcpu. Set the frequency of clkbus to less than clkcpu.)
Peripheral high-speed clock (clksp)
Frequency : 22 MHz (Max)
Clock source : clkrc, clkosc, clkplldiv
Clock dividing : 1, 2, 4, 8, 16 divided of clock source
High-speed oscillation clock (clkoscsel)
Frequency : 22 MHz (Max)
Clock source : clkrc, clkosc
Internal low-speed oscillation clock (clkrcx)
Frequency : 33 kHz (Max)
Low-speed oscillation clock (clksx)
Frequency : 33 kHz (Max)
Clock source : clkrcx, clkxsel

■ Features (continued)

- Bus interface

Bus area : 2 MB × 2 banks
Data bus : 8/ 16 bits

- DMA Controller

Transfer area : Internal ROM space / Internal RAM space / Internal I/O area / External memory space
↔ Internal ROM space / Internal RAM space / Internal I/O area / External memory space
Channel : 4 ch
Transfer form : 2 bus cycles transfer
Transfer requests
MN103LF09 series : 75 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3, A/D converter:1, CAN controller:1, IEBus controller:2, Software:1)
MN103LF10/11/12/13/14/15 series : 74 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3, A/D converter:1, IEBus controller:2, Software:1)
MN103LF22/23/24/25/26/27 series : 73 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3, A/D converter:1, CAN controller:1, Software:1)
MN103LF16/17/18/19/20/21 series : 72 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3, A/D converter:1, Software:1)
Transfer modes : 3 modes (One word transfer / Burst transfer / Intermittent transfer)

- Interrupt functions

Internal interrupts
MN103LF09 series : 97 factors
(Timer:46, Serial I/F:22, IIC:6, Watchdog timer:1, DMA:12, A/D converter:1, CAN controller: 1, LIN controller: 1, IEBus controller: 4, Power Voltage Detection: 2, System error:1)
MN103LF10/11/12/13/14/15 series : 96 factors
(Timer:46, Serial I/F:22, IIC:6, Watchdog timer:1, DMA:12, A/D converter:1, LIN controller: 1, IEBus controller: 4, Power Voltage Detection: 2, System error:1)
MN103LF22/23/24/25/26/27 series : 93 factors
(Timer:46, Serial I/F:22, IIC:6, Watchdog timer:1, DMA:12, A/D converter:1, CAN controller: 1, LIN controller: 1, Power Voltage Detection: 2, System error:1)
MN103LF16/17/18/19/20/21 series : 92 factors
(Timer:46, Serial I/F:22, IIC:6,Watchdog timer:1, DMA:12, A/D converter:1, LIN controller: 1, Power Voltage Detection: 2, System error:1)
External interrupts : 11 factor
(IRQn pin(n = 0 to 8) : 9, NMIRQ pin(sharing pin with IRQ7 as an interrupt factors) :1, Key input:1)

- Watchdog Timer

Watchdog Timer
On detection of error, hardware reset is done inside the LSI
(Non-maskable interrupt is generated by the first watchdog time-out event, and hardware reset is done by a series of two time-out events)
Time-out cycle : CPU clock cycle × N (N = 2^{16}, 2^{18}, 2^{20}, 2^{27})
Watchdog Timer2
On detection of error, hardware reset is done inside the LSI
(Non-maskable interrupt is generated by the first watchdog time-out event, and hardware reset is done by a series of two time-out events)
Time-out cycle : Internal low-speed oscillation clock cycle × N (N = 2^4, 2^5, 2^6, 2^7, 2^8, 2^9, 2^{10}, 2^{11}, 2^{12}, 2^{13}, 2^{14}, 2^{15})

■ Features (continued)

- Timer counter : 26 units

8-bit timer : 8 units
8-bit simple timer : 5 units
8-bit free-running timer : 1 unit
16-bit timer : 10 units
Motor control 16-bit timer : 1 unit
24H 8-bit timer : 1 unit

Timer 0 (8-bit timer)
Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed), compare register with double buffer
Clock source: clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 1 (8-bit timer)
Timer count (Up count), external event count, timer pulse output,
16-bit cascade connection (to timer 0), compare register with double buffer
Clock source: clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 2 (8-bit timer)
Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed), 24-bit cascade connection (to timer 0, timer 1), compare register with double buffer
Clock source: clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 3 (8-bit timer)
Timer count (Up count), external event count, timer pulse output,
16-bit cascade connection (to timer 2), 32-bit cascade connection (to timer 0, timer 1, timer 2), compare register with double buffer
Clock source: clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 4 (8-bit timer)
Timer count (Up count), external event count, timer pulse output, PWM output (Cycle is fixed)
Clock source: clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128, clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 20 (8-bit timer)
Timer count (Up count), external event count, timer pulse output, PWM output (Cycle is fixed)
Clock source: clksp, clksp/4, clksp/16, clksp/32, clksp/64, clkbus/2, clkbus/4, clksx, external clock

Timer 21 (8-bit timer)
Timer count (Up count), timer pulse output, timer output for VFD
Clock source: clkbus/2, clkbus/4, clkbus/16, clkbus/32, clkbus/64, clkbus/128

Timer 22 (8-bit timer)
Timer count (Up count), external event count, timer pulse output, PWM output (Cycle is fixed)
Clock source: clksp, clksp/4, clksp/16, clksp/32, clksp/64, clkbus/2, clkbus/4, clksx, external clock

Timer 6 (8-bit free-running timer)
Clock source: clksp, clkbus, clksx, clksp/2^{12}, clksp/2^{13}, clksx/2^{12}, clksx/2^{13}

Timer 7 (16-bit timer)
Timer count (Up count), external event count, timer pulse output,
PWM output (cycle/duty continuous changeable), input capture (1 system)
Clock source: clksp, clksp/2, clksp/4, clksp/16, clkbus/2, clkbus/4, clkbus/16, external clock

■ Features (continued)

- Timer counter (continued)

Timer 8, 9, 10, 11, 12, 13, 14, 15, 16 (16-bit timer)

Timer count (Up count, Down count), external event count, timer pulse output,
PWM output (cycle/duty continuous changeable), input capture (2 system), 2 phases encoder
Clock source: clkbus, clkbus/8, timer 0 or 1 compare match cycle, external clock

Timer M (Motor control 16-bit timer)

Timer pulse output, external event count, complementary 3 phases PWM output (triangular wave and saw-tooth wave output, dead time insertion),
Output control by external interrupt (Hi-Z output or output data is fixed)
Clock source: clksp, clkbus, external clock divided by 1, 2, 4 or 16

Timer A, B, C, D, E (8-bit simple timer)

Serial transfer base clock generation
Clock source: clksp, clksp/2, clksp/4, clksp/8, clksp/16, clksp/32, clkbus/2, clkbus/4

24H Timer

Alarm function, Interval function
Clock source: clksx, clksp (Only when CPU stop)

- Serial interface : 14 channels

UART/ Clock Synchronous : 11 channels
IIC : 3 channels

Serial 0 (UART / Clock Synchronous / LIN)

UART
Parity check, overrun error/frame error detection,
Transfer size can be selected from 7 to 8 bits.

Clock Synchronous
The communication type can be selected from 2-ware or 3-wire.
First tansfer bit can be selected from MSB or LSB.
Arbitrary size of 2 to 8 bits are selectable.
Continuous transmission, continuous reception, continuous transmission/reception are available.
Synchronous edge selection of transfer clock.
Maximum transfer rate: 3.3 Mbps

LIN
Operate in conjunction with Timer 0, 7 and 8.
Master communication.
Synch Break field transmission, Check sum arithmetic
Slave communication
Wake-up reception, Synch Break field reception, Synch field reception, Check sum arithmetic
Error detection
Check sum error, Bit error

Clock source: Baud Rate Timer B0 output, external clock

■ Features (continued)

- Serial interface (continued)

Serial 1, 2, 3, 4, 9, 10 (UART / Clock Synchronous)

UART

Parity check, overrun error/frame error detection,

Transfer size can be selected from 7 to 8 bits.

Clock Synchronous

The communication type can be selected from 2-ware or 3-wire.

First tansfer bit can be selected from MSB or LSB.

Arbitrary size of 2 to 8 bits are selectable.

Continuous transmission, continuous reception, continuous transmission/reception are available.

Synchronous edge selection of transfer clock.

Maximum transfer rate: 3.3 Mbps

Clock source: Baud Rate Timer Bn output (n = 1 to 4, 9, 10), external clock

Serial 5, 6, 7, 8 (UART / Clock Synchronous)

UART

Parity check, overrun error/frame error detection.

Transfer size can be selected from 7 to 8 bits.

Clock Synchronous

The communication type can be selected from 2-ware or 3-wire. (Data input from SBO pin is prohibited)

First tansfer bit can be selected from MSB or LSB.

Arbitrary size of 7 to 8 bits are selectable. (When selection size is 7 bits, first transfer bit setting is LSB only.)

Continuous transmission, continuous reception, continuous transmission/reception are available.

Maximum transfer rate: 3.3 Mbps

Clock source: Output of timer A, B, C, D, E divided by 2, 16.

External clock

IIC 0, 1, 2 (Multi master IIC)

Multi master IIC

100 kHz/ 400 kHz communication is supported.

7-bit, 10-bit slave address is settable.

General call communication mode is supported.

Clock source: Baud Rate Timer BIn output (n = 0 to 2), external clock

- A/D converter

Resolution : 10 bit

Channel : 16 channels

Clock source : clkbus/2, clkbus/4, clkbus/8, clkbus/16, clksx × 2

- D/A converter

Resolution : 10-bit

Unit : 2 units

- Auto reset

Auto reset function can be selected ON/OFF

- Power supply voltage detection circuit

Detection voltage can be set 2.6 V to 4.0 V by software

- Clock monitoring function

Frequency error detection of external / PLL clock

Hardware reset or non-maskable interrupt generation can be selected by program when a frequency error is detected.

■ Features (continued)

- LED driver: 8 sets

- CAN controller (MN103LF09/22/23/24/25/26/27 series only)

Channels	: 1 channel
	CAN 2.0B specification basis
Communication method	: NRZ (Non-Return to Zero)
Transmission line	: 2-wire serial communication
Communication channel	: Max 1 Mbps
Data length	: 0 to 8 byte
Message frame	: Standard frame and extended frame are supported
	(Standard frame format ID: 11 bits, Extended frame format ID: 29 bits)
Buffer size	: 136-bit × 32 (transmission / reception)

- IEBus (MN103LF09/10/11/12/13/14/15 series only)

Channels	: 2 channels
Communication mode	: Select from mode1 and mode2
Driver/receiver	: External

- Port function

MN103LF09/12/15/18/21/24/27 series

I/O ports	:	130 pins
CMOS I/O	:	102 pins
Combination CMOS I/O and oscillation pin	:	4 pins
Combination CMOS I/O and Analog I/O	:	16 pins
Combination CMOS I/O and LED driver	:	8 pins
Special function pin	:	5 pins
Reset input pin (NRST) (software reset is available)	:	1 pin
A/D converter reference voltage input pin (VREFH)	:	1 pin
Capacity connect pin (VOUT18)	:	1 pin
Function contol pins (NOCDMOD, ATRST)	:	2 pins
Power pins	:	9 pins
Power supply pin(VDD50)	:	3 pins
GND pins (VSS)	:	4 pins
Analog power supply pin(AVDD)	:	1 pins
Analog GND pins (AVSS)	:	1 pins

MN103LF11/14/17/20/23/26 series

I/O ports	:	115 pins
CMOS I/O	:	87 pins
Combination CMOS I/O and oscillation pin	:	4 pins
Combination CMOS I/O and Analog I/O	:	16 pins
Combination CMOS I/O and LED driver	:	8 pins
Special function pin	:	5 pins
Reset input pin (NRST) (software reset is available)	:	1 pin
A/D converter reference voltage input pin (VREFH)	:	1 pin
Capacity connect pin (VOUT18)	:	1 pin
Function contol pins (NOCDMOD, ATRST)	:	2 pins
Power pins	:	8 pins
Power supply pin(VDD50)	:	2 pins
GND pins (VSS)	:	4 pins
Analog power supply pin(AVDD)	:	1 pins
Analog GND pins (AVSS)	:	1 pins

■ Features (continued)

- Port function (continued)

MN103LF10/13/16/19/22/25 series

I/O ports	:	87 pins
CMOS I/O	:	59 pins
Combination CMOS I/O and oscillation pin	:	4 pins
Combination CMOS I/O and Analog I/O	:	16 pins
Combination CMOS I/O and LED driver	:	8 pins
Special function pin	:	5 pins
Reset input pin (NRST) (software reset is available)	:	1 pin
A/D converter reference voltage input pin (VREFH)	:	1 pin
Capacity connect pin (VOUT18)	:	1 pin
Function contol pins (NOCDMOD, ATRST)	:	2 pins
Power pins	:	8 pins
Power supply pin(VDD50)	:	2 pins
GND pins (VSS)	:	4 pins
Analog power supply pin(AVDD)	:	1 pins
Analog GND pins (AVSS)	:	1 pins

- Package

MN103LF09/12/15/18/21/24/27 series : 144 pin LQFP (20 mm × 20 mm / 0.5 mm pitch, halogen free)
MN103LF11/14/17/20/23/26 series : 128 pin LQFP (18 mm × 18 mm / 0.5 mm pitch, halogen free)
MN103LF10/13/16/19/22/25 series : 100 pin LQFP (14 mm × 14 mm / 0.5 mm pitch, halogen free)

- Power supply voltage

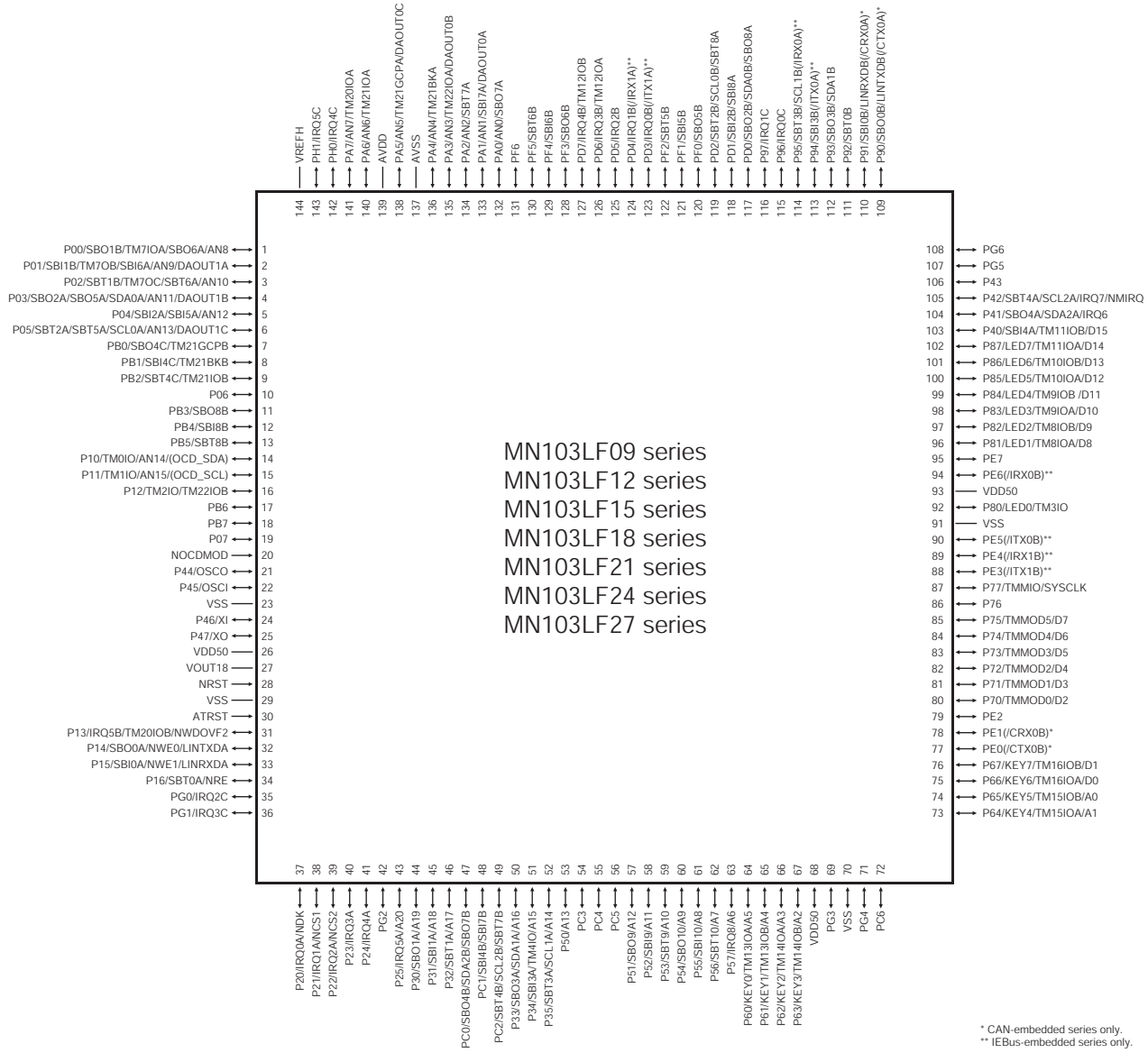
VDD50 : 2.2 V to 5.5 V
AVDD : AVDD = VDD50 (A/D converter or D/A converter is not used)
AVDD = VDD50 ≥ 2.7 V (A/D converter or D/A converter is used)

- Operating temperature

–40 °C to +105 °C

■ Pin Description

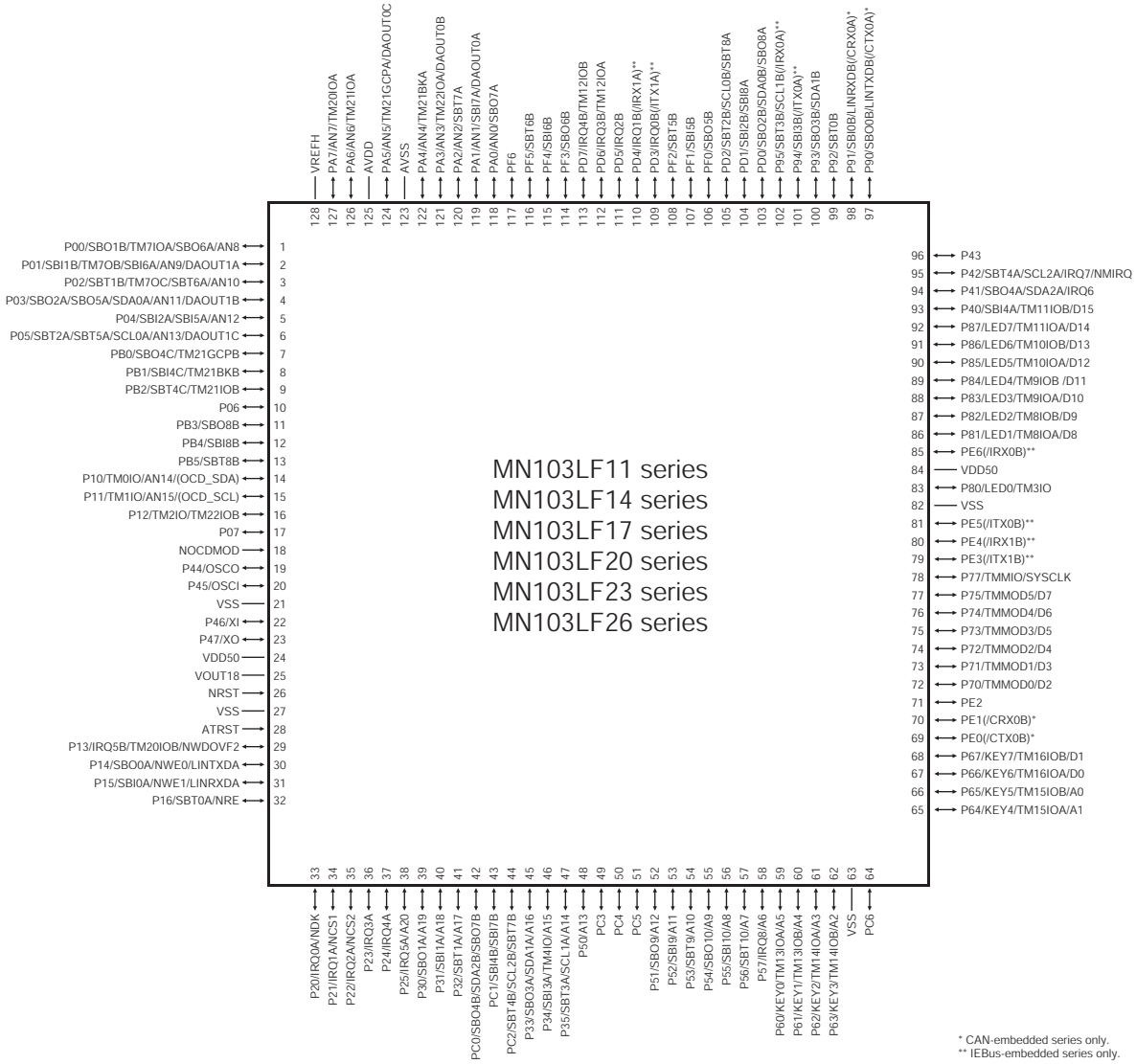
- LQFP144-P-2020D



* CAN-embedded series only.
** IEBus-embedded series only.

■ Pin Description (continued)

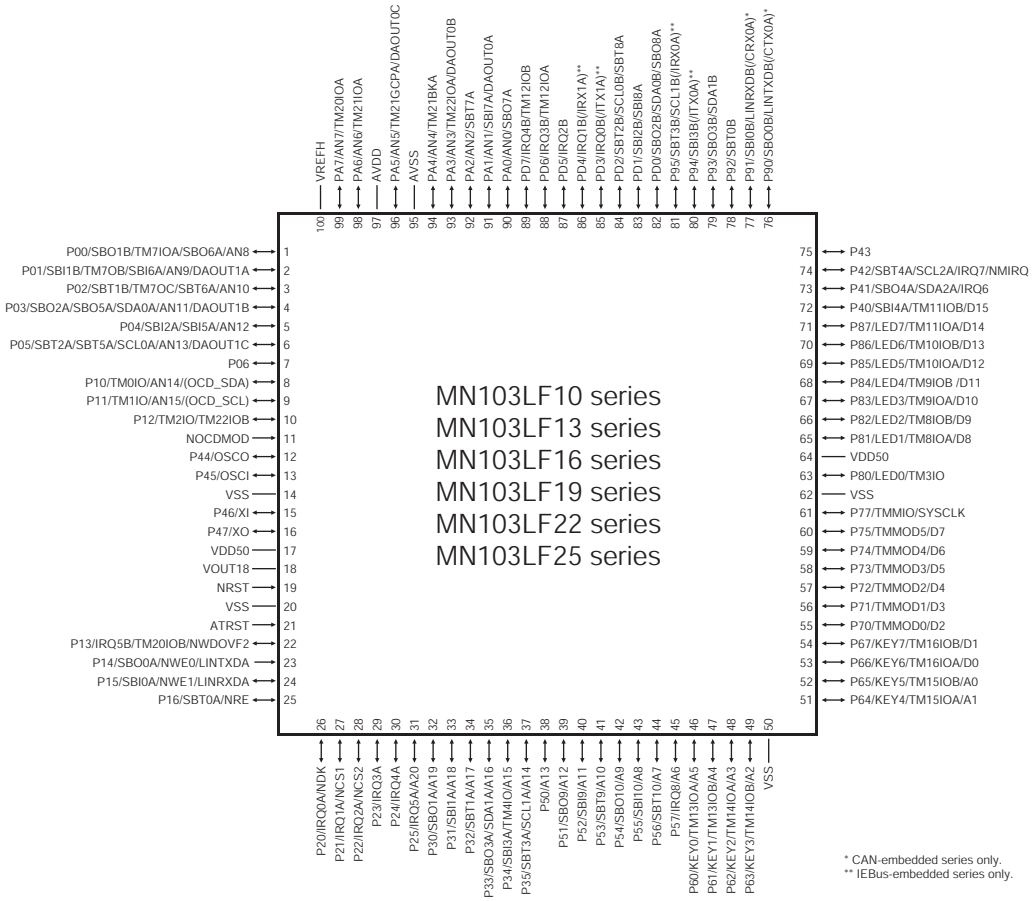
- LQFP128-P-1818F



* CAN-embedded series only.
** IEBus-embedded series only.

■ Pin Description (continued)

• LQFP100-P-1414C



* CAN-embedded series only.
** IEBus-embedded series only.

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(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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