

**MMC 4500**

1 BIT INDUSTRIAL CONTROL UNIT

GENERAL DESCRIPTION

The MMC 4500 is a single bit, one-chip static CMOS processor. The industrial Control Unit (ICU) is design for the use in systems requiring decisions based on successive single bit information. The control program is stored in an external ROM. With a program counter, output latches and input multiplexers, the ICU in a system, forms a stored program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control.

FEATURES

- 16 instructions
- Fully static operation
- Wide range of clock frequencies, typical 1 MHz operation at $V_{DD} = 5V$
- Executes one instruction per clock cycle
- Capable of driving one Low-Power Schottky load or two Low-Power TTL loads
- 3 to 18 V operation
- High noise immunity
- Low quiescent current

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: G and H types	-0.5 to 20	V
	E and F types	-0.5 to 18	V
V_i	Input voltage	-0.5 to $V_{DD}+0.5$	V
I_i	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_A = full package-temperature-range	100	mW
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

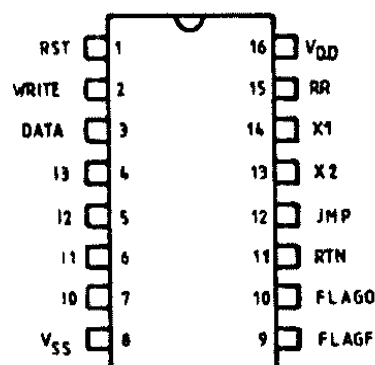
RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types	3 to 18	V
	F and F types	3 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_A	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C

PIN FUNCTION

Pin No.	Function	Symbol
1	Chip Reset	RST
2	Write Pulse	WRITE
3	Data In/Out	DATA
4	MSB Instruction Word	I3
5	Bit 2 Instruction Word	I2
6	Bit 1 Instruction Word	I1
7	LSB Instruction Word	I0
8	Ground	V_{SS}
9	Flag on NOPF	FLAGF
10	Flag on NOPD	FLAGD
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V_{DD}

CONNECTION DIAGRAM



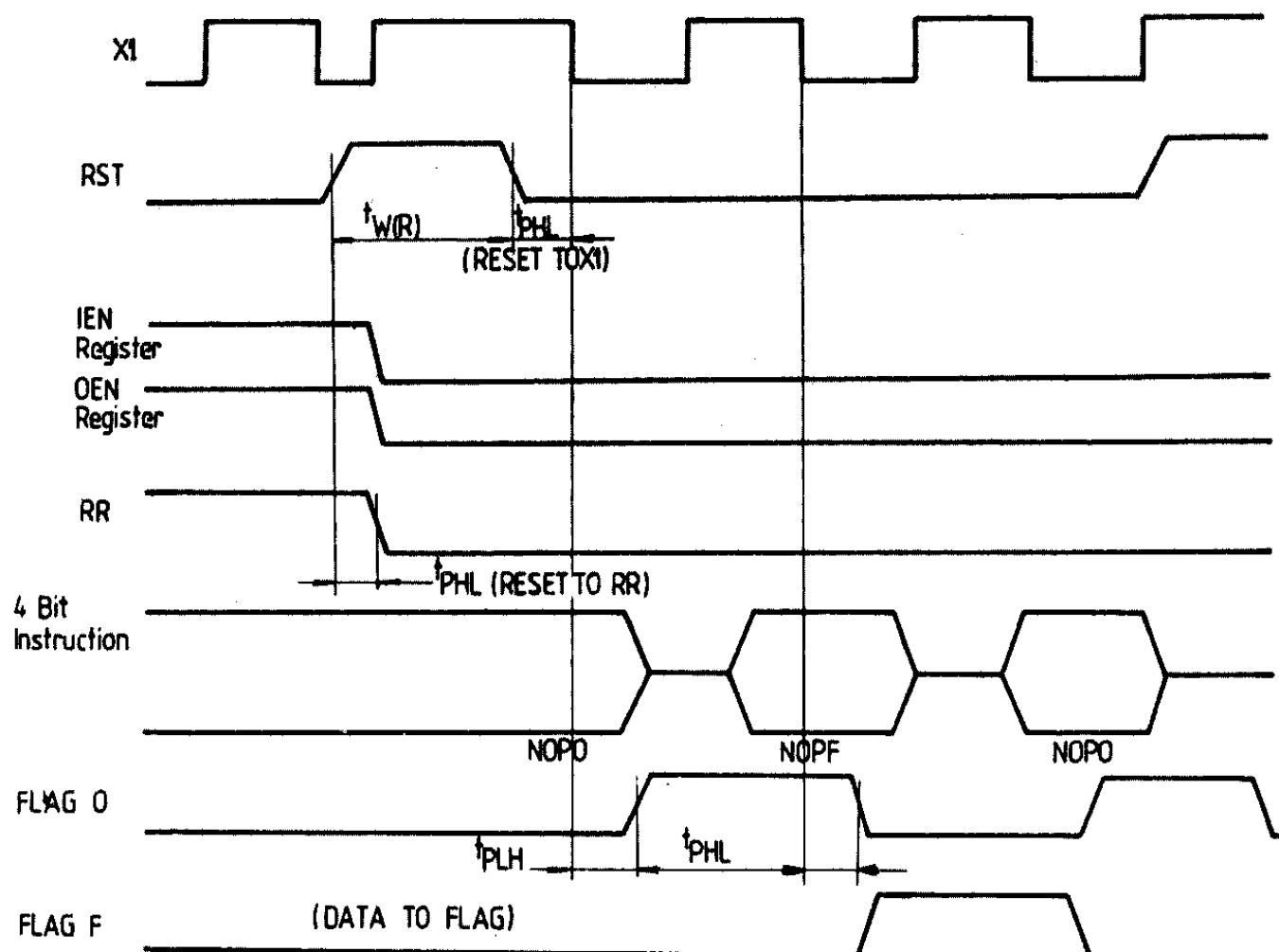
The block diagram illustrates the internal architecture of the 8085 microprocessor. Key components and their interconnections include:

- Control and Timing:** The **OSC** (Oscillator) block generates the **CK** (Clock) signal. The **RST** (Reset) input is connected to a reset circuit that also provides the **RST** signal to the **CONTROL** unit.
- Control Unit:** The **CONTROL** unit is the central hub, receiving **D** (Data) and **CK** signals, and managing the **LOGIC UNIT**, **INSTRUCTION REGISTER**, **DECODER**, and **FLAGS**.
- Instruction Register and Decoder:** The **INSTRUCTION REGISTER** receives 4-bit instructions from the **DECODER** and outputs 4-bit data to the **LOGIC UNIT**. The **DECODER** also outputs 4-bit signals to the **FLAGS** register.
- Logic Unit:** The **LOGIC UNIT** performs logical operations on data from the **D** bus and the **INSTRUCTION REGISTER**. It outputs 4-bit results to the **MUX** (Multiplexer).
- Registers and Buffers:** The **RR** (Register File) and **PI** (Program Counter) are 8-bit registers. The **PI** is connected to the **LOGIC UNIT** and the **DECODER**. The **RR** is connected to the **LOGIC UNIT** and the **MUX**.
- Output and Status:** The **MUX** outputs 4-bit data to the **ORR** (Output Register) and the **FLAGS** register. The **ORR** outputs 4-bit data to the **WRITE** signal. The **FLAGS** register outputs 4-bit status signals: **JMP** (Jump), **ORTN** (Overflow), **FLAGF** (Flag), and **FLAGO** (Flag).

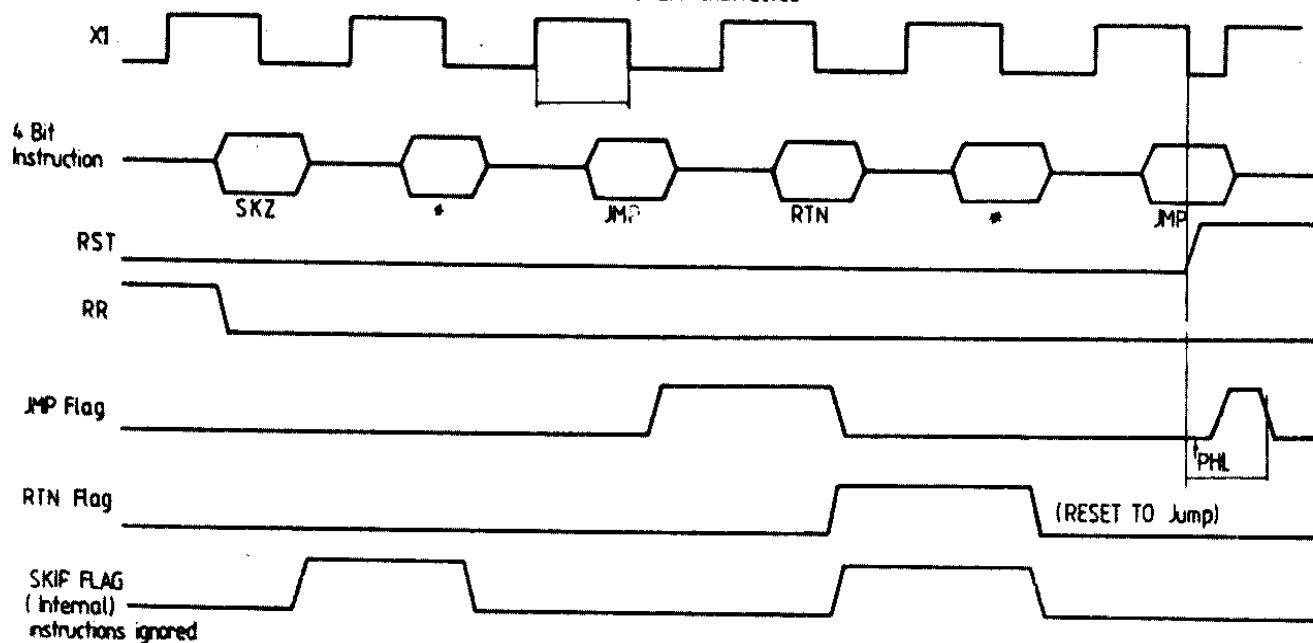
Instruction	Code	Mnemonic	Action
0	0000	NOPO	No Change in registers; $RR \leftarrow RR$, FLAG0 $\leftarrow \overline{\text{FLAG0}}$
1	0001	LD	Load result register; $RR \leftarrow \text{DATA}$
2	0010	LDC	Load complement; $RR \leftarrow \overline{\text{DATA}}$
3	0011	AND	Logical AND; $RR \leftarrow RR \wedge \text{DATA}$
4	0100	ANDC	Logical AND with complement; $RR \leftarrow RR \wedge \overline{\text{DATA}}$
5	0101	OR	Logical OR; $RR \leftarrow RR \vee \text{DATA}$
6	0110	ORC	Logical OR with complement; $RR \leftarrow RR \vee \overline{\text{DATA}}$
7	0111	XNOR	Exclusiv NOR, if $RR = \text{DATA}$, $RR \leftarrow 1$
8	1000	STO	Store; $\text{DATA} \leftarrow RR$, WRITE $\leftarrow \overline{\text{WRITE}}$
9	1001	STOC	Store complement; $\text{DATA} \leftarrow \overline{RR}$, WRITE $\leftarrow \overline{\text{WRITE}}$
10	1010	IEN	Input enable; IEN Register $\leftarrow \text{DATA}$
11	1011	OEN	Output enable; OER Register $\leftarrow \text{DATA}$
12	1100	JMP	Jump, JMP Flag $\leftarrow \overline{\text{JMP Flag}}$
13	1101	RTN	Return, RTN Flag $\leftarrow \overline{\text{RTN Flag}}$ and skip next instruction
14	1110	SKZ	Skip next instruction if $RR = 0$
15	1111	NOPF	No change in registers; $RR \leftarrow RR$, FLAGF $\leftarrow \overline{\text{FLAGF}}$

TIMING DIAGRAM

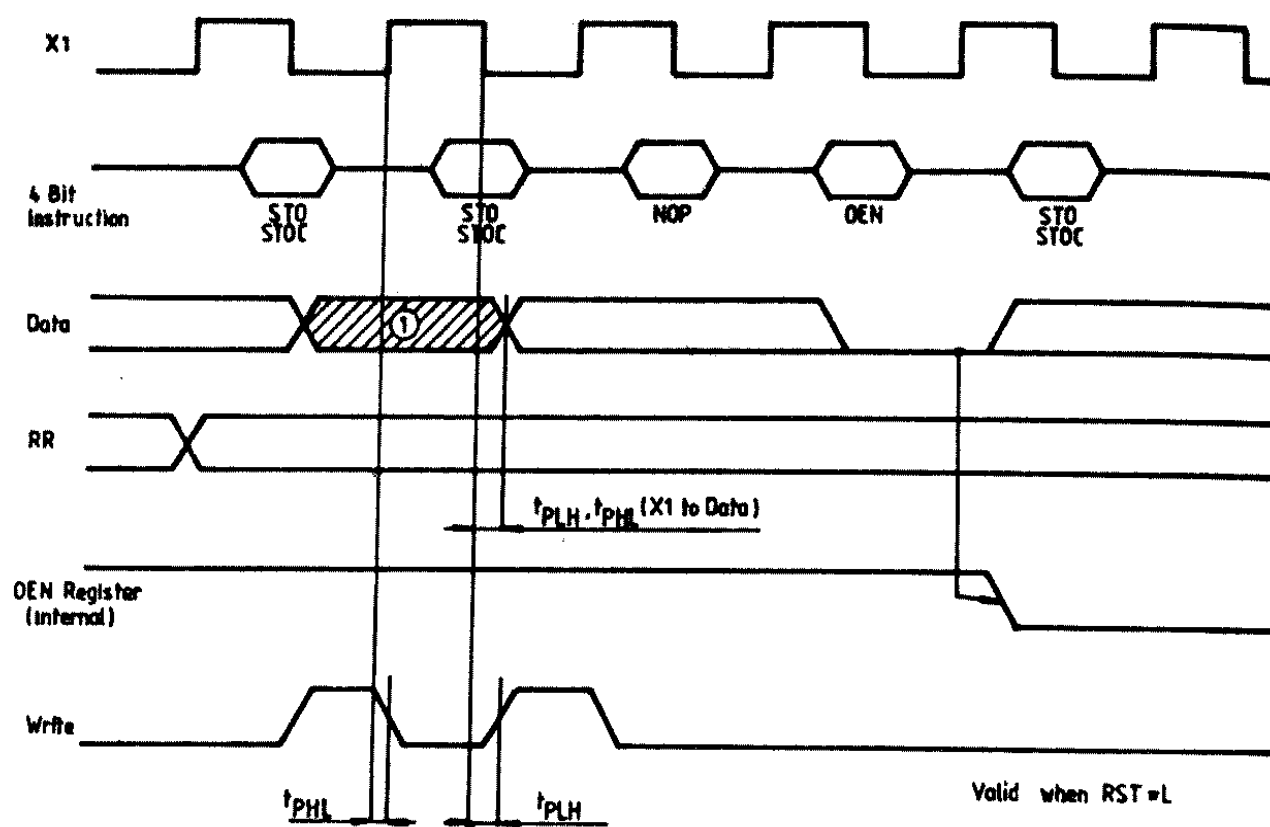
Instructions NOPD NOPF
RR IEN OEN remain unaffected



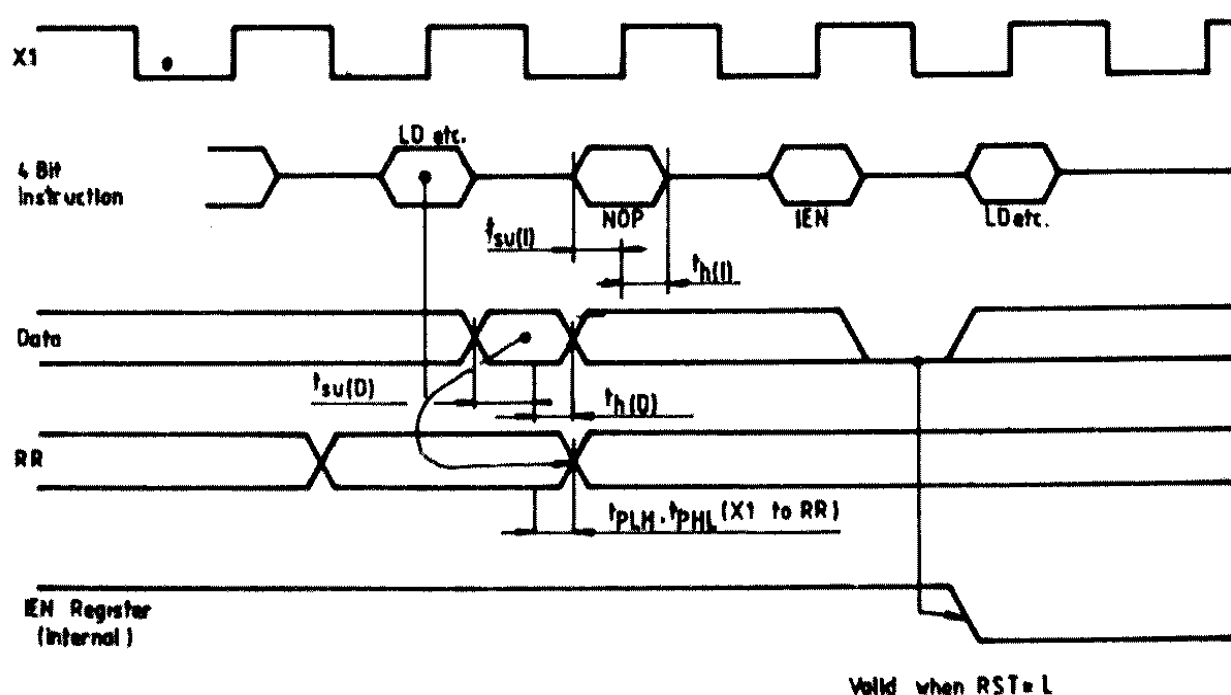
Instructions SKZ JMP RTN
RR IEN OEN remain unaffected



TIMING DIAGRAM



NOTE: 1. Valid output data



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

			TEST CONDITIONS				VALUES							
PARAMETER			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		UNIT
							min.	max.	min.	typ	max.	min.	max.	
I _L —Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA	
		0/10			10		10		0.04	10		300		
		0/15			15		20		0.04	20		600		
		0/20			20		100		0.08	100		3000		
	E, F types	0/ 5			5		20		0.04	20		150		
		0/10			10		40		0.04	40		300		
		0/15			15		80		0.04	80		600		
V _{OH} —Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL} —Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH} —Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL} —Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
V _{IH} Input High Voltage (I3,I2,I1,I0, Pins)			0.5/4.5	< 1	5	2.5		2.5	2.2		2.5		V	
			1/9	< 1	10	6		6	3.1		6			
			1.5/13.5	< 1	15	15		10	4.3		10			
V _{IL} Input Low Voltage (I3,I2,I1,I0, Pins)			4.5/0.5	< 1	5		0.8		1.1	0.8		0.8	V	
			9/1	< 1	10		1.6		2.2	1.6		1.6		
			13.5/1.5	< 1	15		2.4		3.4	2.4		2.4		
I _{OH} —Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA	
		0/ 5	4.6		5	-0.64		-0.51	-1		-0.36			
		0/10	9.5		10	-1.6		-1.3	-2.6		-0.9			
		0/15	13.5		15	-4.2		-3.4	-6.8		-2.4			
	E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1			
		0/ 5	4.6		5	-0.52		-0.44	-1		-0.36			
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9			
		0/15	13.5		15	-3.6		-3.0	-6.8		-2.4			
I _{OL} —Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA	
		0/10	0.5		10	1.6		1.3	2.6		0.9			
		0/15	1.5		15	4.2		3.4	6.8		2.4			
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36			
		0/10	0.5		10	1.3		1.1	2.6		0.9			
		0/15	1.5		15	3.6		3.0	6.8		2.4			
I _{OH} Output drive Current (DATA, WRITE Pins) All types		0/ 5	4.6		5	-1.2		-1.0	-2.0		-0.7		mA	
		0/10	9.5		10	-3.6		-3.0	-6.0		-2.1			
		0/15	13.5		15	-7.2		-6.0	-12.0		-4.2			
I _{OL} Output Sink Current (DATA, Write Pins) All types		0/ 5	0.4		5	1.9		1.6	3.2		1.1		mA	
		0/10	0.5		10	3.6		3.0	6.0		2.1			
		0/15	7.2		15	6.0		6.0	12.0		4.2			

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES						UNIT	
			V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
							min.	max.	min.	typ	max.	min.		max.
I _{OH} 3—state output	G, H types	0/18	0/18		18		±0.4		±10 ⁻⁴	±0.4		±12	μA	
	E, F types	0/15	0/15		15		±1.0		±10 ⁻⁴	±1.0		±7.5		
I _{in} Input Current (RST Pin)					15	25			150			250	μA	
I _{IH} , I _{IL} Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 ⁻⁵	±0.1		±1	μA	
	E, F types	0/15			15		±0.3		±10 ⁻⁵	±0.3		±1		
C _I —input capacitance			Any input						5	7.5			pF	
C _{in} Input Capacitance (DATA Pin)									15				pF	
I _T * Total Supply Current at on External Load Capacitance (CL) on All outputs					5 10 15	I _T =(1.5μA/kHz)xf+I _L I _T =(3.0μA/kHz)xf+I _L I _T =(4.5μA/kHz)xf+I _L							μA	

* The formulas given are for the typical characteristics only at 25°C

• T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.• T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A=25^\circ\text{C}$; $C_L=50\text{pF}$ for JMP, X1, RR, FLAGO, FLAGF; $C_L=130\text{pF}+1\text{TTL}$ load for DATA and WRITE
 $R_L=200\text{K}$; all inputs rise and fall times=20 ns).

CHARACTERISTICS	SYMBOL	V_{DD}	VALUES			UNITS
			Min.	Typ.	Max.	
Propagation delay Time X1 to RR X1 to FLAG F, FLAG O, RTN, JMP X1 to WRITE X1 to DATA RST to RR RST to X1 RST to FLAG F, FLAG O, RTN, JMP RST to WRITE, DATA	t_{dR}	5	—	250	500	ns
		10	—	125	250	
		15	—	100	200	
	t_{dF}	5	—	200	400	
		10	—	100	200	
		15	—	85	170	
	t_{dW}	5	—	225	450	
		10	—	125	250	
		15	—	100	200	
	t_{dD}	5	—	250	500	
		10	—	120	240	
		15	—	100	200	
	t_{dRRR}	5	—	250	500	
		10	—	125	250	
		15	—	100	200	
	t_{dRX}	5	—	450	Note 1	
		10	—	200		
		15	—	150		
	t_{dRF}	5	—	400	800	
		10	—	200	400	
		15	—	150	300	
	t_{dRW}	5	—	450	900	
		10	—	225	450	
		15	—	175	350	
Clock Pulse Width, X1	$t_{W(c1)}$	5	400	200	—	ns
		10	200	100	—	
		15	180	90	—	
Reset Pulse Width, RST	$t_{W(R)}$	5	500	250	—	ns
		10	250	125	—	
		15	200	100	—	
Setup time, instruction Data	t_{SUII}	5	400	200	—	ns
		10	250	125	—	
		15	180	90	—	
	t_{SUIDI}	5	200	100	—	
		10	100	50	—	
		15	80	40	—	
Hold Time Instruction Data	$t_{HI(I)}$	5	100	0	—	ns
		10	50	0	—	
		15	50	0	—	
	$t_{HI(D)}$	5	200	100	—	
		10	100	50	—	
		15	100	50	—	

Note 1 Maximum reset Delay may extend to one half clock period
 Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC potential performance.

TYPICAL APPLICATIONS

