PLESSEY
Semiconductors

T-77-11

ML924

REMOTE CONTROL RECEIVER

The ML924 is an MOS/LSI integrated circuit for use as a receiver of remote control signals generated by the SL490B transmitter circuit, using PPM (Pulse Position Modulation) encoding technique. The receiver has 5 digital outputs whose response to PPM codes may be programmed by six control lines. It has a handshake interface which provides communication with microprocessors and computers.

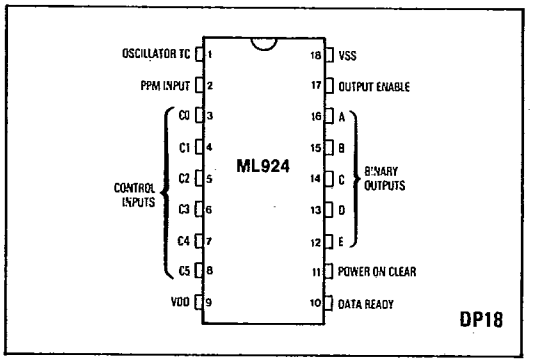

Fig.1 Pin connections (top view)

FEATURES

- 5 Open Drain Outputs with Enable
- Handshake or Interrupt Microprocessor and Computer Interface Signals
- On-Chip Oscillator
- 6 Control Lines to Programme Output Response
- 3 Selectable Output Modes

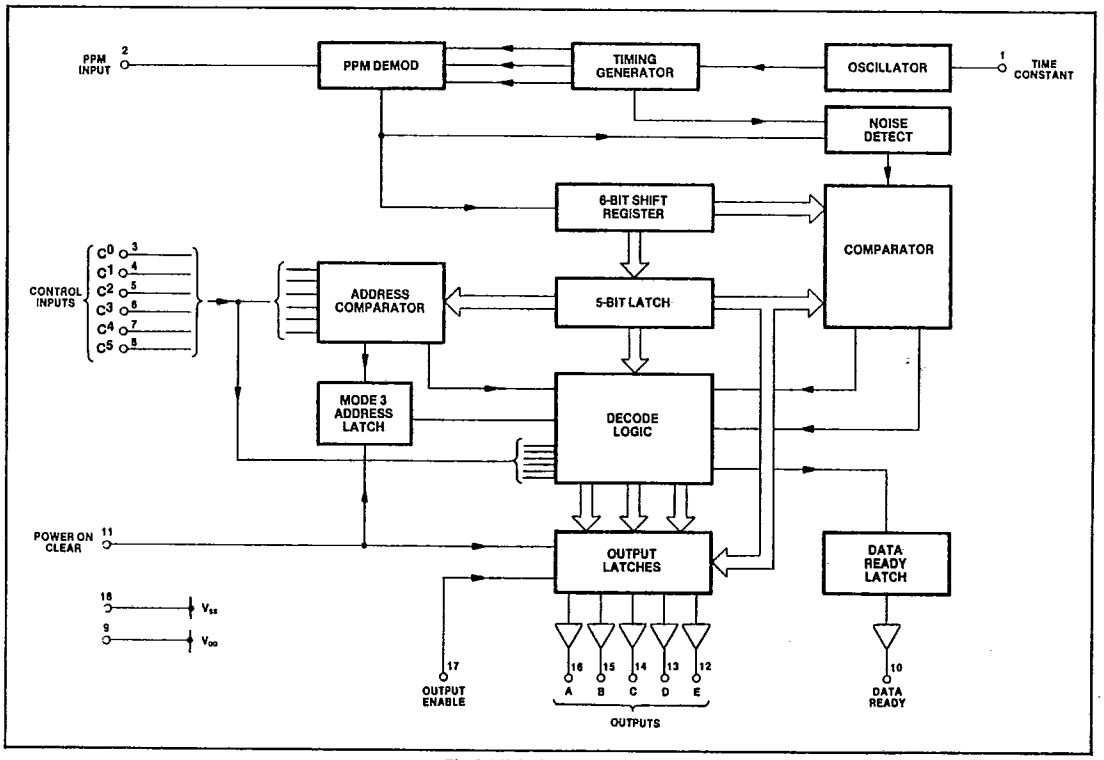

Fig.2 ML924 block diagram

ELECTRICAL CHARACTERISTICS

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Test conditions (unless otherwise stated):
VSS = 0V; VDD = -16V; T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	9	12		18	V	
Supply current	9		6		mA	
Input logic level high ('1')	3-8,17	-1		0	V	
Input logic level low ('0')		V_{DD}		V_{DD} + 3.5	V	
Output logic level high ('1')	10,12-16	-1		0V		50k to V_{DD}
Output logic level low ('0')		V_{DD}		V_{DD} + 0.5	V	
Oscillator frequency	1	15	3k	150k	Hz	Typical TC: C = 22nF, R = 100kΩ
PPM input level high	2	-1		0V		
PPM input level low		V_{DD}		-6V		
PPM input pulse width	2	1		$22T_{osc}$	μs	$T = \frac{1}{f_{osc}}$
Power clear time constant	11	1	400		ms	

NOTE

Rosc (Pin 1) is 56kΩ to 156kΩ, $fosc \simeq \frac{1}{0.15\,CR}$ ±20%

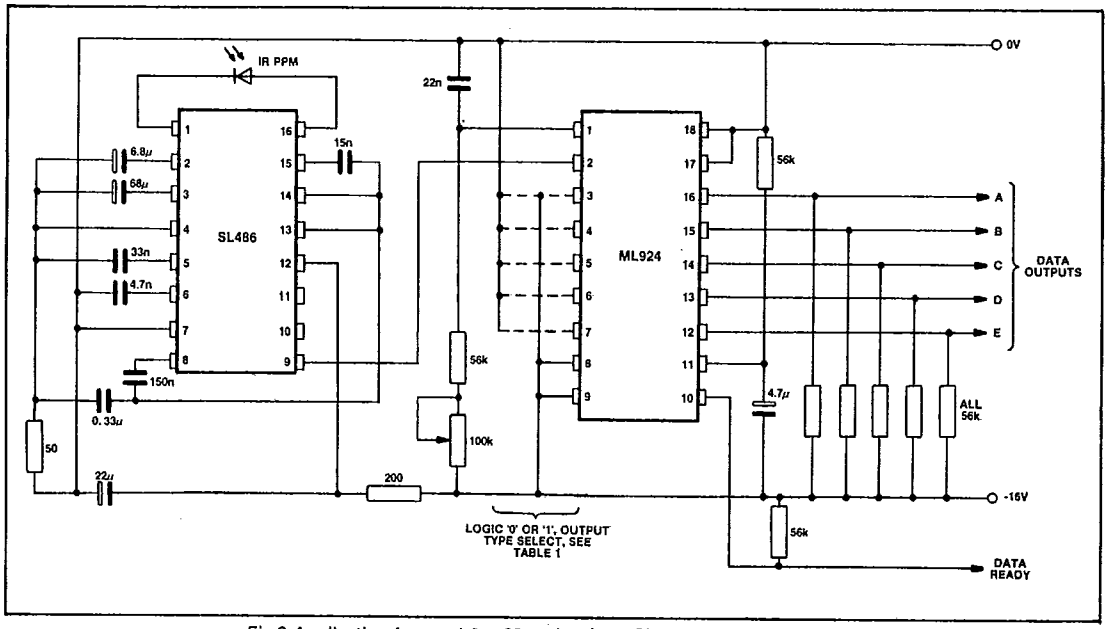

Fig.3 Application for receiving 32 codes, from SL490 transmitter, in mode 1

PIN FUNCTIONS

Positive Logic: Logic '1' = Vss, 0V Logic '0' = V_{DD}, -16V

1. Oscillator TC An RC time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to this pin; the signal must consist of a normal low level with pulses to the high state.

3-8. Control Word C_0 to C_5 Six control bits form the control word which programs the response of the five outputs (see Table 1).

9. V_{DD} -12V to -18V power supply.

10. Data Ready Open drain output. An output of logic '1' indicates the reception of a valid PPM word. It will remain at logic '1' for the duration of transmission.

11. Power Clear A capacitor and resistor connected to this pin define the time delay for the Power Clear Circuit.

12-16. Outputs E-A Open drain outputs which respond to the PPM input as defined in Table 1.

17. Output Enable A logic '1' will enable outputs A to E. A logic '0' will turn all outputs off.

18. Vss 0V (Ground).

APPLICATION NOTES T-77-11

By setting combinations of logic states on the six control line inputs, C_0 to C_5 (pins 3 to 8), the outputs E to A (pins 12 to 16) on the ML924, can respond to the PPM input word (as shown in Fig.4) in three modes, detailed below:

Control Mode 1

Each output E to A directly corresponds to bits e to a in the PPM word. The type of output available can be either latched (LA) or momentary (M) according to the combination of C_0 to C_5 used, as given in Table 1. This mode allows direct control of all five bits on one receiver, by the 32 codes from an SL490B transmitter. Fig.3 shows the ML924 used in this mode in conunction with an SL486 infra-red pre-amplifier.

Control Mode 2

Bits a and b, in the PPM input word, address one of up to four (binary 0 to 3) receivers that has been correspondingly designated that number (W_1W_0), by bits C_0 and C_1 in the control word (Table 1). Bits c and d in the PPM input word, address one of four outputs D to A, on this addressed receiver (Table 1, note 2), via code V_1V_0. Output E is not used.

Bits C_2 to C_5, in the control word, select combinations of output types; either set/reset (S/R) or momentary (M) as shown in Table 1. The addressed output (V_1V_0) on the addressed receiver (W_1W_0) will either be reset by bit e of the PPM input word (logic '0'), or set (pulsed if momentary type output), if bit e is logic '1'.

This mode thus allows the state of up to 16 bits (4 each on 4 receivers), to be individually controlled by the PPM input word, with the 32 codes from an SL490B transmitter. Table 2(a) shows, in detail, the received code interpretation for mode 2.

Control Mode 3

The PPM input word can be interpreted as address or data, depending on the logic state of bit e. If bit e is logic '0', bits a to d address one of up to sixteen (binary 0 to 15) receivers that has been correspondingly designated that number ($U_3U_2U_1U_0$) by bits C_0 to C_3 in the control word (Table 1). If bit e is logic '1', then bits a to d correspond to the outputs A to D on the currently addressed receiver.

The output types can either be all latched (LA) or all momentary (M), depending on the logic state of control bits C_4 and C_5 (Table 1).

Output E of the currently addressed receiver is used as an address acknowledge output (true high), and will go high upon reception of a valid address code. This output will remain high until reception of an invalid address code, or a power-on reset. Thus, only one of the sixteen possible bit E outputs will be high at any one time.

In this manner, up to sixty-four bits (four bits each on sixteen receivers) can be individually controlled by the PPM input word, with the 32 codes from an SL490B transmitter. Fig.5 outlines the application diagram for mode 3, using the maximum possible number of receivers (for one PPM rate). Details of the input PPM code interpretation for mode 3 are given in Table 2(b).

In all modes, taking the output enable input (pin 17) low swithces off all the outputs, except data ready, but the device retains the data internally.

The momentary (M) type of output means that data is available during reception of the PPM input word only, i.e. after a valid word has been detected by the ML924. A valid word is realised when two successive identical PPM input words are detected. The DATA READY output is at logic '1' during the reception of a valid PPM input word. All momentary outputs will be returned to zero when reception of the valid PPM input word ceases (i.e. a successive word is different or absent from the preceding word). DATA READY will also return to the zero state. If the latched (LA) type of output has been chosen, the received data will be latched and retained when reception ceases. Note also that in mode 3 a valid (matched) received address code is also latched. Similarly, for a set/reset (S/R) type of output, data is retained when reception ceases.

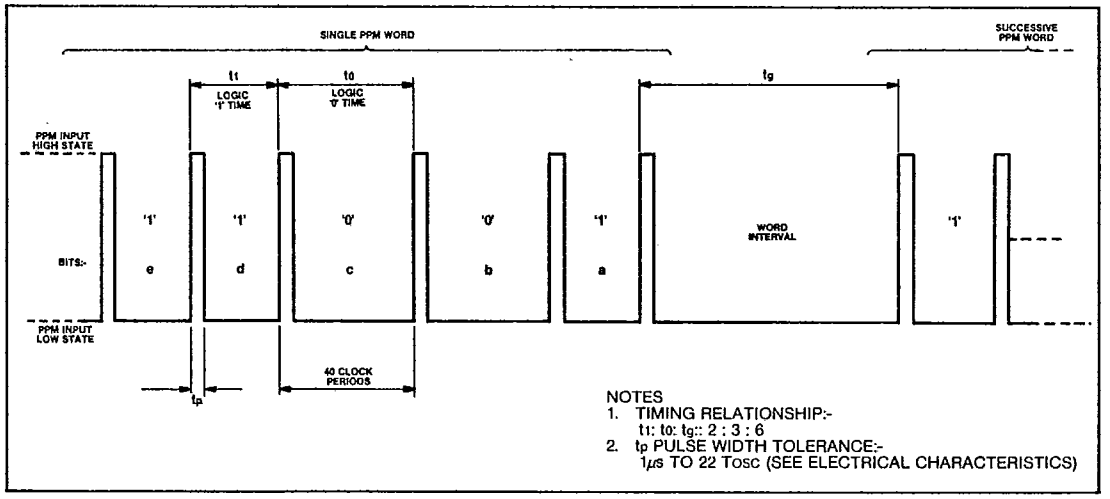

Fig.4 PPM input word format, showing 11001 example

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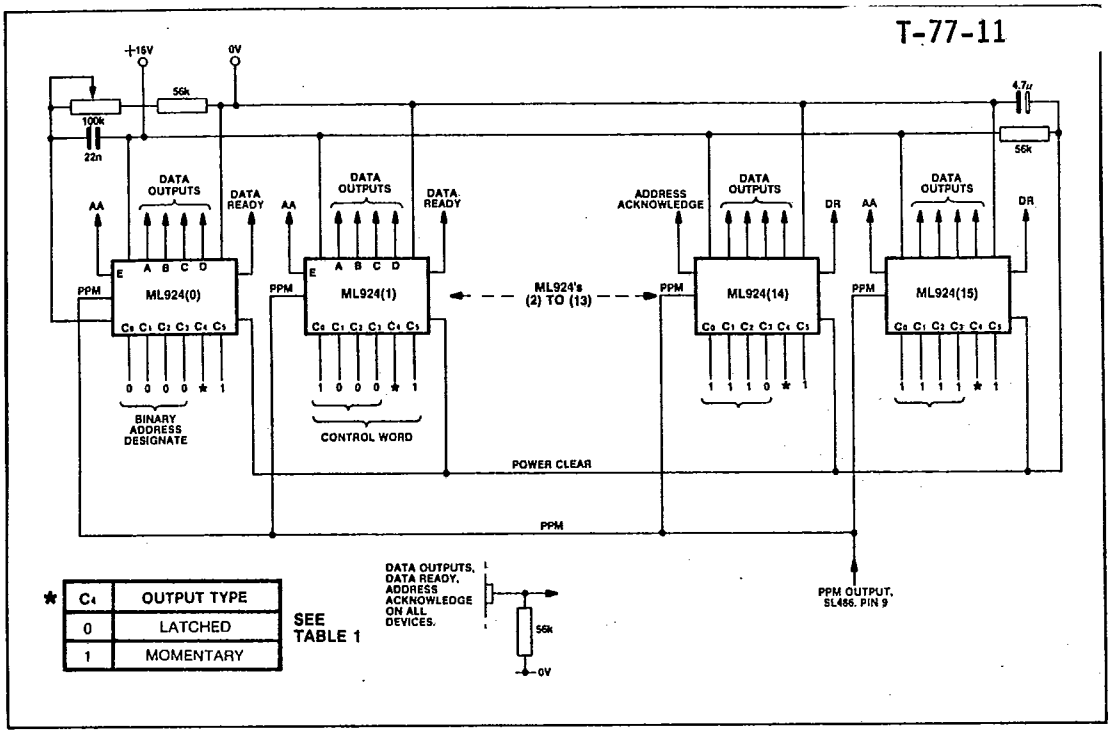

*	C_4	OUTPUT TYPE
	0	LATCHED
	1	MOMENTARY

Fig.5 Application for controlling up to 64 bits in mode 3

Control word						Control mode	Output response					Interpretation of PPM input words	
C_5	C_4	C_3	C_2	C_1	C_0		E	D	C	B	A	e d c b a	e d c b a
0	0	0	0	0	0	1	LA	LA	LA	LA	LA	E D C B A: PPM decoded on all outputs directly	
0	0	0	0	0	1	1	LA	LA	LA	LA	M		
0	0	0	0	1	1	1	LA	LA	LA	M	M		
0	0	0	1	1	1	1	LA	LA	M	M	M		
0	0	1	1	1	1	1	LA	M	M	M	M		
0	1	1	1	1	1	1	M	M	M	M	M		
0	0	1	0	W_1	W_0	2	-	S/R	S/R	S/R	S/R	0 V_1 V_0 W_1 W_0: Output address, Receiver address; Resets an S/R type output. No effect on a momentary output.	1 V_1 V_0 W_1 W_0: Output address, Receiver address; Sets an S/R type output, or pulses a momentary output.
0	1	0	0	W_1	W_0	2	-	S/R	S/R	S/R	M		
0	1	0	1	W_1	W_0	2	-	S/R	S/R	M	M		
0	1	1	0	W_1	W_0	2	-	S/R	M	M	M		
1	0	U_3	U_2	U_1	U_0	3	AA	LA	LA	LA	LA	0 U_3 U_2 U_1 U_0: Receiver address; Designates address mode	1 D C B A: PPM data Sent to outputs on addressed receiver; Designates data mode
1	1	U_3	U_2	U_1	U_0	3	AA	M	M	M	M		

Table 1 Interpretation of ML924 control word

NOTES
1. Control mode 1 : Direct response to the PPM code.
2. Control mode 2 : W_1W_0 is a 2 bit address for the receiver, designated W_1W_0 by the control word. V_1V_0 selects one of 4 outputs on the addressed receiver.

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V_1	V_0	Addressed output
0	0	A (Pin 16)
0	1	B (Pin 15)
1	0	C (Pin 14)
1	0	D (Pin 13)

3. Control mode 3: $U_3U_2U_1U_0$ is a 4 bit address that selects, by means of 16 PPM codes, the receiver designated $U_3U_2U_1U_0$ by the control word, when bit e of the PPM code is '0'. If bit e is '1', the 4 outputs A to D on the currently addressed receiver are directly controlled by bits a to d.
4. Control mode 3: The E output of the receiver acts as an address acknowledge (AA) output. This goes high when a receiver detects a valid address instruction, and indicates that it will receive subsequent data transmission.

OPERATING NOTES

Receiver Oscillator

The receiver operates on a time scale fixed by an internal oscillator and its external components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receiver systems to respond to different transmission rates within the same area). If more than one ML924 is being used in a receiver system (control modes 2 or 3) the oscillators can be connected together, still allowing the receiver system timing to be set with one adjustment only. In other words, only one RC arrangement is needed, with pin 1 on all ML924's connected together for the devices constituting the single receiver system.

Setting Up Procedure

When designing a system using the SL490B/491 transmitters and the ML924 receiver, it is not necessary to adjust the PPM rate on both transmitter and receiver. The usual arrangement is to have a fixed resistor of 33k from pin 16 of the SL490B/491 and to choose the capacitor connected for pin 16 to pin 17 to give the required PPM rate. The value is calculated from the formula $t_o = 1.4CR$. Provided fairly close tolerance components are used for C1 and R1, then assembled transmitter units should be interchangeable without adjustment.

The timing components on the ML924 receiver can be selected using the formula

$$f_{rx} = \frac{1}{0.15CR} \text{ where } f_{rx} = \frac{40}{t_o}$$

t_o being the PPM logic 0 time from the transmitter.

The value of R for the receiver should be between 47k and 200k, a typical arrangement being to use a 47k fixed resistor and a 100k pot as shown in Fig.6. The capacitor should be selected from the above formula to give the nominal frequency somewhere near the mid-range setting of the potentiometer.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter PPM logic '0' time, using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope probe to reduce circuit loading.

Maximum Bit Control

In all modes, the maximum possible number of bits that can be controlled by one 32 code transmitter, can be increased by using more than one PPM rate. For example, it is possible to control a maximum of 128 bits in mode 3, by using 16 receivers operating on one PPM rate, and 16 receivers operating on a second PPM rate separated from the first by a fator of at least 2. If using an SL490B transmitter, a transmission rate of n and (nx2) may be incorporated in one device application, thus allowing 128 bits to be controlled by one 32 code transmitter.

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PPM word bits	a b 1 1	a b 0 1	a b 1 0	a b 0 0	W₀W₁	c	d	e
Receiver address/ control word bits	C₀ C₁ 1 1	C₀ C₁ 0 1	C₀ C₁ 1 0	C₀ C₁ 0 0				
Sets an S/R type output to 1; pulses momentary output	31	30	29	28	V₀V₁	1	1 (D)	1
	27	26	25	24	V₀V₁	0	1 (C)	1
	23	22	21	20	V₀V₁	1	0 (B)	1
	19	18	17	16	V₀V₁	0	0 (A)	1
Resets an S/R type output to zero; no change momentary output	15	14	13	12	V₀V₁	1	1 ($\overline{D}$)	0
	11	10	9	8	V₀V₁	0	1 ($\overline{C}$)	0
	7	6	5	4	V₀V₁	1	0 ($\overline{B}$)	0
	3	2	1	0	V₀V₁	0	0 ($\overline{A}$)	0

Decimal equivalent codes (a) mode 2

ML924 output address

PPM word bits	a b 1 1	a b 0 1	a b 1 0	a b 0 0	c	d	e
Receiver address/ control word bits	C₀ C₁ 1 1	C₀ C₁ 0 1	C₀ C₁ 1 0	C₀ C₁ 0 0	C₂	C₃	
Output data	31	30	29	28	1	1	1
	27	26	25	24	0	1	1
	23	22	21	20	1	0	1
	19	18	17	16	0	0	1
Address data	15	14	13	12	1	1	0
	11	10	9	8	0	1	0
	7	6	5	4	1	0	0
	3	2	1	0	0	0	0

Decimal equivalent codes (b) mode 3

Table 2 ML924 received PPM code interpretation, for modes 2 and 3

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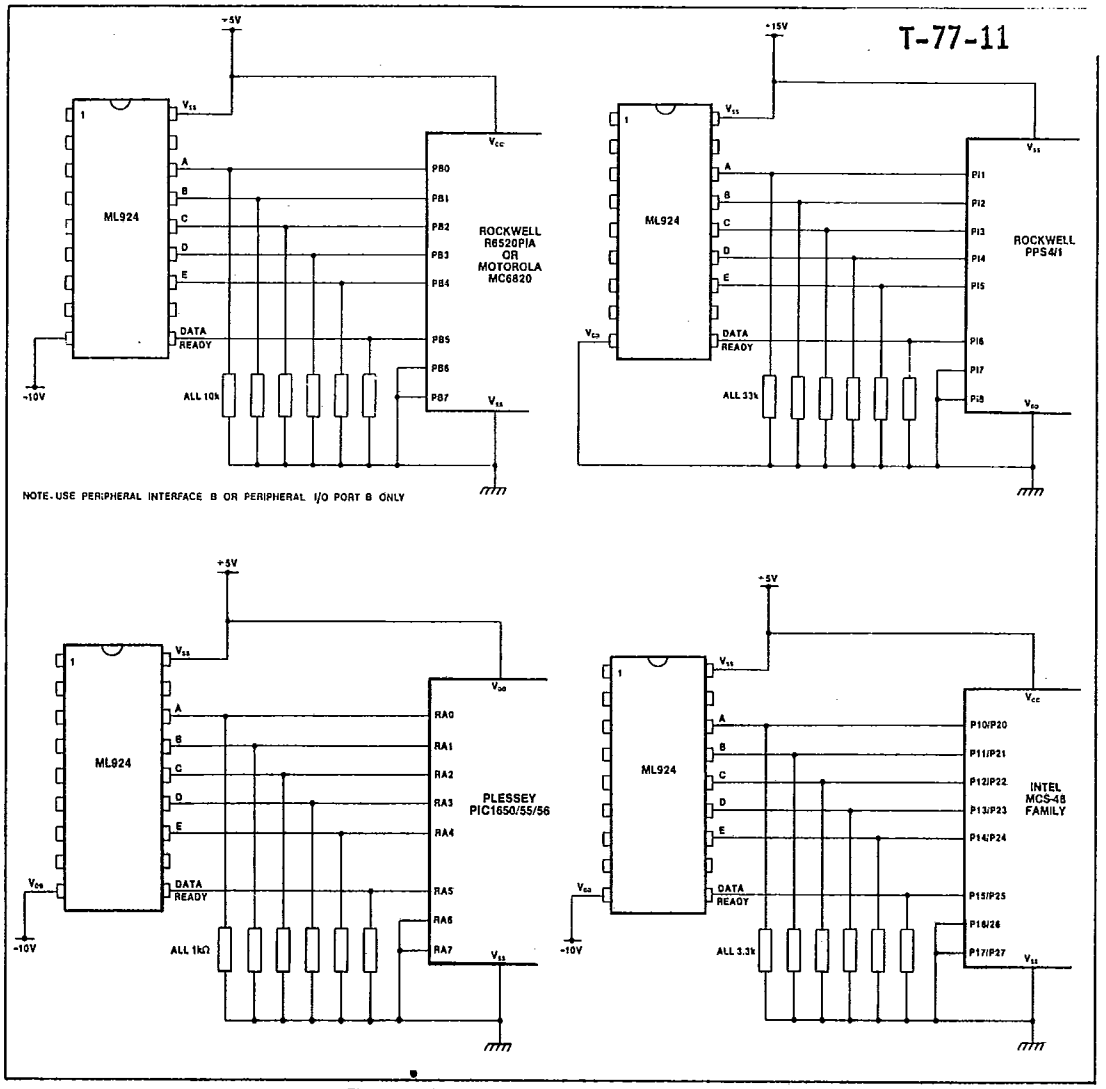

Fig.6 Interface to commonly used microprocessors