LAPIS Semiconductor

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ML9059E

132-Channel LCD Driver with Built-in RAM for LCD Dot Matrix Displays

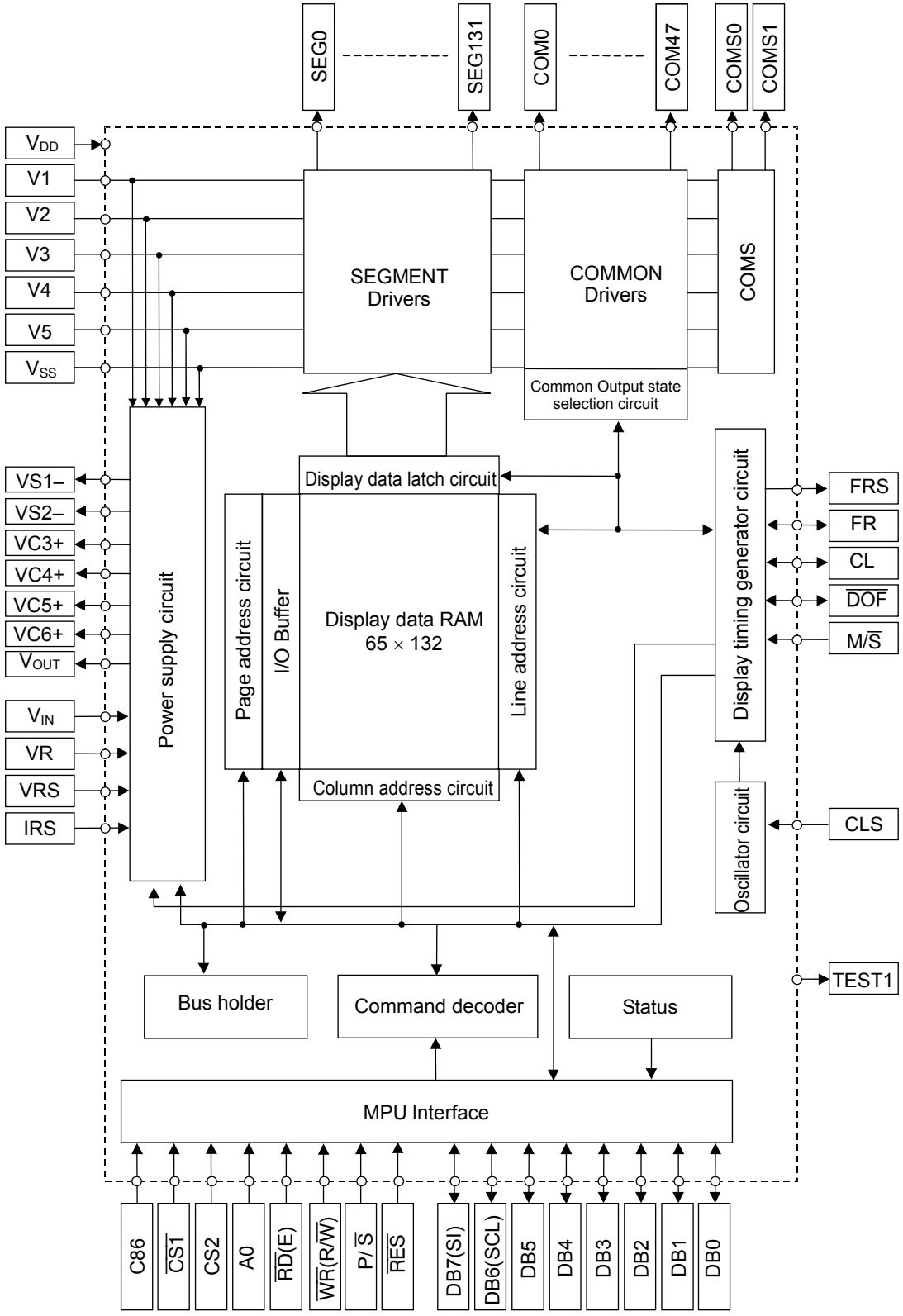
GENERAL DESCRIPTION

The ML9059E is an LSI for dot matrix graphic LCD devices carrying out bit map display. This LSI can drive a dot matrix graphic LCD display panel under the control of an 8- bit microcomputer (hereinafter described MPU). Since all the functions necessary for driving a bit map type LCD device are incorporated in a single chip, using the ML9059E makes it possible to realize a bit map type dot matrix graphic LCD display system with only a few chips. Since the bit map method in which one bit of display RAM data turns ON or OFF one dot in the display panel, it is possible to carry out displays with a high degree of freedom such as Chinese character displays, etc. With one chip, it is possible to construct a graphic display system with a maximum of 49 × 132 dots. The display can be expanded further using two chips. However, the ML9059E is not used in a multiple chip configuration when a line reversal drive is set.
The ML9059E is made using a CMOS process. Because it has a built-in RAM, low power consumption is one of its features, and is therefore suitable for displays in battery-operated portable equipment.
The ML9059E has 49 common signal outputs and 132 segment signal outputs and one chip can drive a display of up to 49 × 132 dots.

FEATURES

- Direct display of the RAM data using the bit map method
  Display RAM data "1" ... Dot is displayed
  Display RAM data "0" ... Dot is not displayed (during forward display)
- Display RAM capacity
  65 × 132 = 8580 bits
- LCD Drive circuits
  49 common outputs, 132 segment outputs
- MPU interface: Can select an 8-bit parallel or serial interface
- Built-in voltage multiplier circuit for the LCD drive power supply
- Built-in LCD drive voltage adjustment circuit
- Built-in LCD drive bias generator circuit
- Can select frame reversal drive or line reversal drive by command
- Built-in oscillator circuit (Internal RC oscillator/external clock input)
- A variety of commands
  Read/write of display data, display ON/OFF, forward/reverse display, all dots ON/all dots OFF, set page address, set display start address, etc.
- Power supply voltage
  Logic power supply: V_{DD}-V_{SS} = 3.7 V to 5.5 V
  Voltage multiplier reference voltage: V_{IN}-V_{SS} = 3.7 V to 5.5 V
  (2- to 4-time multiplier available)
  LCD Drive voltage: V_{BI}-V_{SS} = 6.0 to 18 V
- Package: Gold bump chip (Bump hardness: Low, DV)
  : Gold bump chip (Bump hardness: High, CV)
- This device is not resistant to radiation and light.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V

Parameter	Symbol	Condition	Rated value	Unit	Applicable pins
Power supply voltage	V_{DD}	Tj = 25°C	–0.3 to +6.5	V	V_{DD}
Bias voltage	V_{BI}	Tj = 25°C	–0.3 to +20	V	V1 to V5
Voltage multiplier output voltage	V_{OUT}	Tj = 25°C	–0.3 to +20	V	V_{OUT}
Voltage multiplier reference voltage	V_{IN}	2-time multiplication 3-time multiplication 4-time multiplication	–0.3 to +5.5 –0.3 to +5.5 –0.3 to +5.0	V V	IN
Input voltage	V_I	Tj = 25°C	–0.3 to V_{DD}+0.3 V		All inputs
Storage temperature range	T_{STG}	Chip	–55 to +125	°C	—

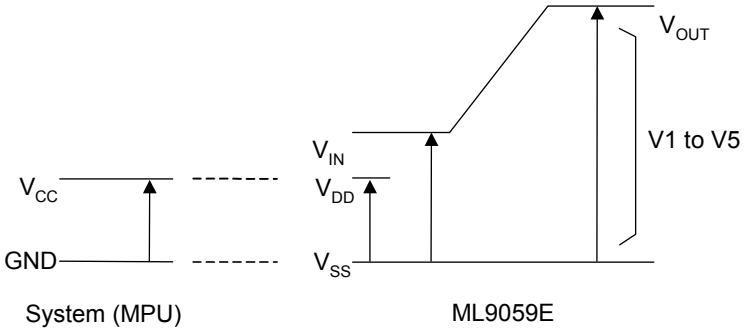
Tj:Chip surface temperature

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0 V

Parameter	Symbol	Condition	Rated value	Unit	Applicable pins
Power supply voltage	V_{DD} —		3.7 to 5.5	V	V_{DD}
Bias voltage	V_{BI}	—	6 to 18	V	V1 to V5
Voltage multiplier reference voltage	V_{IN}	2-time multiplication 3-time multiplication 4-time multiplication	3.7 to 5.5 3.7 to 5.5 3.7 to 4.5	V V	IN
Voltage multiplier output voltage	V_{OUT}	External input	6.0 to 18	V	V_{OUT}
Operating temperature range	T_{JOP}	—	–40 to +85	°C	—

Note 1: The electrical characteristics are influenced by COG trace resistance. This LSI always has to be evaluated before using.



Note 2: The voltages V_{DD}, V1 to V5, and V_{OUT} are values taking V_{SS} = 0 V as the reference.
Note 3: The highest bias potential is V1 and the lowest is V_{SS}.
Note 4: Always maintain the relationship V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 ≥ V_{SS} among these voltages.

Note 5: When using an external power supply, follow the procedure for power application.
When applying external power to the V_{OUT} pin only, apply V_{OUT} after V_{DD}.
When applying external power to the V1 pin only, apply V1 after V_{DD}.
When applying external power to the V1 pin to V5 pin, apply V1 to V5 after V_{DD}.
Note that the above (Note 4) must be satisfied including transient state at power application.

Note 6: When using an external power supply, follow the procedure for power removal described below.
When external power is in use for the V_{OUT} pin only, remove V_{OUT} after V_{DD}.
When external power is in use for the V1 pin only, remove V1 after V_{DD}.
When external power is in use for the V1 pin to V5 pin, remove V1 to V5 after V_{DD}.
Note that the above (Note 4) must be satisfied including transient state at power removal.

ELECTRICAL CHARACTERISTICS

DC Characteristics

[V_{SS} = 0 V, V_{DD} = 3.7 to 5.5 V, Tj =–40 to +85°C]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Applicable pins
"H" Input voltage		V_{IH}		0.8 × V_{DD}	—	V_{DD}	V	*1
"L" Input voltage		V_{IL}		0	—	0.2 × V_{DD}		
"H" Input voltage		V_{IH}		0.8 × V_{DD}	—	V_{DD}	V	*2
"L" Input voltage		V_{IL}		0	—	0.2 × V_{DD}		
Hysteresis width		ΔV	V_{DD} = 5.0 V	0.85	1.0	1.55		
"H" output voltage		V_{OH}	I_{OH} = –0.5 mA	0.8 × V_{DD}	—	—	V	*3
"L" output voltage		V_{OL}	I_{OL} = 0.5 mA	—	—	0.2 × V_{DD}		
"H" Input current		I_{IH}	V_I = V_{DD}	–1.0	—	+1.0	μA *4	*5
"L" Input current		I_{IL}	V_I = 0 V	–3.0	—	+3.0		
Input capacitance		C_I	Tj=25°C F=10kHz	—	8	12	pF *	1, *2
V1 output voltage temperature gradient		V1TC	Tj = 25°C V1 = 12 V	–0.03	–0.05	–0.08	%/°C	V1
Reference voltage		V_{REG}	Tj = 25°C	2.925	3.00	3.075	V	V_{RS}
V1 output voltage		V1	*6	10.58	10.85	11.12	V	V1
Voltage multiplier output voltage		V_{OUT}	3-time multiplication *7	13.0	—	—	V	V_{OUT}
			4-time multiplication *8	15.9	—	—	V	V_{OUT}
V_{OUT} - V1 voltage		Vot1	*9	0.6	—	—	V	V_{OUT}, V1
LCD driver ON resistance		R_{ON}	I_O = ±50 μA	—	—	10	kΩ	SEG1 to 131, COMS0, COMS1, COM0 to 47
Oscillator frequency	Internal oscillation	f_{OSC}	Tj = 25°C	27	33	39	kHz	*10
				21	—	47	kHz	
	External input	f_{EXT}		14	17	20	kHz	CL*10

*1: DB0 to DB5, DB7 (SI), FR, $\overline{DOF}$ Pins

*2: A0, $\overline{CS1}$, CS2, CLS, M/$\overline{S}$, C86, P/$\overline{S}$, IRS,$\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{RES}$, CL, DB6 (SCL) Pins

*3: DB0 to DB7, FR, FRS, $\overline{DOF}$, CL Pins

*4: A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/$\overline{S}$, C86, P/$\overline{S}$, $\overline{RES}$, IRS Pins

*5: Applicable to the pins DB0 to DB5, DB6 (SCL), DB7 (SI), CL, FR, $\overline{DOF}$ in the high impedance state.

*6: Tj = 25°C, α = 31, (1+Rb/Ra) = 4, V_{OUT} = 13.5 V (External input), LCD drive output = no-load

*7: V_{IN} = 4.8 V, voltage multiplier capacitor C1 = 2.6 to 4.0 μF, voltage multiplier output load current I = 500 μA. Only a voltage multiplier circuit operates, not activating the voltage adjustment circuit and V/F circuit, by command "2C".

*8: V_{IN} = 4.5 V, voltage multiplier capacitor C1 = 2.6 to 4.0 μF, voltage multiplier output load current I = 500 μA. Only a voltage multiplier circuit operates, not activating the voltage adjustment circuit and V/F circuit, by command “2C”.

*9: V1 load current I = 400 μA. 8 V is externally input to $V_{OUT.}$
The voltage adjustment circuit and V/F circuit operate by command “2B”. LCD output = no load

*10: See Table 1 for the relationship between the oscillator frequency and the frame frequency.

Table 1. Relationship among the oscillator frequency (f_{OSC}), external input frequency (f_{EXT}) display clock frequency (f_{LCDCK}), and LCD frame frequency (f_{FR})

Parameter		Display clock frequency (f_{LCDCK})	LCD frame frequency (f_{FR})
ML9059E	When the internal oscillator is used	$f_{OSC}/8$	$f_{OSC}/(8 \times 49)$
	When the internal oscillator is not used	$f_{EXT}/4$ f	$_{EXT}/(4\times 49)$

• Operating current consumption value

(1) During display operation, internal power supply OFF (The current flowing through V_{DD} with V1 to V5 externally applied when an external power supply is used, not including the current for the LCD drive)

[V$_{SS}$ = 0 V, Tj = 25°C]

Display mode	Symbol	Condition	Rated value			Unit
			Min	Typ	Max	
All-white I	$_{DD}$	V_{DD} = 5 V, V1- V_{SS} = 11 V, no load	—	16	45	μA
		V_{DD} = 3.7 V, V1- V_{SS} = 8 V, no load	—	12	35	
Checker pattern	I_{DD}	V_{DD} = 5 V, V1- V_{SS} = 11 V, no load	—	16	45	μA
		V_{DD} = 3.7 V, V1- V_{SS} = 8 V, no load	—	12	35	

(2) During display operation, internal power supply ON (Total of currents flowing through V_{DD} and V_{IN})

[V$_{SS}$ = 0 V, Tj = 25°C]

Display mode	Symbol C	ondition		Rated value			Unit
				Min	Typ	Max	
All-white I	$_{DDIN}$	Frame reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load		—	100	170	μA
		Frame reversal, V_{DD}, V_{IN} = 3.7 V, 4-time voltage multiplication V1 - V_{SS}= 8 V, no load		—	110	190	
		16-line reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load	—		100	170	
Checker pattern	I_{DDIN}	Frame reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load		—	120	205	μA
		Frame reversal, V_{DD}, V_{IN} = 3.7 V, 4-time voltage multiplication V1 - V_{SS}= 8 V, no load		—	130	220	
		16-line reversal, V_{DD}, V_{IN} = 5 V, 3-time voltage multiplication V1 - V_{SS}= 11 V, no load	—		120	205	

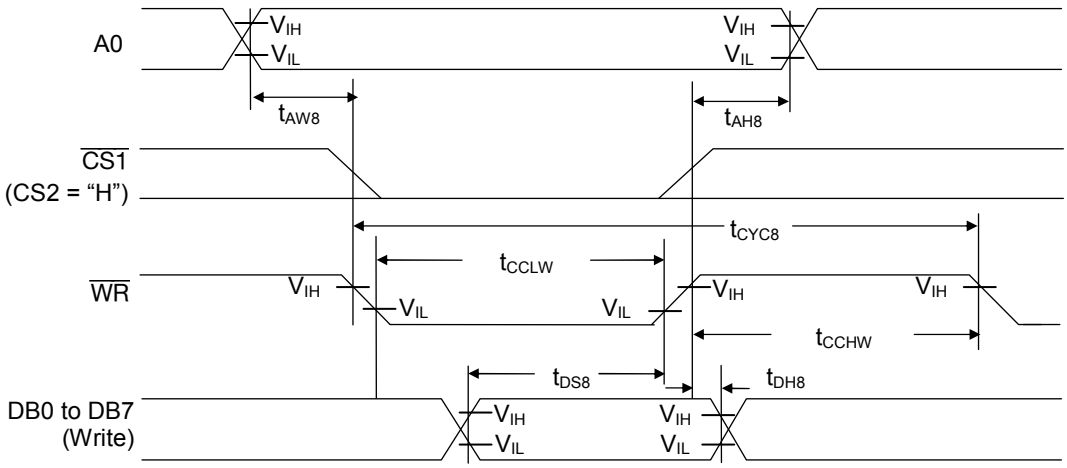
• Power save mode current consumption

[V_{SS} = 0 V, Tj = 25°C]

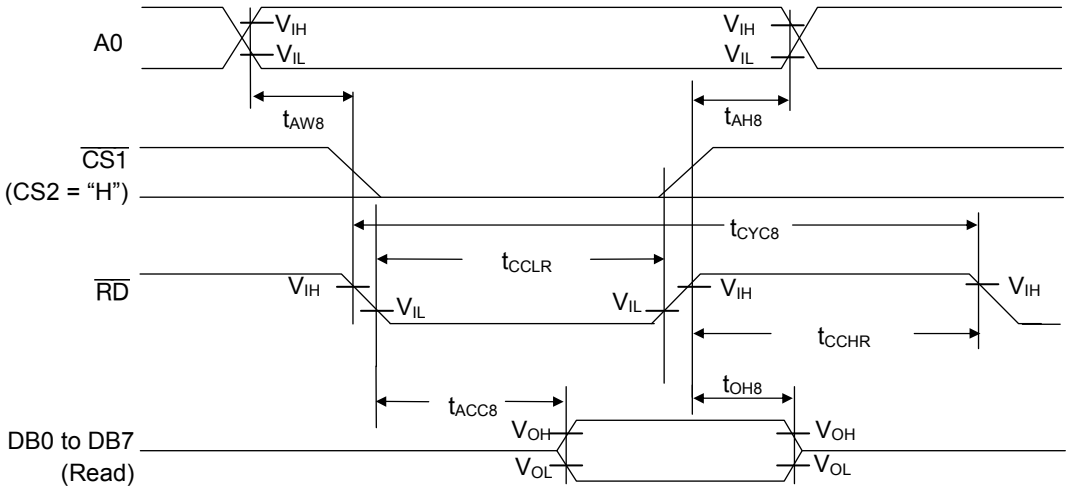
Parameter Sy	mbol	Condition	Rated value			Unit
			Min	Typ	Max	
Sleep mode	I_{DDS1}	V_{DD} = 3.7 V	—	0.3	5	μA
Standby mode	I_{DDS2}	V_{DD} = 3.7 V	—	9	15	

Parallel Interface Timing Characteristics

• System bus Write characteristics 1 (80-series MPU)



• System bus Read characteristics 1 (80-series MPU)



[V_{DD} = 4.5 to 5.5 V, Tj = –40 to +85°C]

Parameter Sy	mbol	Condition	Rated value		Unit
			Min	Max	
Address hold time	t_{AH8}		5	—	ns
Address setup time	t_{AW8}		5	—	
System cycle time	t_{CYC8}		166	—	
Control L pulse width ($\overline{WR}$) t	$_{CCLW}$		30	—	
Control L pulse width ($\overline{RD}$)	t_{CCLR}		70	—	
Control H pulse width ($\overline{WR}$)	t_{CCHW}		55	—	
Control H pulse width ($\overline{RD}$) t	$_{CCHR}$		55	—	
Data setup time	t_{DS8}		30	—	
Data hold time	t_{DH8}		10	—	
$\overline{RD}$ Access time	t_{ACC8} —	CL = 100 pF		70	
Output disable time	t_{OH8}		5 50		

[V_{DD} = 3.7 to 4.5 V, Tj = –40 to +85°C]

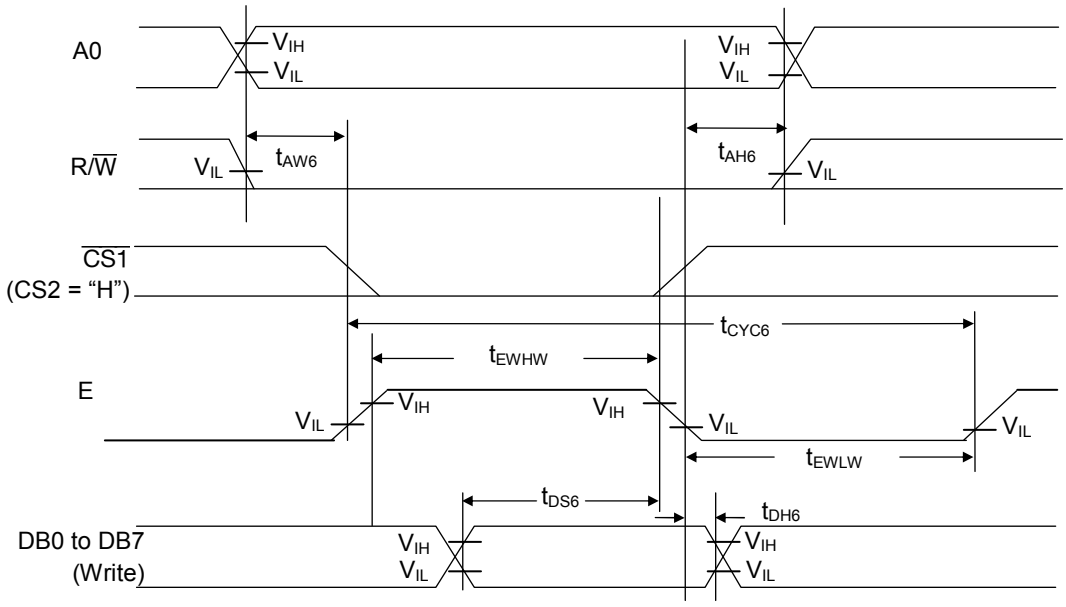
Parameter Sy	mbol	Condition	Rated value		Unit
			Min	Max	
Address hold time	t_{AH8}		5	—	ns
Address setup time	t_{AW8}		5	—	
System cycle time	t_{CYC8}		300	—	
Control L pulse width ($\overline{WR}$) t	$_{CCLW}$		60	—	
Control L pulse width ($\overline{RD}$)	t_{CCLR}		120	—	
Control H pulse width ($\overline{WR}$)	t_{CCHW}		60	—	
Control H pulse width ($\overline{RD}$) t	$_{CCHR}$		60	—	
Data setup time	t_{DS8}		40	—	
Data hold time	t_{DH8}		15	—	
$\overline{RD}$ Access time	t_{ACC8} —	CL = 100 pF		140	
Output disable time	t_{OH8}		10 100		

Note 1: The input signal rise and fall times are specified as 15ns or less.
When using the system cycle time for fast speed, the specified values are (tr + tf) ≤ (t_{CYC8} – t_{CCLW} – t_{CCHW}) or (tr + tf) ≤ (t_{CYC8} – t_{CCLR} – t_{CCHR}).

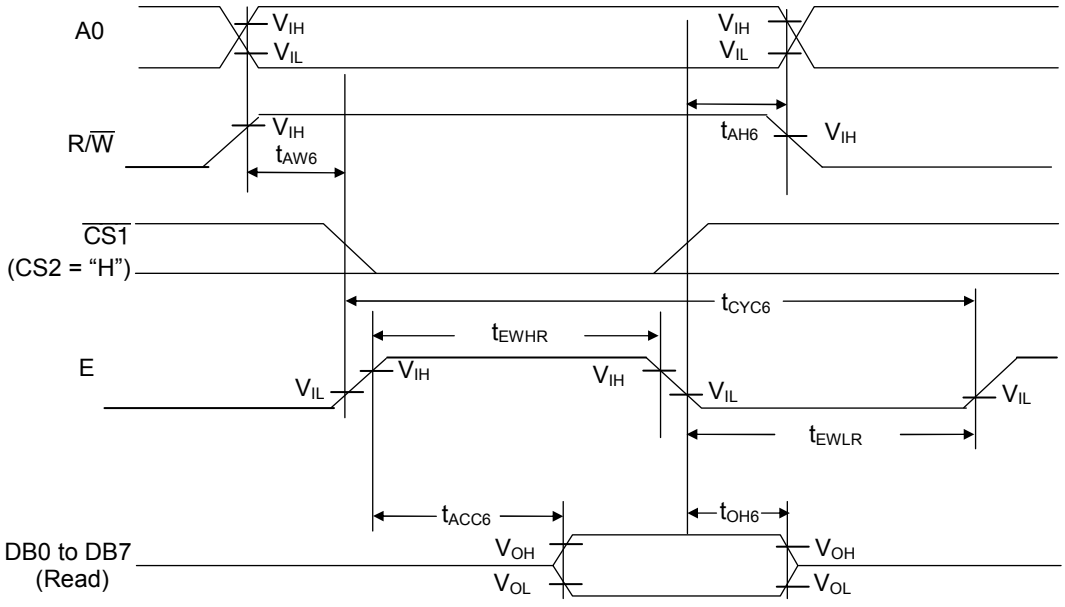
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

Note 3: The values of t_{CCLW} and t_{CCLR} are specified during the overlapping period of $\overline{CS1}$ at “L” (CS2 = “H”) and the “L” levels of $\overline{WR}$ and $\overline{RD}$, respectively.

• System bus Write characteristics 2 (68-series MPU)



• System bus Read characteristics 2 (68-series MPU)



[V_{DD} = 4.5 to 5.5 V, Tj = –40 to +85°C]

Parameter Sy		mbol	Condition	Rated value		Unit
				Min	Max	
Address hold time		t_{AH6}		5	—	ns
Address setup time		t_{AW6}		5	—	
System cycle time		t_{CYC6}		166	—	
Data setup time		t_{DS6}		30	—	
Data hold time		t_{DH6}		10	—	
Access time		t_{ACC6}	CL = 100 pF	—	70	
Output disable time		t_{OH6}		10	50	
Enable H pulse width	Read	t_{EWHR}		70	—	
	Write	t_{EWHW}		30	—	
Enable L pulse width	Read	t_{EWLR}		60	—	
	Write t	$_{EWLW}$		60	—	

[V_{DD} = 3.7 to 4.5 V, Tj = –40 to +85°C]

Parameter Sy		mbol	Condition	Rated value		Unit
				Min	Max	
Address hold time		t_{AH6}		5	—	ns
Address setup time		t_{AW6}		5	—	
System cycle time		t_{CYC6}	300		—	
Data setup time		t_{DS6}	40		—	
Data hold time		t_{DH6}		15	—	
Access time		t_{ACC6}	CL = 100 pF	—	140	
Output disable time		t_{OH6}		10	100	
Enable H pulse width	Read t	$_{EWHR}$	120		—	
	Write t	$_{EWHW}$		60	—	
Enable L pulse width	Read t	$_{EWLR}$	60		—	
	Write t	$_{EWLW}$		60	—	

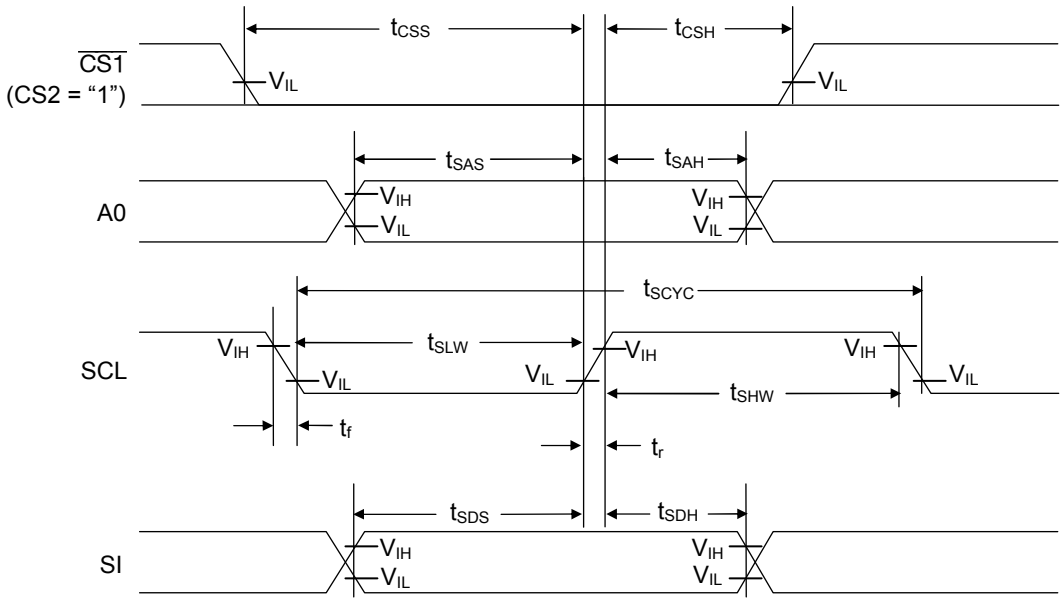
Note 1: The input signal rise and fall times are specified as 15ns or less.
When using the system cycle time for fast speed, the specified values are (tr + tf) ≤ (t_{CYC6} – t_{EWLW} – t_{EWHW}) or (tr + tf) ≤ (t_{CYC6} – t_{EWLR} – t_{EWHR}).

Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

Note 3: The values of t_{EWLW} and t_{EWLR} are specified during the overlapping period of $\overline{CS1}$ at “L” (CS2 = “H”) and the “H” level of E.

Serial Interface Timing Characteristics

• Serial interface



[V_{DD} = 4.5 to 5.5 V, Tj = –40 to +85°C]

Parameter Sy	mbol	Condition	Rated value		Unit
			Min	Max	
Serial clock period	t_{SCYC}		200	—	ns
SCL "H" Pulse width	t_{SHW}		75	—	
SCL "L" Pulse width	t_{SLW}		75	—	
Address setup time	t_{SAS}		50	—	
Address hold time	t_{SAH}		100	—	
Data setup time	t_{SDS}		50	—	
Data hold time	t_{SDH}		50	—	
CS setup time	t_{CSS}		100	—	
CS hold time	t_{CSH}		100	—	

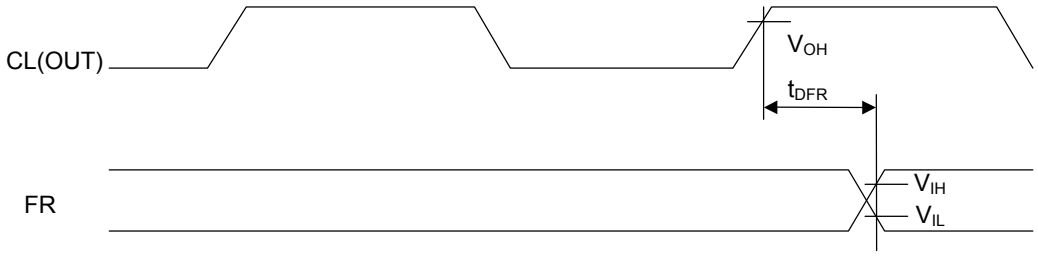
Note 1: The input signal rise and fall times are specified as 15ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

[V_{DD} = 3.7 to 4.5 V, Tj = –40 to +85°C]

Parameter Sy	mbol	Condition	Rated value		Unit
			Min	Max	
Serial clock period	t_{SCYC}		250	—	ns
SCL “H” Pulse width	t_{SHW}		100	—	
SCL “L” Pulse width	t_{SLW}		100	—	
Address setup time	t_{SAS}		150	—	
Address hold time	t_{SAH}		150	—	
Data setup time	t_{SDS}		100	—	
Data hold time	t_{SDH}		100	—	
CS setup time	t_{CSS}		150	—	
CS hold time	t_{CSH}		150	—	

Note 1: The input signal rise and fall times are specified as 15ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

• Display control output timing



[V_{DD} = 4.5 to 5.5 V, Tj = –40 to +85°C]

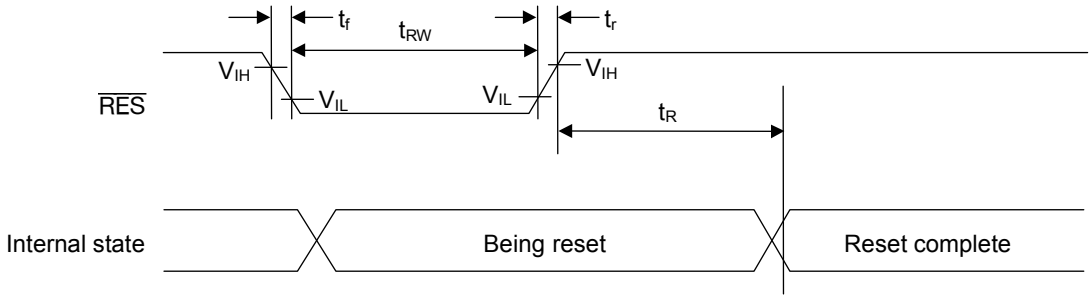
Parameter Sy	mbol	Condition	Rated value			Unit
			Min	Typ	Max	
FR Delay time	t_{DFR}	CL = 50 pF	—	10	40	ns

[V_{DD} = 3.7 to 4.5 V, Tj = –40 to +85°C]

Parameter Sy	mbol	Condition	Rated value			Unit
			Min	Typ	Max	
FR Delay time	t_{DFR}	CL = 50 pF	—	20	80	ns

Note 1: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.
Note 2: Valid only when the device operates in master mode.

• Reset input timing



[V_{DD} = 4.5 to 5.5 V, Tj = –40 to +85°C]

Parameter Sy	mbol	Condition	Rated value			Unit
			Min	Typ	Max	
Reset time	t_R		—	—	0.5	µs
Reset “L” pulse width	t_{RW}		0.5 —		—	

[V_{DD} = 3.7 to 4.5 V, Tj = –40 to +85°C]

Parameter Sy	mbol	Condition	Rated value			Unit
			Min	Typ	Max	
Reset time	t_R		—	—	1	µs
Reset “L” pulse width	t_{RW}		1 —		—	

Note 1: The input signal rise and fall times (t_r, t_f) are specified as 15 ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

PIN DESCRIPTION

Function	Pin name	Number of pins	I/O	Description
MPU Interface	DB0 to DB7	8	I/O	These are 8-bit bi-directional data bus pins that can be connected to 8-bit standard MPU data bus pins. When a serial interface is selected (P/$\overline{S}$ = "L"): DB7: Serial data input pin (SI) DB6: Serial clock input pin (SCL) In this case, DB0 to DB5 will be in the high impedance state. DB0 to DB7 will all be in the high impedance state when the chip select is in the inactive state. Fix the DB0 to DB5 pins at "H" or "L" level.
	A0	1	I	Normally, the lowest bit of the MPU address bus is connected and used for distinguishing between data and commands. A0 = "H": Indicates that DB0 to DB7 is display data. A1 = "L": Indicates that DB0 to DB7 is control data.
	$\overline{RES}$	1	I	Initial setting is made by making $\overline{RES}$ = "L". The reset operation is made during the active level of the $\overline{RES}$ signal.
	$\overline{CS1}$ CS2	2	I	These are the chip select signals. The Chip Select of the LSI becomes active when $\overline{CS1}$ is "L" and also CS2 is "H" and allows the input/output of data or commands.
	$\overline{RD}$ (E)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This pin is connected to the $\overline{RD}$ signal of the 80-series MPU, and the data bus of the ML9059E goes into the output state when this signal is "L". The active level of this signal is "H" when connected to a 68-series MPU. This pin will be the Enable and clock input pin when connected to a 68-series MPU. When a serial interface is selected (P/$\overline{S}$ = "L"), fix this pin at "H" or "L" level.
	$\overline{WR}$ (R/$\overline{W}$)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This pin is connected to the $\overline{WR}$ signal of the 80-series MPU. The data on the data bus is latched into the ML9059E at the rising edge of the $\overline{WR}$ signal. When connected to a 68-series MPU, this pin becomes the input pin for the Read/Write control signal. R/$\overline{W}$ = "H": Read, R/$\overline{W}$ = "L": Write When a serial interface is selected (P/$\overline{S}$ = "L"), fix this pin at "H" or "L" level.
	C86	1	I	This is the pin for selecting the MPU interface type. C86 = "H": 68-Series MPU interface. C86 = "L": 80-Series MPU interface.

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td>MPU Interface</td><td>P/$\overline{S}$</td><td>1</td><td>I</td><td>This is the pin for selecting parallel data input or serial data input.
P/$\overline{S}$ = “H”: Parallel data input.
P/$\overline{S}$ = “L”: Serial data input.
The pins of the LSI have the following functions depending on the state of P/$\overline{S}$ input.
<table>
<tr><th>P/$\overline{S}$</th><th>Data/command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>DB0 to DB7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>—</td><td>SCL(DB6)</td></tr>
</table>
During serial data input, it is not possible to read the display data in the RAM</td></tr>
<tr><td>Oscillator circuit</td><td>CLS</td><td>1</td><td>I</td><td>This is the pin for selecting whether to enable or disable the internal oscillator circuit for the display clock.
CLS = “H”: The internal oscillator circuit is enabled.
CLS = “L”: The internal oscillator circuit is disabled (External input).
When CLS = “L”, the display clock is input at the pin CL.</td></tr>
<tr><td>Display timing generator circuit</td><td>M/$\overline{S}$</td><td>1</td><td>I</td><td>This is the pin for selecting whether master operation or slave operation is made towards the ML9059E. During slave operation, the synchronization with the LCD display system is achieved by inputting the timing signals necessary for LCD display.
M/$\overline{S}$ = “H”: Master operation
M/$\overline{S}$ = “L”: Slave operation
The functions of the different circuits and pins will be as follows depending on the states of M/$\overline{S}$ and CLS signals.
<table>
<tr><th>M/$\overline{S}$</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>$\overline{DOF}$</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="4">Display timing generator circuit</td><td>CL</td><td>1</td><td>I/O</td><td>This is the clock input/output pin.
The function of this pin will be as follows depending on the states of M/$\overline{S}$ and CLS signals.
<table><tr><th>M/$\overline{S}$</th><th>CLS</th><th>CL</th></tr><tr><td rowspan="2">“H”</td><td>“H”</td><td>Output</td></tr><tr><td>“L”</td><td>Input</td></tr><tr><td rowspan="2">“L”</td><td>“H”</td><td>Input</td></tr><tr><td colspan="2">“L” Input</td></tr></table>When the ML9059E is used in the master/slave mode, the corresponding CL pin has to be connected.</td></tr>
<tr><td>FR</td><td>1</td><td>I/O</td><td>This is the input/output pin for LCD display frame reversal signal.
M/$\overline{S}$ = “H”: Output
M/$\overline{S}$ = “L”: Input
When the ML9059E is used in the master/slave mode, the corresponding FR pin has to be connected.</td></tr>
<tr><td>$\overline{DOF}$</td><td>1</td><td>I/O</td><td>This is the blanking control pin for the LCD display.
M/$\overline{S}$ = “H”: Output
M/$\overline{S}$ = “L”: Input
When the ML9059E is used in the master/slave mode, the corresponding $\overline{DOF}$ pin has to be connected.</td></tr>
<tr><td>FRS</td><td>1</td><td>O</td><td>This is the output pin for static drive.
This pin is used in combination with the FR pin.</td></tr>
<tr><td rowspan="4">Power supply circuit</td><td>IRS</td><td>1</td><td>I</td><td>This is the pin for selecting the resistor for adjusting the voltage V1.
IRS = “H”: The internal resistor is used.
IRS = “L”: The internal resistor is not used. The voltage V1 is adjusted using the external potential divider resistors connected to the pins VR. This pin is effective only in the master operation. This pin is tied to the “H” or the “L” level during slave operation.</td></tr>
<tr><td>V_{DD}</td><td>12</td><td>—</td><td>These pins are tied to the MPU power supply pin V_{CC}.</td></tr>
<tr><td>V_{SS}</td><td>12</td><td>—</td><td>These are the 0 V pins connected to the system ground (GND).</td></tr>
<tr><td>V_{IN}</td><td>5</td><td>—</td><td>These are the reference power supply pins of the voltage multiplier circuit for driving the LCD.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="9">Power supply circuit</td><td>V_{RS}</td><td>2</td><td>—</td><td>These are the test pins for the LCD power supply voltage adjustment circuit. Leave these pins open.</td></tr>
<tr><td>V_{OUT}</td><td>2</td><td>I/O</td><td>These are the output pins during voltage multiplication. Connect a capacitor between these pins and V_{SS}.</td></tr>
<tr><td>V1
V2
V3
V4
V5</td><td>10</td><td>I/O</td><td>These are the multiple level power supply pins for the LCD power supply. The voltages specified for the LCD cells are applied to these pins after resistor network voltage division or after impedance transformation using operational amplifiers. The voltages are specified taking V_{SS} as the reference, and the following relationship should be maintained among them.
$V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{SS}$
Master operation: When the power supply is ON, the following voltages are applied to V2 to V5 from the built-in power supply circuit. The selection of voltages is determined by the LCD bias set command.
<table>
<tr><th></th><th colspan="2">ML9059E</th></tr>
<tr><td>V2 7/8</td><td>× V1</td><td>5/6 × V1</td></tr>
<tr><td>V3 6/8</td><td>× V1</td><td>4/6 × V1</td></tr>
<tr><td>V4 2/8</td><td>× V1</td><td>2/6 × V1</td></tr>
<tr><td>V5</td><td>1/8 × V1</td><td>1/6 × V1</td></tr>
</table></td></tr>
<tr><td>VR</td><td>2</td><td>I</td><td>Voltage adjustment pins. Voltages between V1 and V_{SS} are applied using a resistance voltage divider.
These pins are effective only when the internal resistors for voltage V1 adjustment are not used (IRS = “L”).
Do not use these pins when the internal resistors for voltage V1 adjustment are used (IRS = “H”).</td></tr>
<tr><td>VS1– 3</td><td></td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for voltage multiplication.
Connect capacitors between these pins and VC3+, VC5+.</td></tr>
<tr><td>VS2– 3</td><td></td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for voltage multiplication.
Connect capacitors between these pins and VC4+, VC6+.</td></tr>
<tr><td>VC3+ 3</td><td></td><td>O</td><td>These are the input pins for voltage multiplication.
Apply the voltage equal to V_{IN} to the pins or leave them open, depending on voltage multiplication values.</td></tr>
<tr><td>VC4+ 3</td><td></td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins.
For 3-time voltage multiplication, the pins are configured as inputs for voltage multiplication.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="2">Power supply circuit</td><td>VC5+</td><td>3</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS1– and these pins.
For 2-time voltage multiplication, the pins are configured as inputs for voltage multiplication.</td></tr>
<tr><td>VC6+</td><td>3</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins.</td></tr>
<tr><td rowspan="3">LCD Drive output</td><td>SEG0 to SEG131</td><td>132</td><td>O</td><td>These are the LCD segment drive outputs.
One of the levels among V1, V3, V4, and V_{SS} is selected depending on the combination of the display RAM content and the FR signal
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Forward display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V1</td><td>V3</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V4</td></tr>
<tr><td>L</td><td>H</td><td>V3</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{SS}</td></tr>
</table>
The output voltage is V_{SS} when the Display OFF command is executed.</td></tr>
<tr><td>COM0 to COM47</td><td>48</td><td>O</td><td>These are the LCD common drive outputs.
One of the levels among V1, V2, V5, and V_{SS} is selected depending on the combination of the scan data and the FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V1</td></tr>
<tr><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>L</td><td>V5</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{SS}</td></tr>
</table>
The output voltage is V_{SS} when the Display OFF command is executed.</td></tr>
<tr><td>COMS0
COMS1</td><td>2</td><td>O</td><td>These are the common output pins only for indicators. Both pins output the same signal. Leave these pins open when they are not used. The same signal is output in both master and slave operation modes.</td></tr>
<tr><td>Test pin</td><td>TEST1</td><td>1</td><td>O</td><td>These are the pins for testing the IC chip. Leave these pins open during normal use.</td></tr>
<tr><td rowspan="2">—</td><td>DUMMY</td><td>67</td><td rowspan="2">—</td><td rowspan="2">Leave this pin open.</td></tr>
<tr><td>DUMMY-B</td><td>11</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MPU Interface

MPU R	ead mode	Write mode
80-Series	Pin $\overline{RD}$ = "L"	Pin $\overline{WR}$ = "L"
68-Series	Pin R/$\overline{W}$ = "H" Pin E = "H"	Pin R/$\overline{W}$ = "L" Pin E = "H"

In the case of the 80-series MPU interface, a command is started by applying a low pulse to the $\overline{RD}$ pin or the $\overline{WR}$ pin.
In the case of the 68-series MPU interface, a command is started by applying a high pulse to the E pin.

• Selection of interface type
The ML9059E carries out data transfer using either the 8-bit bi-directional data bus (DB0 to DB7) or the serial data input line (SI). Either the 8-bit parallel data input or serial data input can be selected as shown in Table 2 by setting the P/$\overline{S}$ pin to the "H" or the "L" level.

Table 2 Selection of interface type (parallel/serial)

P/$\overline{S}$	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	DB0 to DB5
H: Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	DB0 to DB5
L: Serial input	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	—

A hyphen (—) indicates that the pin can be tied to the "H" or the "L" level.

• Parallel interface
When the parallel interface is selected, (P/$\overline{S}$ = "H"), it is possible to connect this LSI directly to the MPU bus of either an 80-series MPU or a 68-series MPU as shown in Table 3. depending on whether the pin C86 is set to "H" or "L".

Table 3 Selection of MPU during parallel interface (80–/68–series)

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	DB0 to DB7
H: 68-Series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	DB0 to DB7
L: 80-Series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	DB0 to DB7

The data bus signals are identified as shown in Table 4 below depending on the combination of the signals A0, $\overline{RD}$ (E), and $\overline{WR}$ (R/$\overline{W}$) of Table 3.

Table 4 Identification of data bus signals during parallel interface

	Common 68-Seri es		80-Series	
	A0 R/	$\overline{W}$	$\overline{RD}$	$\overline{WR}$
Display data read	1	1	0	1
Display data write	1	0	1	0
Status read	0	1	0	1
Control data write (command)	0	0	1	0

Serial Interface

When the serial interface is selected (P/$\overline{S}$ = "L"), the serial data input (SI) and the serial clock input (SCL) can be accepted if the chip is in the active state ($\overline{CS1}$ = "L" and CS2 = "H"). The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data is read in from the serial data input pin in the sequence DB7, DB6, ... , DB0 at the rising edge of the serial clock input, and is converted into parallel data at the rising edge of the 8th serial clock pulse and processed further. The identification of whether the serial data is display data or command is judged based on the A0 input, and the data is treated as display data when A0 is "H" and as command when A0 is "L". The A0 input is read in and identified at the rising edge of the (8 × n) th serial clock pulse after the chip has become active. Fig. 1 shows the signal chart of the serial interface. (When the chip is not active, the shift register and the counter are reset to their initial states. No data read out is possible in the case of the serial interface. It is necessary to take sufficient care about wiring termination reflection and external noise in the case of the SCL signal. We recommend verification of operation in an actual unit.)

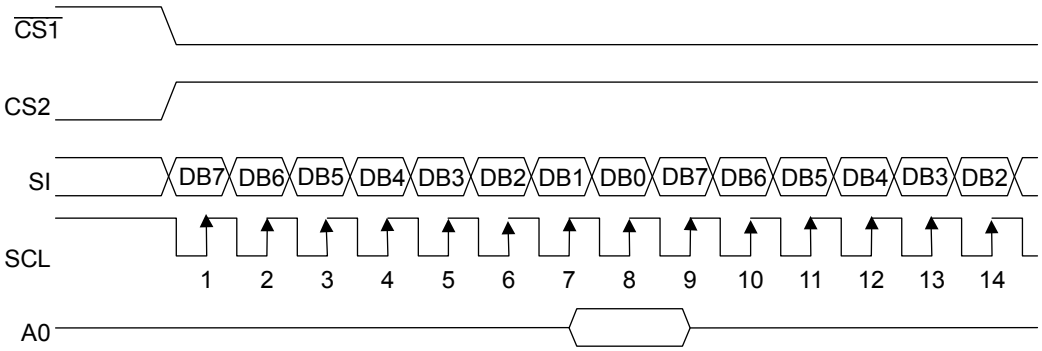


Fig. 1 Signal chart during serial interface

• Chip select

The ML9059E has the two chip select pins $\overline{CS1}$ and CS2, and the MPU interface or the serial interface is enabled only when $\overline{CS1}$ = "L" and CS2 = "H". When the chip select signals are in the inactive state, the DB0 to DB7 lines will be in the high impedance state and the inputs A0, $\overline{RD}$, and $\overline{WR}$ will not be effective. When the serial interface has been selected, the shift register and the counter are reset when the chip select signals are in the inactive state.

• Accessing the display data RAM and the internal registers

Accessing the ML9059E from the MPU side requires merely that the cycle time (t_{CYC}) be satisfied, and high speed data transfer without requiring any wait time is possible. Also, during the data transfer with the MPU, the ML9059E carries out a type of pipeline processing between LSIs via a bus holder associated with the internal data bus. For example, when the MPU writes data in the display data RAM, the data is temporarily stored in the bus holder, and is then written into the display data RAM before the next data read cycle. Further, when the MPU reads out data in the display data RAM, first a dummy data read cycle is carried out to temporarily store the data in the bus holder which is then placed on the system bus and is read out during the next read cycle. There is a restriction on the read sequence of the display data RAM, which is that the read instruction immediately after setting the address does not read out the data of that address, but that data is output as the data of the address specified during the second data read sequence, and hence care should be taken about this during reading. Therefore, always one dummy read is necessary immediately after setting the address or after a write cycle: (The status read cannot use dummy read cycles.) This relationship is shown in Figs 2(a) and 2(b).

• Data write

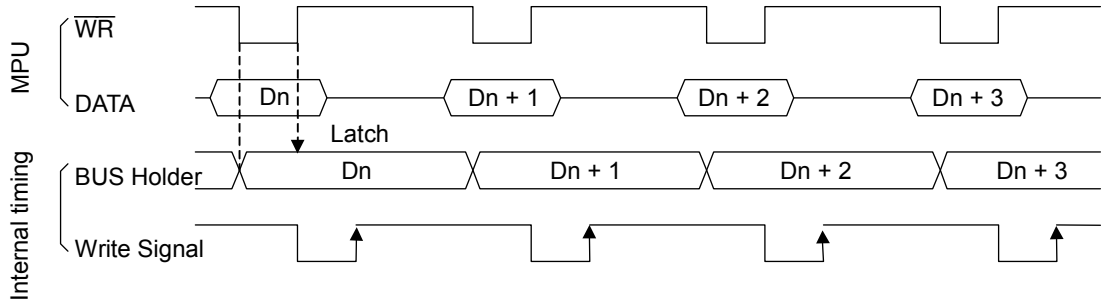


Fig. 2(a) Write sequence of display data RAM

• Data read

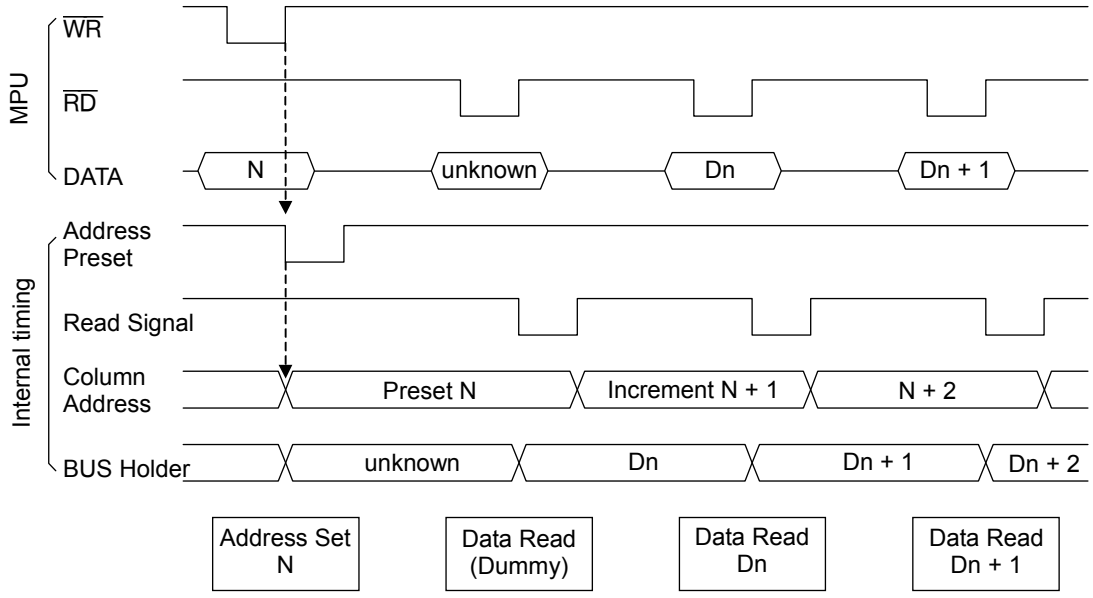


Fig. 2(b) Read sequence of display data RAM

Dn = Data

N = Address data

• Busy flag

The busy flag being "1" indicates that the ML9059E is carrying out reset operations, and hence no instruction other than a status read instruction is accepted during this period. The busy flag is output at pin DB7 when a status read instruction is executed.

Display Data RAM

• Display data RAM

This is the RAM storing the dot data for display and has an organization of 65 (8 pages × 8 bits +1) × 132 bits. It is possible to access any required bit by specifying the page address and the column address. Since the display data DB7 to DB0 from the MPU corresponds to the LCD display in the direction of the common lines as shown in Fig. 3, there are fewer restrictions during display data transfer when the ML9059E is used in a multiple chip configuration, thereby making it easily possible to realize a display with a high degree of freedom. Also, since the display data RAM read/write from the MPU side is carried out via an I/O buffer, it is done independent of the signal read operation for the LCD drive. Consequently, the display is not affected by flickering, etc., even when the display data RAM is accessed asynchronously during the LCD display operation.

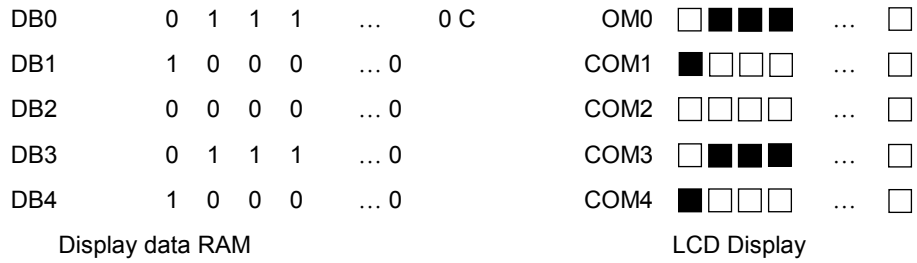


Fig. 3 Relationship between display data RAM and LCD display

• Page address circuit

The page address of the display data RAM is specified using the page address set command as shown in Fig. 4. Specify the page address again when accessing after changing the page. The page address 8 (DB3, DB2, DB1, DB0 → 1, 0, 0, 0) is the RAM area dedicated to the indicator, and only the display data DB0 is valid in this page.

• Column address circuit

The column address of the display data RAM is specified using the column address set command as shown in Fig. 4. Since the specified column address is incremented (by +1) every time a display data read/write command is issued, the MPU can access the display data continuously. Further, the incrementing of the column address is stopped at the column address of 83(H). Since the column address and the page address are independent of each other, it is necessary, for example, to specify separately the new page address and the new column address when changing from column 83(H) of page 0 to column 00(H) of page 1. Also, as is shown in Table 5, it is possible to reverse the correspondence relationship between the display data RAM column address and the segment output using the ADC command (the segment driver direction select command). This reduces the IC placement restrictions at the time of assembling LCD modules.

Table 5 Correspondence relationship between the display data RAM column address and the segment output

ADC	SEGMENT Output				
	SEG0				SEG131
DB0 = "0"	0(H)	→	Column Address	→	83(H)
DB0 = "1"	83(H)	←	Column Address	←	0(H)

• Line address circuit
The line address circuit is used for specifying the line address corresponding to the common output when displaying the contents of the display data RAM as is shown in Fig. 4. Normally, the topmost line in the display is specified using the display start line address set command (COM0 output in the forward display state of the common output, and COM47 output in the reverse display state). The display area is 48 lines in the direction of increasing line address from the specified display start line address. When the indicator–dedicated common output pin (COMS) is selected, data in Line Address 40 H = page 8 and bit 0 is displayed irrespective of the display start line address. COMS selection is 49th in order.
It is possible to carry out screen scrolling by dynamically changing the line address using the display start line address set command.

• Display data latch circuit
The display data latch circuit is a latch for temporarily storing the data from the display data RAM before being output to the LCD drive circuits. Since the commands for selecting forward/reverse display and turning the display ON/OFF control the data in this latch, the data in the display data RAM will not be changed.

Oscillator Circuit

This is an RC oscillator that generates the display clock. The oscillator circuit is effective only when M/$\overline{S}$ = "H" and also CLS = "H". The oscillations will be stopped when CLS = "L", and the display clock has to be input to the CL pin.

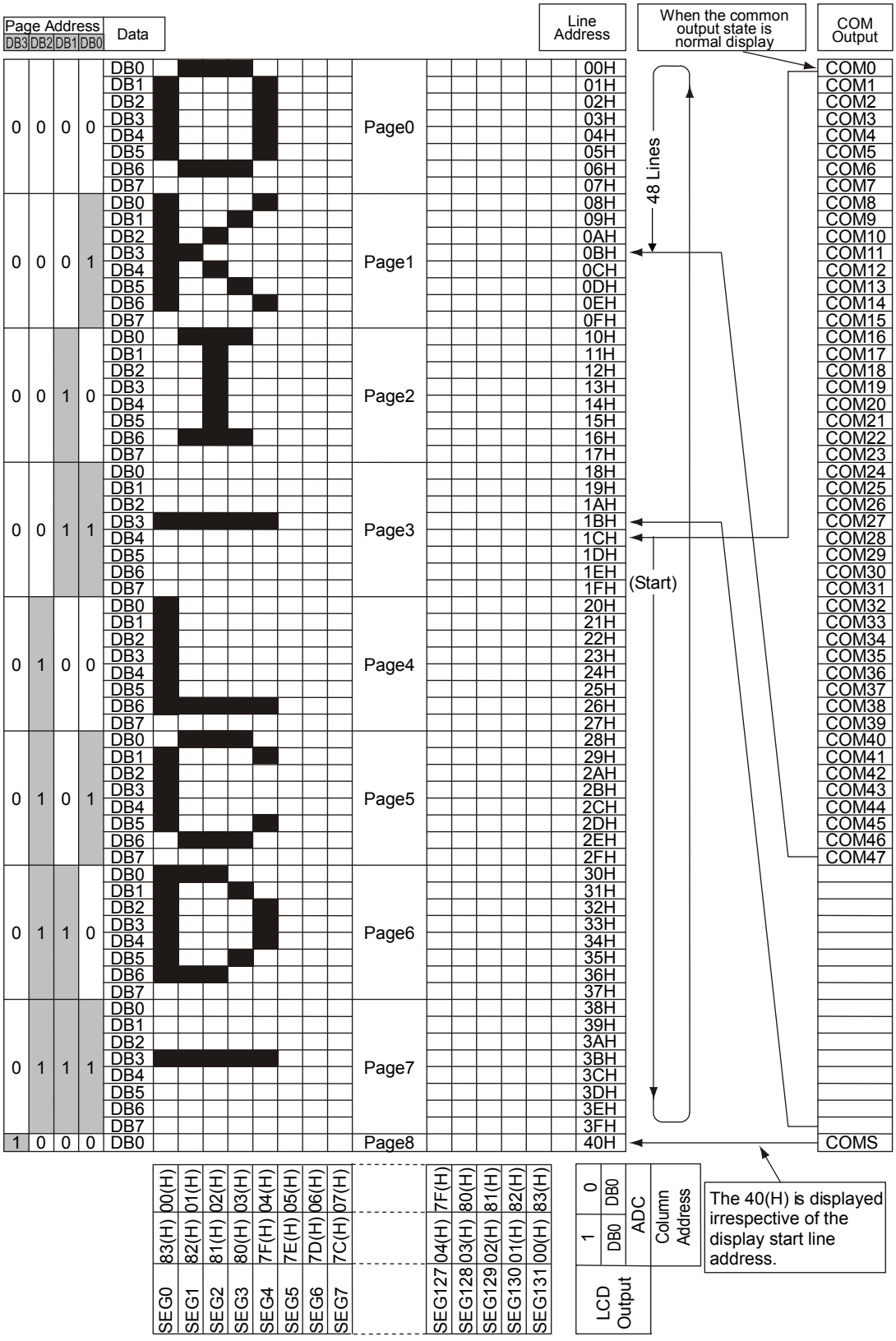


Fig. 4 Display data RAM address map

Display Timing Generator Circuit

This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. The read out of the display data to the LCD drive circuits is completely independent of the display data RAM access from the MPU. As a result, there is no bad influence such as flickering on the display even when the display data RAM is accessed asynchronously during the LCD display. Also, the internal common timing and LCD frame reversal (FR) signals are generated by this circuit from the display clock. The drive waveforms of the frame reversal drive method shown in Fig. 5(a) for the LCD drive circuits are generated by this circuit. The drive waveforms of the line reversal drive method shown in Fig. 5(b) are also generated by the command.

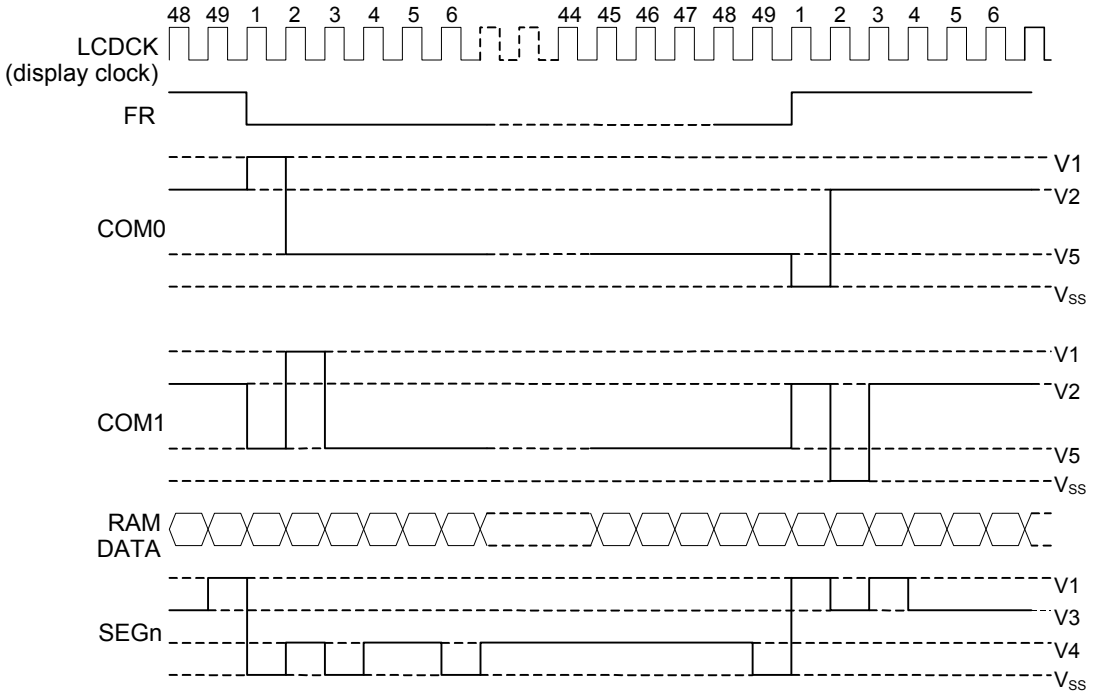


Fig. 5(a) Waveforms in the frame reversal drive method

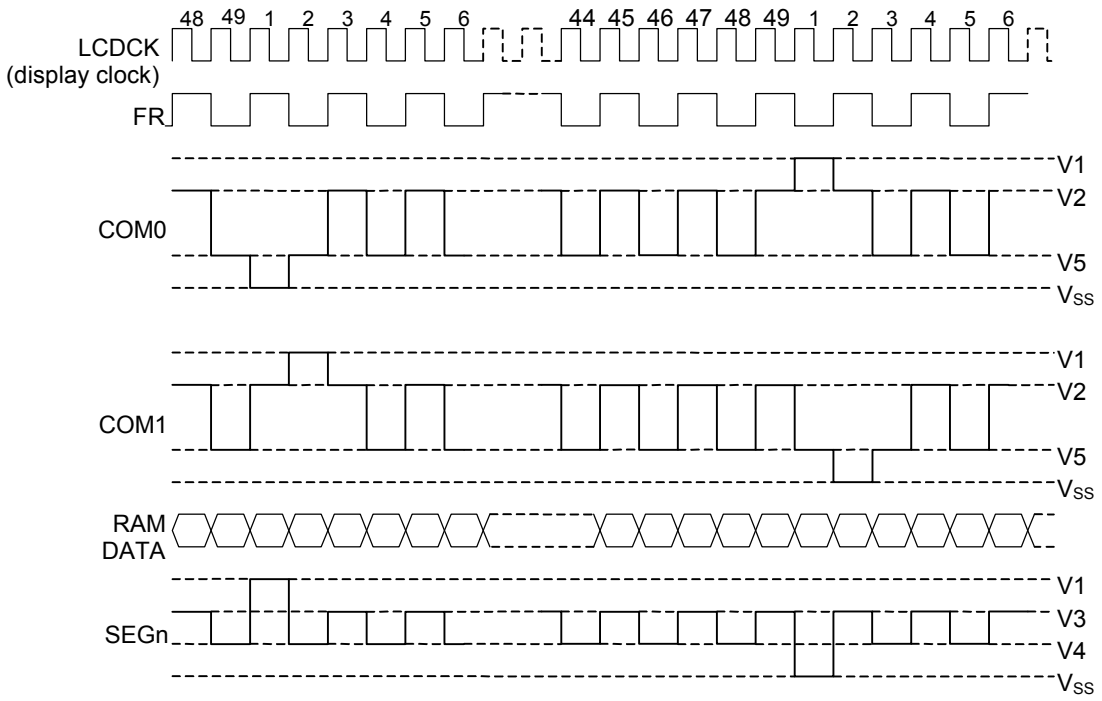


Fig. 5(b) Waveforms in the line reversal drive method

When the ML9059E is used in a multiple chip configuration, it is necessary to supply the slave side display timing signals (FR, CL, and $\overline{DOF}$) from the master side. However, when the line reversal drive is set, the ML9059E is not used in a multiple chip configuration.
The statuses of the signals FR, CL, and $\overline{DOF}$ are shown in Table 6.

Table 6 Display timing signals in master mode and slave mode

Operating mode		FR	CL	$\overline{DOF}$
Master mode (M/$\overline{S}$ = "H")	Internal oscillator circuit enabled (CLS = H)	Output	Output	Output
	Internal oscillator circuit disabled (CLS = L)	Output	Input	Output
Slave mode (M/$\overline{S}$ = "L")	Internal oscillator circuit disabled (CLS = H)	Input	Input	Input
	Internal oscillator circuit disabled (CLS = L)	Input	Input	Input

Note: During master mode, the oscillator circuit operates from the time the power is applied. The oscillator circuit can be stopped only in the sleep state.

Common Output State Selection Circuit (See Table 7)

Since the common output scanning directions can be set using the common output state selection command in the ML9059E, it is possible to reduce the IC placement restrictions at the time of assembling LCD modules.

Table 7 Common output state settings

State C	ommon Scanning direction
Forward Display	COM0 → COM47
Reverse Display	COM47 → COM0

LCD Drive Circuit

This LSI incorporates 181 sets of multiplexers for the ML9059E, that generate 4-level outputs for driving the LCD. These output the LCD drive voltage in accordance with the combination of the display data, common scanning signals, and the FR signal. Fig. 6 shows examples of the segment and common output waveforms in the frame reversal drive method.

Static Indicator Circuit

The FR pin is connected to one side of the LCD drive electrode of the static indicator and the FRS pin is connected to the other side.
The static indicator display is controlled by a command only independently of other display control commands.
The electrode of the static indicator should has a wiring pattern that is distant from the dynamic drive electrode.
If the wiring pattern is placed too near to the dynamic drive electrode, the LCD and electrode may be degraded.

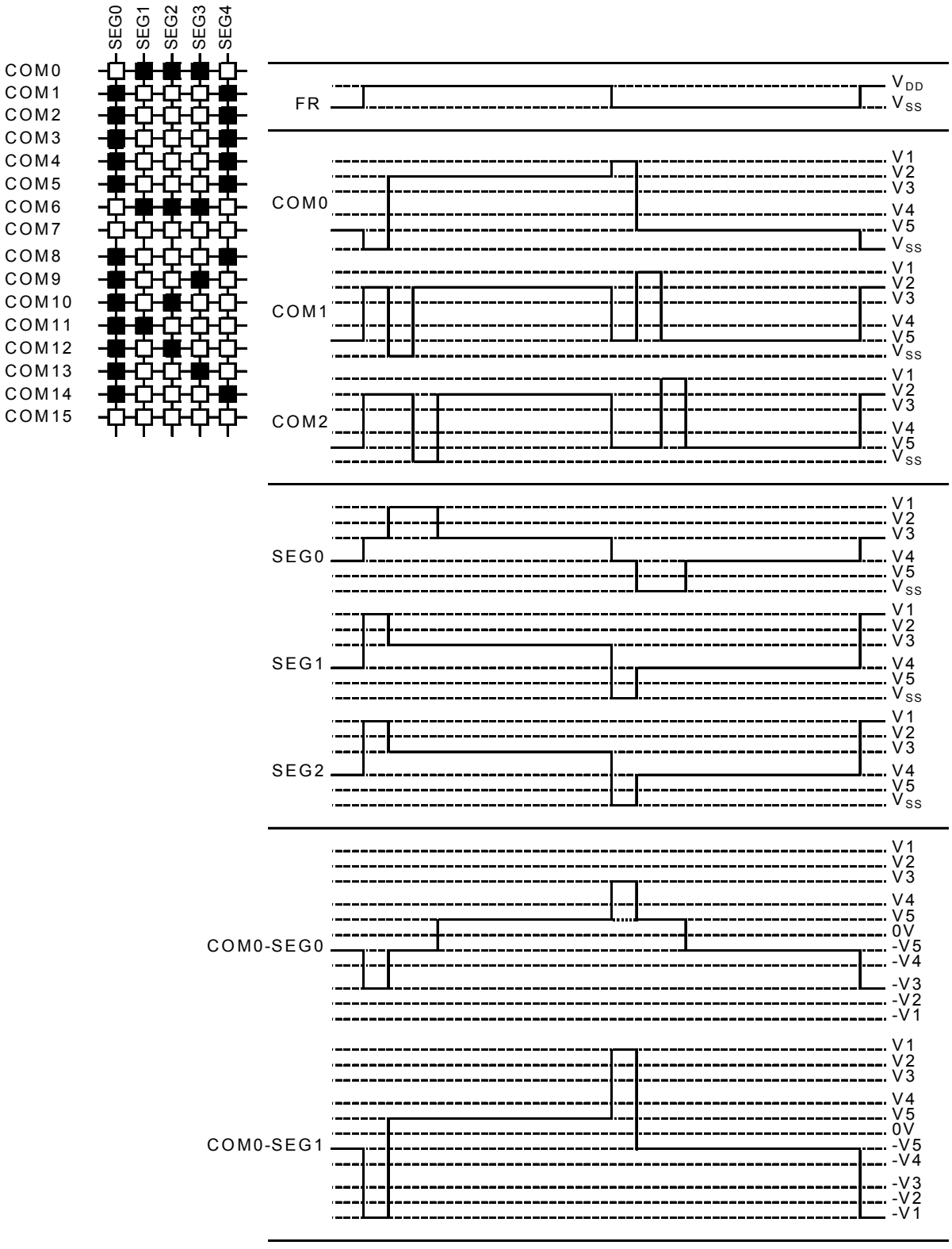


Fig. 6 Output waveforms in the frame reversal drive method (FR waveform/common waveform/segment waveform/voltage difference between common and segment)

Power Supply Circuit

This is the low power consumption type power supply circuit for generating the voltages necessary for driving LCD devices, and consists of voltage multiplier circuits, voltage adjustment circuits, and voltage follower circuits. In the power supply circuit, it is possible to control the ON/OFF of each of the circuits of the voltage multiplier, voltage adjustment circuits, and voltage follower circuits using the power control set command. As a result, it is also possible to use parts of the functions of both the external power supply and the internal power supply. Table 8 shows the functions controlled by the 3-bit data of the power control set command and Table 9 shows a sample combination.

Table 8 Details of functions controlled by the bits of the power control set command

Control bit	Function controlled by the bit
DB2	Voltage multiplier circuit control bit
DB1	Voltage adjustment circuit (V1 voltage adjustment circuit) control bit
DB0	Voltage follower circuit (V/F circuit) control bit

Table 9 Sample combination for reference

State used	DB2	DB1	DB0	Circuit			External voltage input	Voltage multiplier pins *1
				Voltage multiplier	V Adjustment	V/F		
Only the internal power supply is used	1	1	1	○	○	○	V_{IN}	Used
Only V adjustment and V/F circuits are used	0	1	1	×	○	○	V_{OUT}	OPEN
Only V/F circuits are used	0	0	1	×	×	○	V1	OPEN
Only the external power supply is used	0	0	0	×	×	×	V1 to V5	OPEN

*1: The voltage multiplier pins are the pins VS1–, VS2–, VC3+, VC4+, VC5+, and VC6+.
If combinations other than the above are used, normal operation is not guaranteed.

• Voltage multiplier circuits

The connections for 2- to 4-time voltage multiplier circuits are shown below.

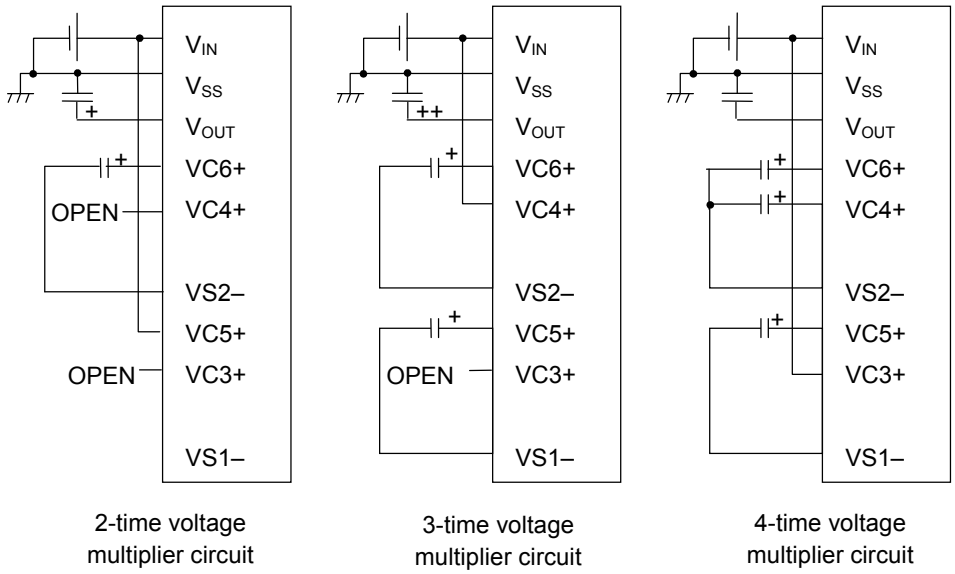


Fig. 7 Connection examples for voltage multiplier circuits

The voltage relationships in voltage multiplication are shown in Fig. 8.

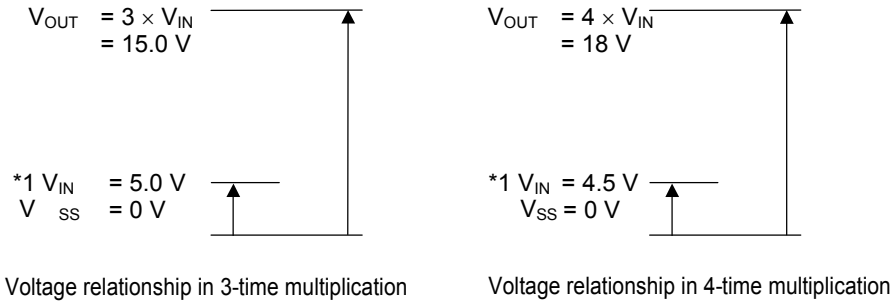


Fig. 8 Voltage relationships in voltage multiplication

*1: The voltage range of V_{IN} should be set from 6V to 18.33V so that the voltage at the pin V_{OUT} does not exceed the voltage multiplier output voltage operating range.

• Voltage adjustment circuit

The voltage multiplier output V_{OUT} produces the LCD drive voltage V1 via the voltage adjustment circuit. Since the ML9059E incorporates a high accuracy constant voltage generator, a 64-level electronic potentiometer function, and also resistors for voltage V1 adjustment, it is possible to build a high accuracy voltage adjustment circuit with very few components. In addition, the ML9059E is available with the temperature gradients of a VREG - about –0.05%/°C.

(a) When the internal resistors for voltage V1 adjustment are used

It is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands and without needing any external resistors, if the internal voltage V1 adjustment resistors and the electronic potentiometer function are used. The voltage V1 can be obtained by the following equation A-1 in the range of V1<VOUT.

$$V1 = (1 + (Rb/Ra)) \bullet VEV = (1 + (Rb/Ra)) \bullet (1 - (\alpha/324)) \bullet VREG \quad \text{(Eqn. A-1)}$$

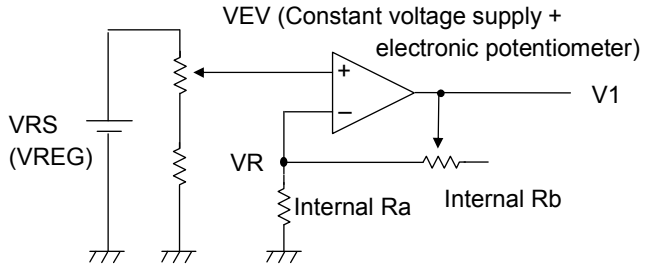


Fig. 9 V1 voltage adjustment circuit (equivalent circuit)

VREG is a constant voltage generated inside the IC and VRS pin output voltage.
Here, α is the electronic potentiometer function which allows one level among 64 levels to be selected by merely setting the data in the 6-bit electronic potentiometer register. The values of α set by the electronic potentiometer register are shown in Table 10.

Table 10 Relationship between electronic potentiometer register and α

α	DB5 DB4	DB3		DB2 DB1	DB0	
63	0 0 0			0	0	0
62	0 0 0			0	0	1
61	0 0 0			0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1 1 0		
0	1 1 1			1	1	1

Rb/Ra is the voltage V1 adjustment internal resistor ratio and can be adjusted to one of 7 levels by the voltage V1 adjustment internal resistor ratio set command. The reference values of the ratio (1 + Rb/Ra) according to the 3-bit data set in the voltage V1 adjustment internal resistor ratio setting register are listed in Table 11.

Table 11 Voltage V1 adjustment internal resistor ratio setting register values and the ratio (1+Rb/Ra) (Nominal)

Register			(1 + Rb/Ra)
DB2	DB1	DB0	
0 0		0	3.0
0 0		1	3.5
0 1		0	4.0
0 1		1	4.5
1 0		0	5.0
1 0		1	5.5
1 1		0	6.0

Note: Use V1 gain in the range from 3 to 6 times. Because this LSI has temperature gradient, V1 voltage rises at lower temperatures. When using V1 gain of 6 times, adjust the built-in electronic potentiometer so that V1 voltage does not exceed 18 V.

When V1 is set using the built-in resistance ratio, the accuracies are shown in Table 12.

Table 12 Relation between V1 Output Voltage Accuracy and V1 Gain Using Built-in Resistor

Parameter	V1 gain							Unit
	3 times	3.5 times	4 times	4.5 times	5 times	5.5 times	6 times	
V1 output voltage accuracy	±2.5	±2.5	±2.5	±2.5	±2.5	±2.5	±2.5	%
V1 maximum output voltage	9	10.5 12		13.5 15		16.5 18		V

Note: The V1 maximum output voltages in Table 12 are nominal values when Tj = 25°C and electronic potentiometer α = 0. The V1 output voltage accuracy in Table 12 are values when V1 load current I = 0 μA, 20 V is externally input to V_{OUT}, and display is turned OFF.

(b) When external resistors are used (voltage V1 adjustment internal resistors are not used)
It is also possible to set the LCD drive power supply voltage V1 without using the internal resistors for voltage V1 adjustment but connecting external resistors (Ra' and Rb') between V_{SS} & VR and between VR & V1. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.
The voltage V1 can be obtained by the following equation B-1 in the range of $V1<V_{OUT}$ by setting the external resistors Ra' and Rb' appropriately.
$V1 = (1 + (Rb'/Ra')) \bullet VEV = (1 + (Rb'/Ra')) \bullet (1 - (\alpha/324)) \bullet VREG$ (Eqn. B-1)

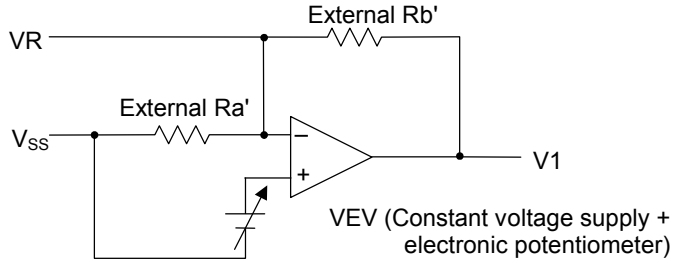


Fig. 10 V1 voltage adjustment circuit (equivalent circuit)

Setting example: Setting V1 = 7 V at Tj = 25°C
When the electronic potentiometer register value is set to the middle value of (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0), the value of α will be 31 and that of VREG will be 3.0 V, and hence the equation B-1 becomes as follows:
$V1 = (1 + (Rb'/Ra')) \bullet (1 - (\alpha/324)) \bullet VREG$
$7 = (1 + (Rb'/Ra')) \bullet (1 - (31/324)) \bullet 3.0$ (Eqn. B-2)
Further, if the current flowing through Ra' and Rb' is set as 5 μA, the value of Ra' + Rb' will be - Ra' + Rb' = 1.4 MΩ (Eqn. B-3)
and hence,
Rb'/Ra' = 1.58, Ra' = 543 kΩ, Rb' = 857 kΩ.
In this case, the variability range of voltage V1 using the electronic potentiometer function will be as given in Table 13.

Table 13 Example 1 of V1 variable-voltage range using electronic potentiometer function

V1 M	in	Typ	Max	Unit
Variable-voltage range	6.24 (α = 63)	7.0 (α = 31)	7.74 (α = 0)	[V]

(c) When external resistors are used (voltage V1 adjustment internal resistors are not used) and a variable resistor is also used

It is possible to set the LCD drive power supply voltage V1 using fine adjustment of Ra' and Rb' by adding a variable resistor to the case of using external resistors in the above case. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.

The voltage V1 can be obtained by the following equation C-1 in the range of $V1<V_{OUT}$ by setting the external resistors R_1, R_2 (variable resistor), and R_3 appropriately and making fine adjustment of R_2 (ΔR_2).

$V1 = (1 + (R_3 + R_2 - \Delta R_2)/(R_1 + \Delta R_2)) \bullet VEV$

$= (1 + (R_3 + R_2 - \Delta R_2)/(R_1 + \Delta R_2)) \bullet (1 - (\alpha/324)) \bullet VREG$ (Eqn. C-1)

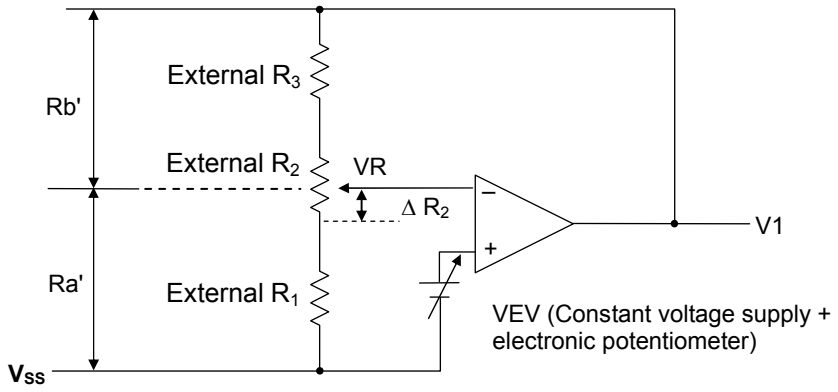


Fig. 11 V1 voltage adjustment circuit (equivalent circuit)

Setting example: Setting V1 in the range 5 V to 9 V using R_2 at Tj = 25°C .

When the electronic potentiometer register value is set to (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0, 0), the value of α will be 31 and that of VREG will be 3.0 V, and hence in order to make V1 = 9 V when $\Delta R_2 = 0\Omega$, the equation C-1 becomes as follows:

$9 = (1 + (R_3 + R_2)/R_1) \bullet (1 - (31/324)) \bullet (3.0)$ (Eqn. C-2)

In order to make V1 = 5 V when $\Delta R_2 = R_2$,

$5 = (1 + R_3/(R_1+R_2)) \bullet (1 - (31/324)) \bullet (3.0)$ (Eqn. C-3)

Further, if the current flowing between V_{SS} and V1 is set as 5 µA, the value of $R_1 + R_2 + R_3$ becomes-

$R_1 + R_2 + R_3 = 1.8\ M\Omega$ (Eqn. C-4)

and hence,

$R_1 = 542\ k\Omega$, $R_2 = 436\ k\Omega$, $R_3 = 822\ k\Omega$.

In this case, the variability range of voltage V1 using the electronic potentiometer function and the increment size will be as given in Table 13.

Table 14 Example 2 of V1 variable-voltage range using electronic potentiometer function and variable resistor

V1 M	in	Typ	Max	Unit
Variable-voltage range	4.45 (α = 63)	7.0 (α = 31)	9.96 (α = 0)	[V]

In Figures 10 and 11, the voltage VEV is obtained by the following equation by setting the electronic potentiometer between 0 and 63.

VEV = (1 - (α/324)) • VREG
α = 0: VEV = (1 – (0/324)) • 3.0 V = 3.0 V
α = 31: VEV = (1 – (31/324)) • 3.0 V = 2.712 V
α = 63: VEV = (1 – (63/324)) • 3.0 V = 2.416 V

The increment size of the electronic potentiometer at VEV when VREG = 3.0 is :

$$\Delta = \frac{3.0 \quad - 2.416}{63} = 9.27 \text{ mV (Nominal)}$$

When VREG = 3.069 V, α = 0 : VEV = 3.069 V, α = 63 : VEV = 2.472 V
The increment size is :

$$\Delta = \frac{3.069 \text{ V} - 2.472 \text{ V}}{63} = 9.476 \text{ mV}$$

When VREG = 2.931 V, α = 0 : VEV = 2.931 V, α = 63 : VEV = 2.361 V
The increment size is :

$$\Delta = \frac{2.931 \text{ V} - 2.361 \text{ V}}{63} = 9.047 \text{ mV}$$

* When using the voltage V1 adjustment internal resistors or the electronic potentiometer function, it is necessary to set at least the voltage adjustment circuit and the voltage follower circuits both in the operating state using the power control setting command. Also, when the voltage multiplier circuit is OFF, it is necessary to supply a voltage externally to the V_{OUT} pin.
* The pin VR is effective only when the voltage V1 adjustment internal resistors are not used (pin IRS = "L"). Leave this pin open when the voltage V1 adjustment internal resistors are being used (pin IRS = "H").
* Since the input impedance of the pin VR is high, it is necessary to take noise countermeasures such as using short wiring length or a shielded wire .
* The supply current increases in proportion to the panel capacitance. When power consumption increases, the V_{OUT} level may fall. The voltage (V_{OUT} – V1) should be more than 3 V.

• LCD Drive voltage generator circuits

The voltage V1 is divided using resistors inside the IC to generate the voltages V2, V3, V4, and V5 that are necessary for driving the LCD. In addition, these voltages V2, V3, V4, and V5 are impedance transformed using voltage follower circuits and fed to the LCD drive circuits. The bias ratio of 1/8 or 1/6 can be selected using the LCD bias setting command.

• At built-in power-on, and transition from power save state to display mode

After built-in power-on, at the command "2F(H)" input, or on transition from power save state to display mode, the display does not operate for a maximum period of 300 ms until the built-in power is stabilized. This period of no display is not influenced by display ON/OFF command. Despite input of display ON command during this period, the display does not operate for this period. However, the command is valid. After the wait time is finished, the display operates. (During this period of no display, all commands are acceptable.)

• Command sequence for shutting off the internal power supply

When shutting off the internal power supply, it is recommended to use the procedure given in Fig. 12 of switching OFF the power after putting the LSI in the power save state using the following command sequence.

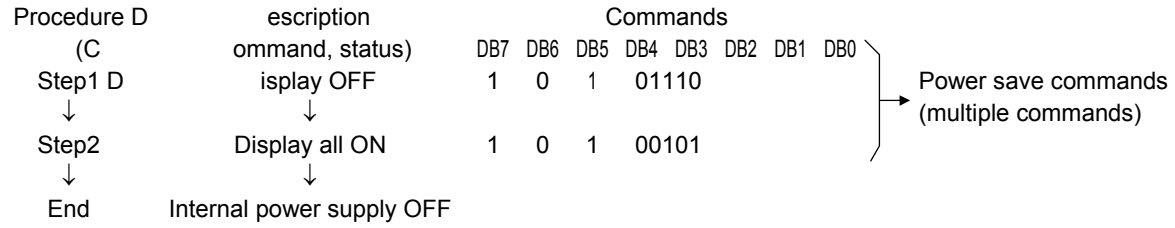


Fig. 12 Command sequence for shutting off the internal power supply

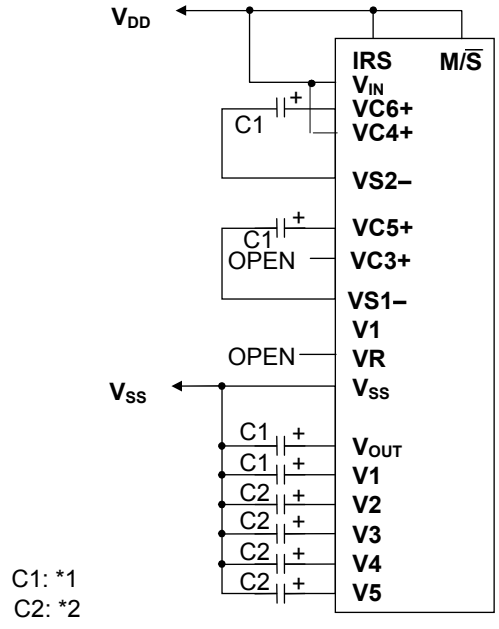
• Application circuits

(Two V1 pins are described in the following examples for explanation, but they are the same.)

(1) When the voltage multiplier circuit, voltage adjustment circuit, and V/F circuits are all used

When using the internal voltage V1 adjustment resistors

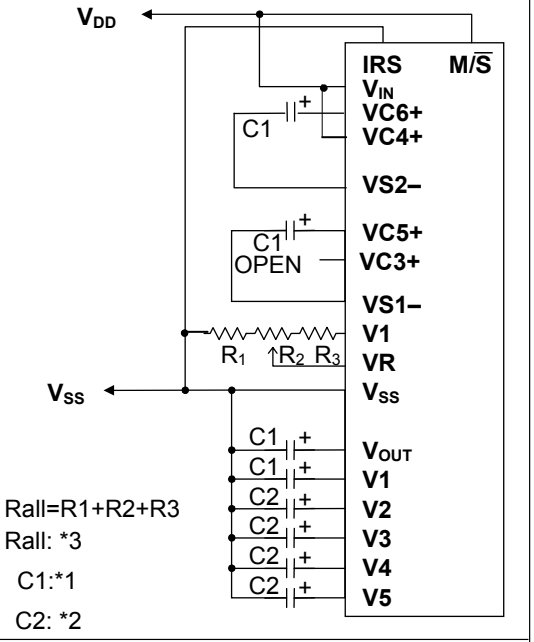
$V_{IN} = V_{DD}$ 3-time voltage multiplication



(2) When the voltage multiplier circuit, voltage adjustment circuit, and V/F circuits are all used

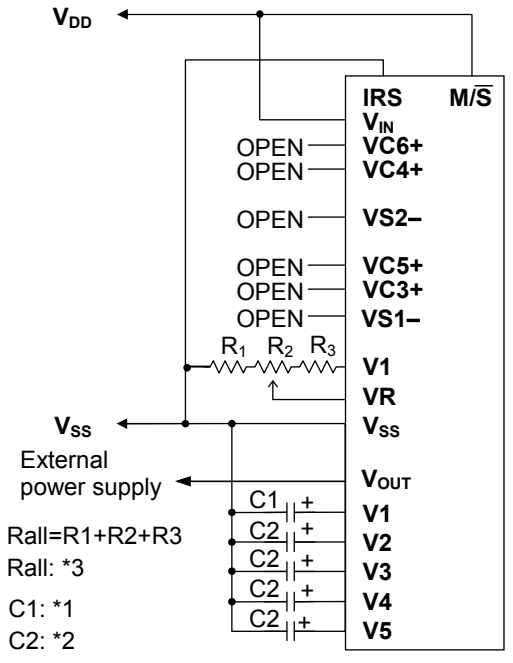
When not using the internal voltage V1 adjustment resistors

$V_{IN} = V_{DD}$ 3-time voltage multiplication



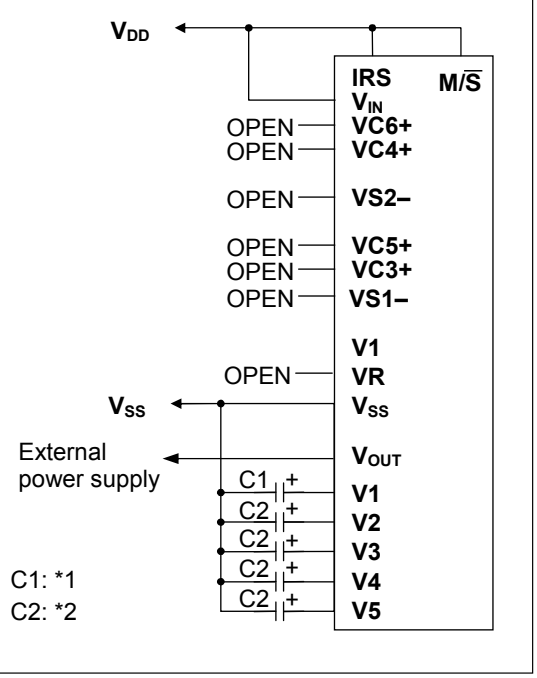
(3) When only the voltage adjustment circuit and V/F circuits are used

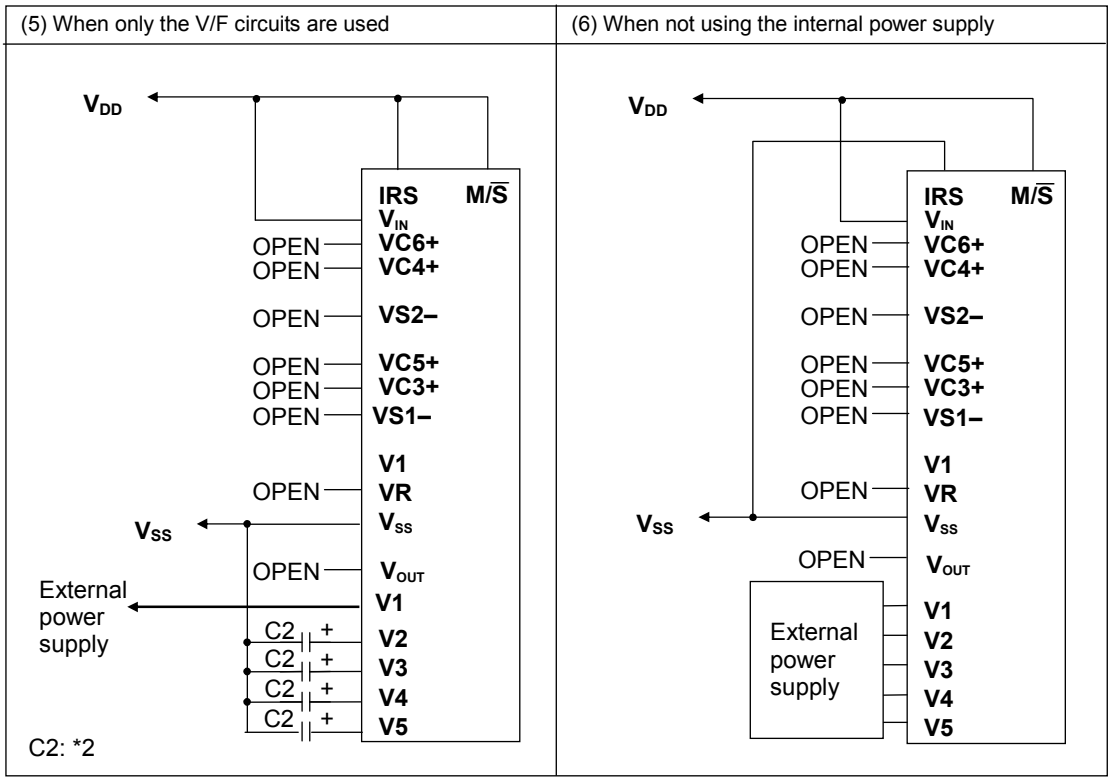
When not using the internal voltage V1 adjustment resistors



(4) When only the voltage adjustment circuit and V/F circuits are used

When using the internal voltage V1 adjustment resistors





Note: When trace resistance external to COG-mounted chip does not exist,

① when C1 (*1) = 0.9 μF to 5.7 μF, C2 (*2) = 0.42 μF to 1.2 μF, use in the range Rall (*3) = 1 MΩ to 5 MΩ.

② when C1 (*1) = 1.8 μF to 5.7 μF, C2 (*2) = 0.42 μF to 1.2 μF, use in the range Rall (*3) = 500 kΩ to 1 MΩ.

Make sure that voltage multiplier output voltage, and V1 output voltage have enough margin before using this LSI.

- Initial setting

Note: If electric charge remains in smoothing capacitor connected between the LCD driver voltage output pins (V1 to V5) and the V_{SS} pin, a malfunction might occur: the display screen gets dark for an instant when powered on.

To avoid a malfunction at power-on, it is recommended to follow the flowchart in the "EXAMPLES OF SETTINGS FOR THE INSTRUCTIONS" section in page 54.

LIST OF OPERATION

No	Operation		DBn 7 6 5 4 3 2 1 0	A0	$\overline{RD}$	$\overline{WR}$	Comment
1	Display OFF		1 0 1 0 1 1 1 0	0	1	0	LCD Display: OFF when DB0 = 0 ON when DB0 = 1
	Display ON		1 0 1 0 1 1 1 1	0	1	0	
2	Display start line set		0 1 Address	0	1	0	The display starting line address in the display RAM is set.
3	Page address set		1 0 1 1 Address	0	1	0	The page address in the display RAM is set.
4	Column address set (upper bits)		0 0 0 1 Address (upper)	0 1		0	The upper 4 bits of the column address in the display RAM is set.
	Column address set (lower bits)		0 0 0 0 Address (lower)	0 1		0	The lower 4 bits of the column address in the display RAM is set.
5	Status read		Status * * * *	0 0		1	The status information is read out from the upper 4 bits.
6	Display data write		Write data	1	1	0	Writes data to the display data RAM.
7	Display data read		Read data	1	0	1	Reads data from the display data RAM.
8	ADC select	Forward	1 0 1 0 0 0 0 0	0	1	0	Correspondence to the segment output for the display data RAM address Forward when DB0 = 0 Reverse when DB0 = 1
		Reverse	1 0 1 0 0 0 0 1	0	1	0	
9	Display	Forward	1 0 1 0 0 1 1 0	0	1	0	Forward or reverse LCD display mode Forward when DB0 = 0 Reverse when DB0 = 1
		Reverse	1 0 1 0 0 1 1 1	0	1	0	
10	LCD All-on display	OFF(Normal display)	1 0 1 0 0 1 0 0	0	1	0	LCD Normal display when DB0 = 0 All-on display when DB0 = 1
		ON	1 0 1 0 0 1 0 1	0	1	0	
11	LCD bias set		1 0 1 0 0 0 1 0	0	1	0	Sets the LCD drive voltage bias ratio. 1/8 when DB0 = 0 and 1/6 when DB0 = 1
			1 0 1 0 0 0 1 1	0	1	0	
12	Read-modify-write		1 1 1 0 0 0 0 0	0	1	0	Incrementing column address During a write: +1 During a read: 0
13	End		1 1 1 0 1 1 1 0	0	1	0	Releases the read-modify-write state.
14	Reset		1 1 1 0 0 0 1 0	0	1	0	Internal reset
15	Common output state select		1 1 0 0 0 * * *	0	1	0	Selects the common output scanning direction. Forward when DB3 = 0 Reverse when DB3 = 1
			1 1 0 0 1 * * *	0	1	0	
16	Power control set		0 0 1 0 1 Operating state	0 1		0	Selects the operating state of the internal power supply. Set the lower 3 bits.
17	Voltage V1 adjustment internal resistance ratio set		0 0 1 0 0 Resistance ratio setting	0 1		0	Selects the internal resistor ratio. Set the lower 3 bits.

No	Operation		DBn 7 6 5 4 3 2 1 0	A0	$\overline{RD}$	$\overline{WR}$	Comment
18	Electronic potentiometer	Electronic Potentiometer mode set	1 0 0 0 0 0 0 1	0	1	0	Sets a 6-bit data in the electronic potentiometer register to adjust the V1 output voltage. (2-byte command)
		Electronic potentiometer register set	* * Electronic potentiometer value	0 1		0	
19	Static indicator	OFF	1 0 1 0 1 1 0 0	0	1	0	OFF when DB0 = 0
		ON	1 0 1 0 1 1 0 1	0	1	0	ON when DB0 = 1
	Static indicator register set		* * * * * * State	0	1	0	Sets the blinking state. (2-byte command)
20 [1)]	LCD drive method set		1 1 0 1 0 * * *	0	1	0	Frame reversal when DB3 = 0.
			1 1 0 1 1 * * *	0	1	0	Line reversal when DB3 = 1
	Line reversal number set		* * * Number of lines	0 1		0	Sets the number (2-byte command) of line reversal.
21	Power save						Compound command of Display OFF and Display all-on.
22	NOP		1 1 1 0 0 0 1 1	0	1	0	The “No Operation” command.
23	Test		1 1 1 1 * * * *	0	1	0	The command for factory testing of the IC chip.

*: Invalid data (input: Don’t care, output: Unknown)

Note 1: When the line reversal drive is set, the ML9059E is not used in a multiple chip configuration.

DESCRIPTIONS OF OPERATION

Display ON/OFF (Write)

This is the command for controlling the turning on or off the LCD panel. The LCD display is turned on when a "1" is written in bit DB0 and is turned off when a "0" is written in this bit.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Display ON	0	1	0	1			0	1	1	1	1
Display OFF	0	1	0	1			0	1	1	1	0

Display Start Line Set (Write)

This command specifies the display starting line address in the display data RAM.
Normally, the topmost line in the display is specified using the display start line set command.
It is possible to scroll the display screen by dynamically changing the address using the display start line set command.

Line address	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0			0	0	0	0	0
1	0	0	1	0			0	0	0	0	1
2	0	0	1	0			0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
62	0	0	1	1	1	1	1	1	0
63	0	0	1	1	1	1	1	1	1

Page Address Set (Write)

This command specifies the page address which corresponds to the lower address when accessing the display data RAM from the MPU side.
It is possible to access any required bit in the display data RAM by specifying the page address and the column address.

Page address	A0	DB7 D	B6 D	B5 D	B4 D	B3 D	B2 D	B1 D	B0
0	0	1	0	1	1	0	0	0	0
1	0	1	0	1	1	0	0	0	1
2	0	1	0	1	1	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
7	0	1	0	1	1	0	1	1	1
8	0	1	0	1	1	1	0	0	0

Note: Do not specify values that do not exist as an address.

Column Address Set (Write)

This command specifies the column address of the display data RAM. The column address is specified by successively writing the upper 4 bits and the lower 4 bits. Since the column address is automatically incremented (by + 1) every time the display data RAM is accessed, the MPU can read or write the display data continuously. The incrementing of the column address is stopped at the address 83(H).

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Upper bits	0	0	0	0	1	a7	a6	a5	a4
Lower bits	0	0	0	0	0	a3	a2	a1	a0

Column address	a7	a6	a5	a4	a3	a2	a1	a0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
130	1	0	0	0	0	0	1	0
131	1	0	0	0	0	0	1	1

Note: Do not specify values that do not exist as an address.

Status Read (Read)

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BUSY	ADC	ON/OFF	RESET	*	*	*	*

*: Invalid data

BUSY	When BUSY is '1', it indicates that the internal operations are being made or the LSI is being reset. Although no command is accepted until BUSY becomes '0', there is no need to check this bit if the cycle time can be satisfied.
ADC	This bit indicates the relationship between the column address and the segment driver. 0: Reverse (SEG131 → SEG0); column address 0(H) → 83(H) 1: Forward (SEG0 → SEG131); column address 0(H) → 83(H) (Opposite to the polarity of the ADC command.)
ON/OFF	This bit indicates the ON/OFF state of the display. (Opposite to the polarity of the display ON/OFF command.) 0: Display ON 1: Display OFF
RESET	This bit indicates that the LSI is being reset due to the $\overline{RES}$ signal or the reset command. 0: Operating state 1: Being reset

Display Data Write (Write)

This command writes an 8-bit data at the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after writing the data, the MPU can write successive display data to the display data RAM.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Write data							

Display Data Read (Read)

This command read the 8-bit data from the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after reading the data, the MPU can read successive display data from the display data RAM. Further, one dummy read operation is necessary immediately after setting the column data. The display data cannot be read out when the serial interface is being used.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Read data							

ADC Select (Segment driver direction select) (Write)

Using this command it is possible to reverse the relationship of correspondence between the column address of the display data RAM and the segment driver output. It is possible to reverse the sequence of the segment driver output pin by the command.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Forward	0	1	0	1	0	0	0	0	0
Reverse	0	1	0	1	0	0	0	0	1

Forward/Reverse Display Mode (Write)

It is possible to toggle the display on and off condition without changing the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	RAM Data
Forward	0	1	0	1	0	0	1	1	0	Display on when “H”
Reverse	0	1	0	1	0	0	1	1	1	Display on when “L”

LCD Display All-on ON/OFF (Write)

Using this command, it is possible to forcibly turn ON all the dots in the display irrespective of the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.
This command is given priority over the Forward/reverse display mode command.

	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
All-on display OFF (Normal display)	0	1	0	1	0	0	1	0	0
All-on display ON	0	1	0	1	0	0	1	0	1

The power save mode will be entered into when the Display all-on ON command is executed in the display OFF condition.

LCD Bias Set (Write)

This command is used for selecting the bias ratio of the voltage necessary for driving the LCD device or panel.

LCD bias	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1/8 bias	0	1	0	1	0	0	0	1	0
1/6 bias	0	1	0	1	0	0	0	1	1

Read Modify Write (Write)

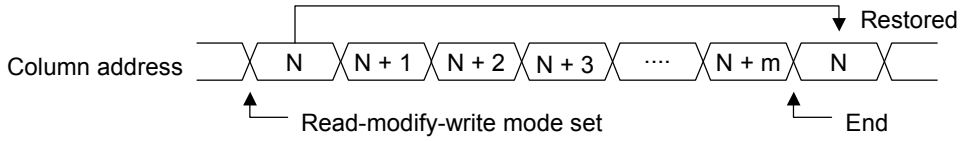
This command is used in combination with the End command. When this command is issued once, the column address is not changed when the Display data read command is issued, but is incremented (by +1) only when the Display data write command is issued. This condition is maintained until the End command is issued. When the End command is issued, the column address is restored to the address that was effective at the time the Read-modify-write command was issued last. Using this function, it is possible to reduce the overhead on the MPU when repeatedly changing the data in special display area such as a blinking cursor.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	0	0	0	0

End (Write)

This command releases the read-modify-write mode and restores the column address to the value at the beginning of the mode.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	1	1	1	0



Reset (Write)

This command initializes the display start line number, column address, page address, common output state, voltage V1 adjustment internal resistor ratio, electronic potentiometer function, and the static indicator function, and also releases the read-modify-write mode or the test mode. This command does not affect the contents of the display data RAM.
The reset operation is made after issuing the reset command.
The initialization after switching on the power is carried out by the reset signal input to the $\overline{RES}$ pin.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	0	0	1	0

Common Output State Select (Write)

This command is used for selecting the scanning direction of the common output pins.

Sc	anning direction	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Forward C	OM0 → COM47	0	1	1	0	0	0	*	*	*
Reverse	COM47 → COM0	0	1	1	0	0	1	*	*	*

*: Invalid data

Power Control Set (Write)

This command set the functions of the power supply circuits.

A0		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Voltage multiplier circuit: OFF	0	0	0	1	0	1	0		
Voltage multiplier circuit: ON	0	0	0	1	0	1	1		
Voltage adjustment circuit: OFF	0	0	0	1	0	1		0	
Voltage adjustment circuit: ON	0	0	0	1	0	1		1	
Voltage follower circuits: OFF	0	0	0	1	0	1			0
Voltage follower circuits: ON	0	0	0	1	0	1			1

Voltage V1 Adjustment Internal Resistor Ratio Set

This command sets the ratios of the internal resistors for adjusting the voltage V1.

Resistor ratio	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3.0	0 0		0 1		0 0		0 0		0
3.5	0 0		0 1		0 0		0 0		1
4.0	0 0		0 1		0 0		0 1		0
4.5	0 0		0 1		0 0		0 1		1
5.0	0 0		0 1		0 0		1 0		0
5.5	0 0		0 1		0 0		1 0		1
6.0	0 0		0 1		0 0		1 1		0
Input inhibiting code	0 0		0 1		0 0		1 1		1

Note: Because this LSI has temperature gradient, V1 rises at lower temperatures. When using V1 gain of 6 times, adjust the built-in electronic potentiometer so that V1 does not exceed 18 V.

Electronic Potentiometer (2-byte command)

This command is used for controlling the LCD drive voltage V1 output by the voltage adjustment circuit of the internal LCD power supply and for adjusting the intensity of the LCD display.
This is a two-byte command consisting of the Electronic potentiometer mode set command and the Electronic potentiometer register set command, both of which should always be issued successively as a pair.

• Electronic potentiometer mode set (Write)
When this command is issued, the electronic potentiometer register set command becomes effective.
Once the electronic potentiometer mode is set, it is not possible to issue any command other than the Electronic potentiometer register set command. This condition is released after data has been set in the register using the Electronic potentiometer register set command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	1

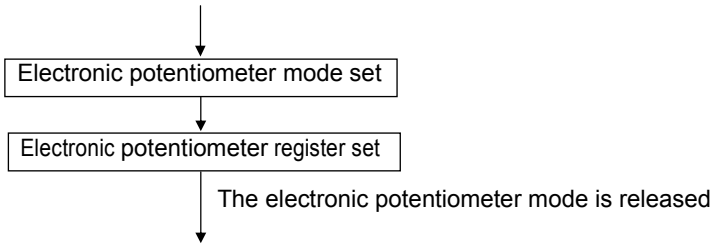
• Electronic potentiometer register set (Write)
By setting a 6-bit data in the electronic potentiometer register using this command, it is possible to set the LCD drive voltage V1 to one of the 64 voltage levels.
The electronic potentiometer mode is released after some data has been set in the electronic potentiometer register using this command.

α	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
63	0	*	*	0	0	0	0	0	1
62	0	*	*	0	0	0	0	0	1
61	0	*	*	0	0	0	0	1	0
60	0	*	*	0	0	0	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	⋮	⋮	⋮	1	1	1	1	1	0
0	0	*	*	1	1	1	1	1	1

*: Invalid data

Set the data (*, *, 1, 0, 0, 0, 0, 0) when not using the electronic potentiometer function.

Sequence of setting the electronic potentiometer register:



Static Indicator (2-byte command)

This command is used for controlling the static drive type indicator display.
Static indicator display is controlled only by this command and is independent of all other display control commands.

Since the Static indicator ON command is a two-byte command used in combination with the static indictor register set command, these two commands should always be used together.
(The Static indicator OFF command is a single byte command.)

• Static indicator ON/OFF (Write)
When the Static indicator ON command is issued, the Static indicator register set command becomes effective. Once the Static indicator ON command is issued, it is not possible to issue any command other than the Static indicator register set command. This condition is released only after some data is written into the register using the static indicator register set command.

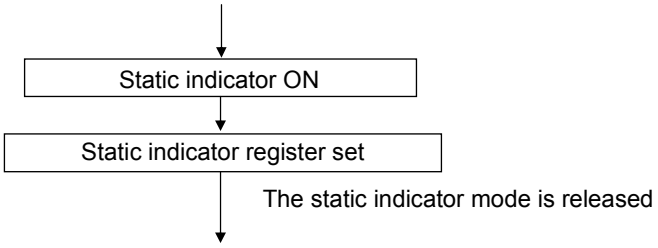
Static indicator	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
OFF	0	1	0	1	0	1	1	0	0
ON	0	1	0	1	0	1	1	0	1

• Static indicator register set (Write)
This command is used to set data in the 2-bit static indicator register thereby setting the blinking state of the static indicator.

Indicator	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
OFF	0	*	*	*	*	*	*	0	0
ON(Blinking at about 1sec intervals)	0	*	*	*	*	*	*	0	1
ON(Blinking at about 0.5sec intervals)	0	*	*	*	*	*	*	1	0
ON(Continuously ON)	0	*	*	*	*	*	*	1	1

*: Invalid data

Sequence of setting the static indicator register:



LCD Drive Method Set (Write)
This command sets the LCD drive method.

• Line reversal drive (2-byte command)/frame reversal drive select
Line or frame reversal drive can be selected as the LCD drive method.
When selecting line reversal drive, which is 2-byte command used with line reversal number set command, be sure to use both commands successively.
Once line reversal drive is set, commands other than line reversal number set command cannot be used. This state is released after data is set to the register by line reversal number set command.
The frame reversal set command is a single byte command.

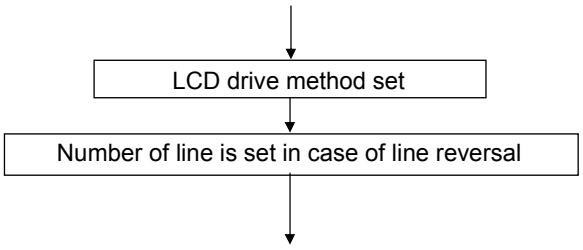
LCD drive method	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Frame reversal	0	1 1 0	1 0				*	*	*
Line reversal	0	1 1 0	1 1				*	*	*

*: Inv alid data

• Line reversal number set (Write)
The number of lines is set when the line reversal is set using the LCD drive method set command.

Number of line reversal	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0 *		*	* 0		0	0	0	0
2	0 *		*	* 0		0	0	0	1
3	0 *		*	* 0		0	0	1	0
4	0 *		*	* 0		0	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
31	⋮	⋮	⋮	⋮	1 1		1 1		0
32	0 *		*	* 1		1	1	1	1

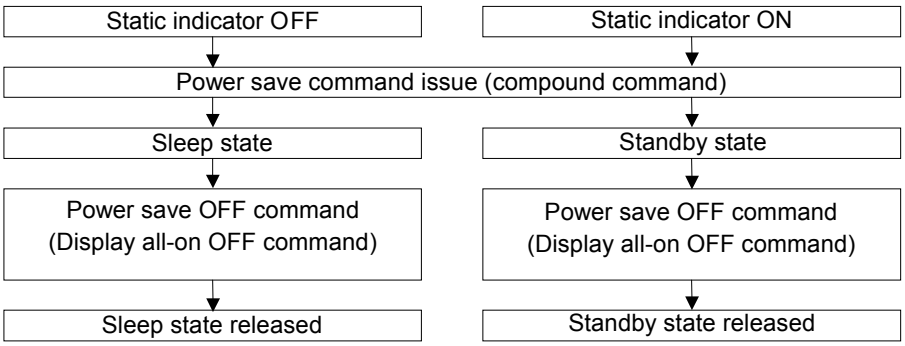
*: Inv alid data



Note 1: Because the number of line reversal depends on panel size and panel load capacitance, set the optimum number of lines at the time of ES evaluation.
Note 2: When line reversal drive is used, a multiple chip configuration cannot be achieved.

Power Save (Compound command)

The LSI goes into the power save state when the Display all-on ON command is issued when the LSI is in the display OFF state, and it is possible to greatly reduce the current consumption in this state. The power save state is of two types, namely, the sleep state and the standby state, and the LSI goes into the standby state when the static indicator has been made ON.
The display data and the operating mode just before entering the power save mode are retained in both the sleep state and the standby state, and also the MPU can access the display data RAM and other registers in these states. The power save mode is released by issuing the Display all-on OFF command. (See the following figure.)



• Sleep state

In this state, all the operations of the LCD display system are stopped and it is possible to reduce the current consumption to a level near the idle state current consumption unless there are acces ses from the MPU. The internal conditions in the sleep state are as follows:

(1) The oscillator circuit and the LCD power supply are stopped.

(2) All the LCD drive circuits are stopped and the segment and common driver outputs will be at the V_{SS} level.

• Standby state

All operations of the dynamic LCD display section are stopped, only the static display circuits for the indicators operate and hence the current consumption will be the minimum necessary for static drive. The internal conditions in the standby state are as follows:

(1) The power supply circuit for LCD drive is stopped. The oscillator circuit will be operating.

(2) The LCD drive circuits for dynamic display are stopped and the segment and common driver outputs will be at the V_{SS} level. The static display section will be operating.

Note: When using an external power supply, stop external power supply at power save start-up.
For example, when providing each level of LCD drive voltage with external voltage divider, add a circuit for cutting off current flowing through the resistors of the voltage divider when initiating power save.
The ML9059E has LCD display blanking control pin, $\overline{DOF}$, which goes "L" at power save start-up. The external power supply can be stopped using $\overline{DOF}$ output.

NOP (Write)

This is a No Operation command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	0	0	0	1	1

Test (Write)

This is a command for testing the IC chip. Do not use this command. When the test command is issued by mistake, this state can be released by issuing a NOP command.

A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	1	*	*	*	*

*: Invalid data

Initialized Condition Using the $\overline{\text{RES}}$ Pin

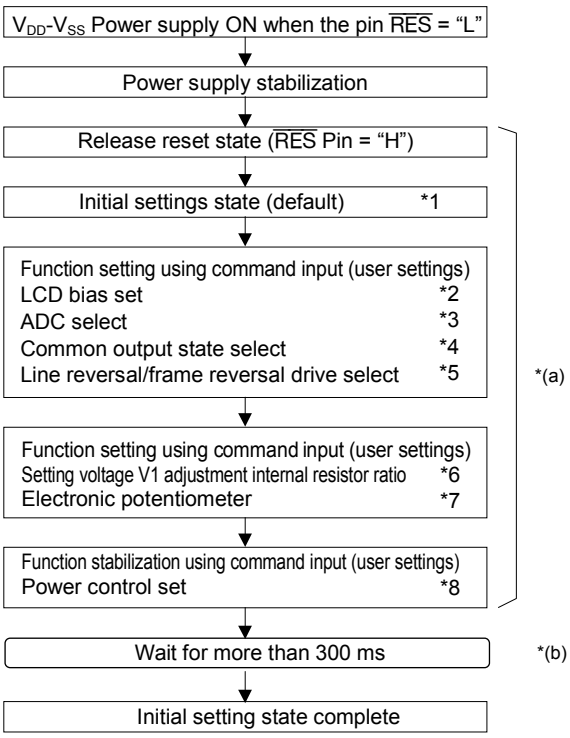
This LSI goes into the initialized condition when the $\overline{\text{RES}}$ input goes to the "L" level. The initialized condition consists of the following conditions.

(1) Disp lay OFF
(2) Forward display mode
(3) ADC select: Incremented (ADC command DB0 = "L")
(4) Power control register: (DB2, DB1, DB0) = (0, 0, 0)
(5) The registers and data in the serial interface are cleared.
(6) LCD Power supply bias ratio: 1/8 bias
(7) All display dots OFF
(8) R ead-modify-write: OFF
(9) Static indicator: OFF
Static indicator register: (DB1, DB0) = (0, 0)
(10) Line 1 is set as the display start line.
(11) The column address is set to address 0.
(12) The page address is set to 0.
(13) Common output state: Forward
(14) Voltage V1 adjustment internal resistor ratio register: (DB2, DB1, DB0) = (1, 0, 0)
(15) The electronic potentiometer register set mode is released.
Electronic potentiometer register: (DB5, DB4, DB3, DB2, DB1, DB0) = (1, 0, 0 ,0, 0, 0)
(16) The LCD drive method is set to the frame reversal drive.
Line reversal number register: (DB4, DB3, DB2, DB1, DB0) = (1, 0, 0, 0, 0)

On the other hand, when the reset command is used, only the conditions (8) to (15) above are set.
As is shown in the "MPU Interface (example for reference)", the $\overline{\text{RES}}$ pin is connected to the Reset pin of the MPU and the initialization of this LSI is made simultaneously with the resetting of the MPU. This LSI always has to be reset using the $\overline{\text{RES}}$ pin at the time the power is switched ON. Also, excessive current can flow through this LSI when the control signal from the MPU is in the high impedance state. It is necessary to take measures to ensure that the input pins of this LSI do not go into the high impedance state after the power has been switched ON. When the built-in LCD drive power supply circuit of the ML9059E is not used, it is necessary that $\overline{\text{RES}}$ = "L" when the external LCD drive power supply goes ON. During the period when $\overline{\text{RES}}$ = "L", although the oscillator circuit is operating, the display timing generator would have stopped and the pins CL, FR, FRS, and $\overline{\text{DOF}}$ would have been tied to the "H" level. There is no effect on the pins DB0 to DB7.

EXAMPLES OF SETTINGS FOR THE INSTRUCTIONS

When Using the Internal Power Supply Immediately After Power-on

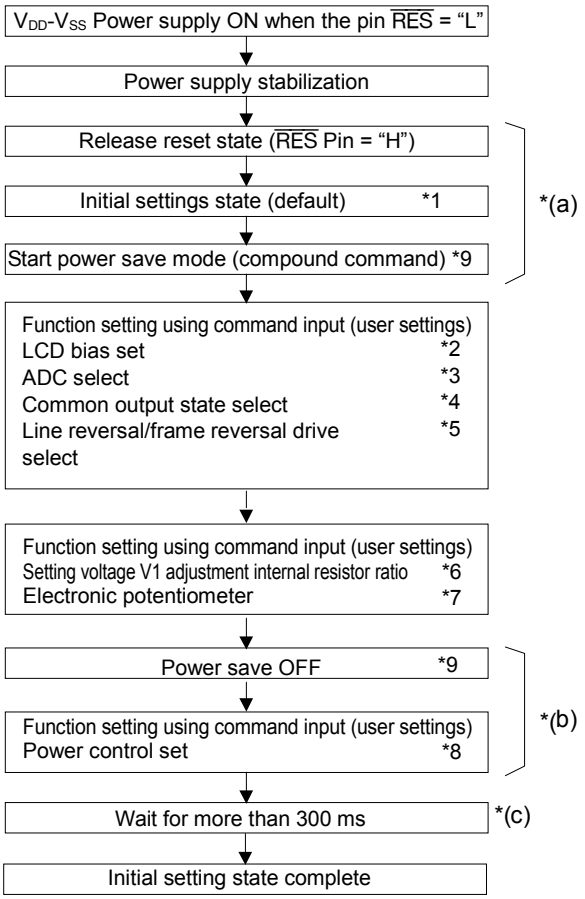


*(a): Carry out power control set within 5ms after releasing the reset state.
The 5ms duration changes depending on the panel characteristics and the value of the smoothing capacitor. We recommend verification of operation using an actual unit.

*(b): When trace resistance in COG mounting does not exist, wait for over 300 ms.
Since this value varies with trace resistance, V1, smoothing capacitors, or voltage multiplier capacitors in COG mounting, confirm operation on an actual circuit board when using this LSI.

Notes: Sections to be referred to
- *1: Functional description "Reset circuit"
- *2: Description of operation "LCD bias set"
- *3: Description of operation "ADC select"
- *4: Description of operation "Common output state select"
- *5: Description of operation "Line reversal/frame reversal drive select"
- *6: Functional description "Power supply circuit", Operation description "Voltage V1 adjustment internal resistor ratio set"
- *7: Functional description "Power supply circuit", Description of operation "Electronic potentiometer"
- *8: Functional description "Power supply circuit", Description of operation "Power control set"

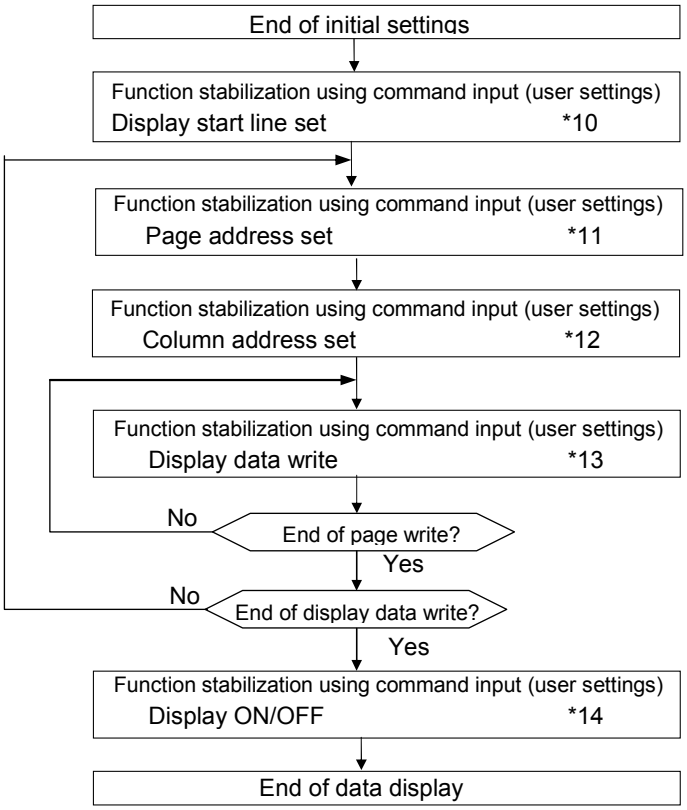
When Not Using the Internal Power Supply Immediately After Power-on



*(a): Enter the power save state within 5ms after releasing the reset state.
*(b): Carry out power control set within 5ms after releasing the power save state.
The 5ms duration in *(a) and *(b) changes depending on the panel characteristics and the value of the smoothing capacitor. We recommend verification of operation using an actual unit.
*(c): When trace resistance in COG mounting does not exist, wait for over 300 ms.
Since this value varies with trace resistance, V1, smoothing capacitors, or voltage multiplier capacitors in COG mounting, confirm operation on an actual circuit board when using this LSI.

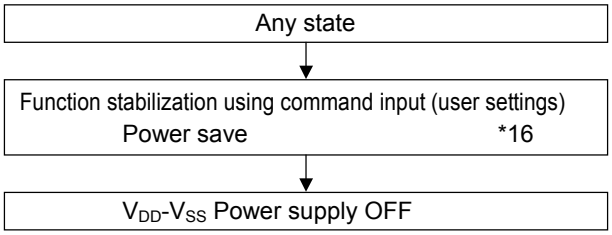
Notes: Sections to be referred to
*1: Functional description "Reset circuit"
*2: Description of operation "LCD bias set"
*3: Description of operation "ADC select"
*4: Description of operation "Common output state select"
*5: Description of operation "Line reversal/frame reversal drive select"
*6: Functional description "Power supply circuit", Description of operation "Voltage V1 adjustment internal resistor ratio set"
*7: Functional description "Power supply circuit", Description of operation "Electronic potentiometer"
*8: Functional description "Power supply circuit", Description of operation "Power control set"
*9: The power save state can be either the sleep state or the standby state.
Description of operation "Power save (compound command)"

Data Display



Notes: Sections to be referred to
*10: Description of operation “Display start line set”
*11: Description of operation “Page address set”
*12: Description of operation “Column address set”
*13: Description of operation “Display data write”
*14: Description of operation “Display ON/OFF”

Power Supply OFF (*15)



Notes: Sections to be referred to

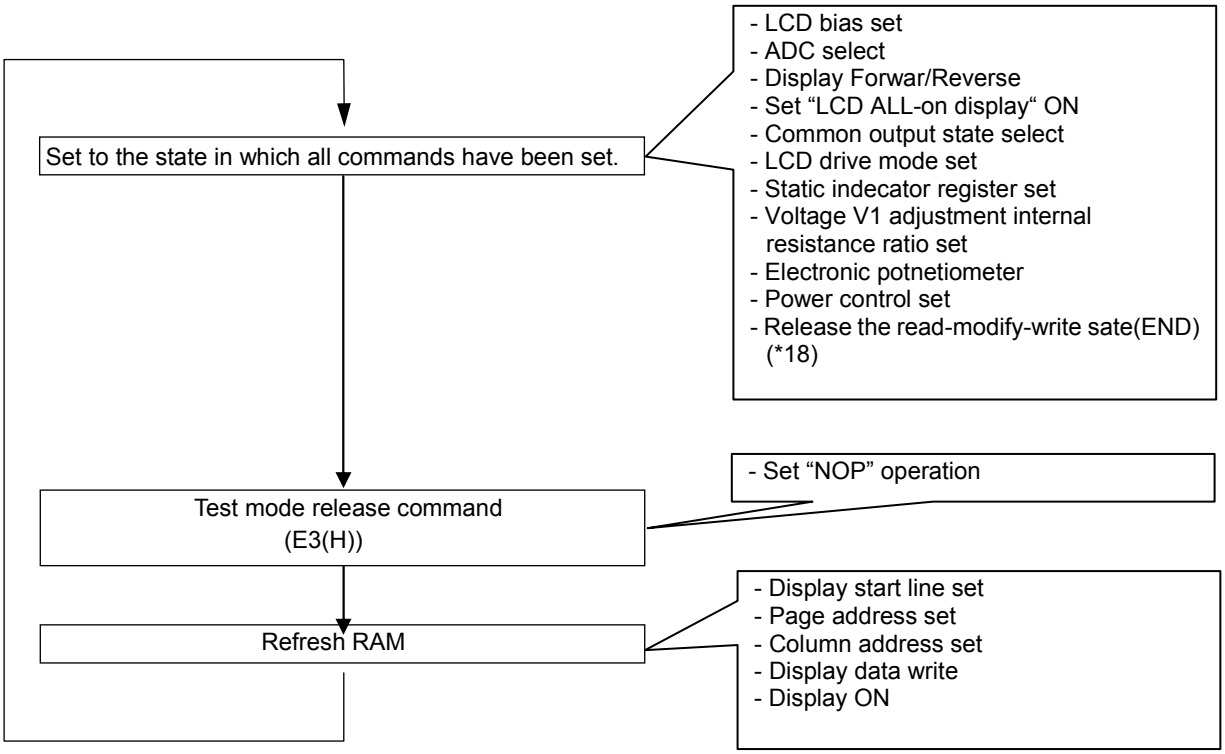
*15: The power supply of this LSI is switched OFF after switching OFF the internal power supply. Function description “Power supply circuit”
If the power supply of this LSI is switched OFF when the internal power supply is still ON, since the state of supplying power to the built-in LCD drive circuits continues for a short duration, it may affect the display quality of the LCD panel. Always follow the power supply switching OFF s equence.

*16: Description of operation “Power save”

*17: After reset is input the power supply may off without obeying above sequence.

Refresh

Although the ML9059E holds operation state by commands, excessive external noise might change the internal state.
On a chip-mounting and system level, it is necessary to take countermeasures against preventing noise from occurring. It is recommended to use the refresh sequence periodically to control sudden noise.

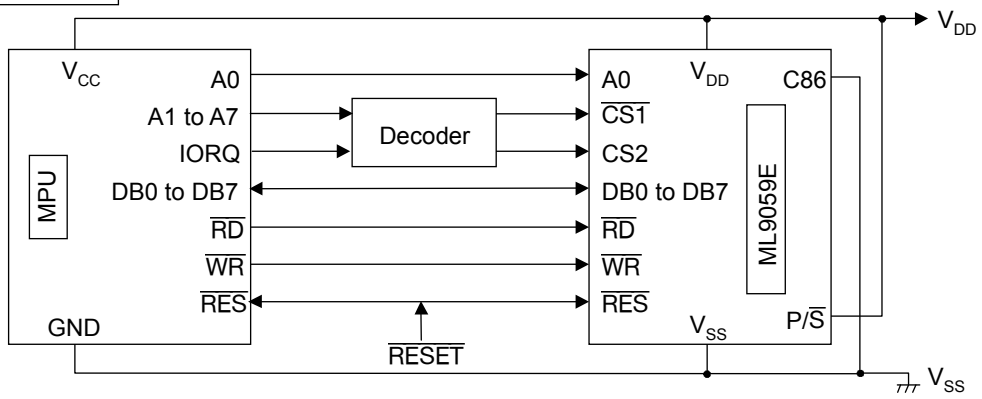


*18: Regardless of presence of setting of “Read-modify-write”commanfd, please carry out “END” command.

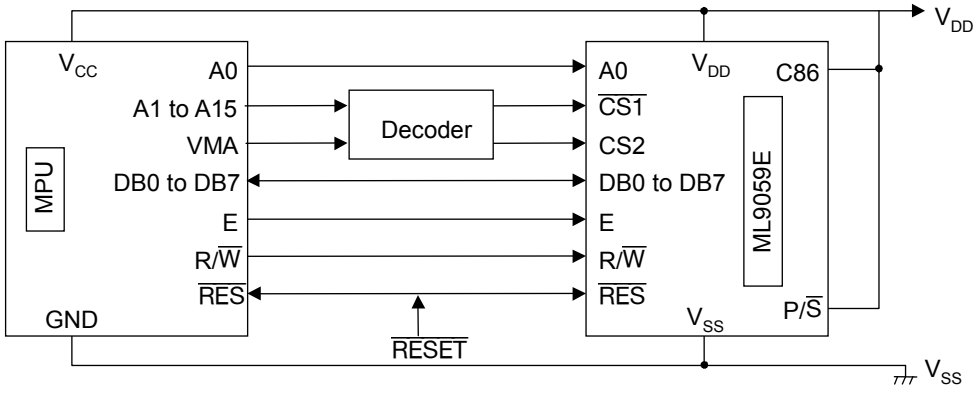
MPU INTERFACE

The ML9059E series ICs can be connected directly to the 80-series and 68-series MPUs.
Further, by using the serial interface, it is possible to operate the LSI with a minimum number of signal lines.
In addition, it is possible to expand the display area by using the ML9059E series LSIs in a multiple chip configuration. In this case, it is possible to select the individual LSI to be accessed using the chip select signals.

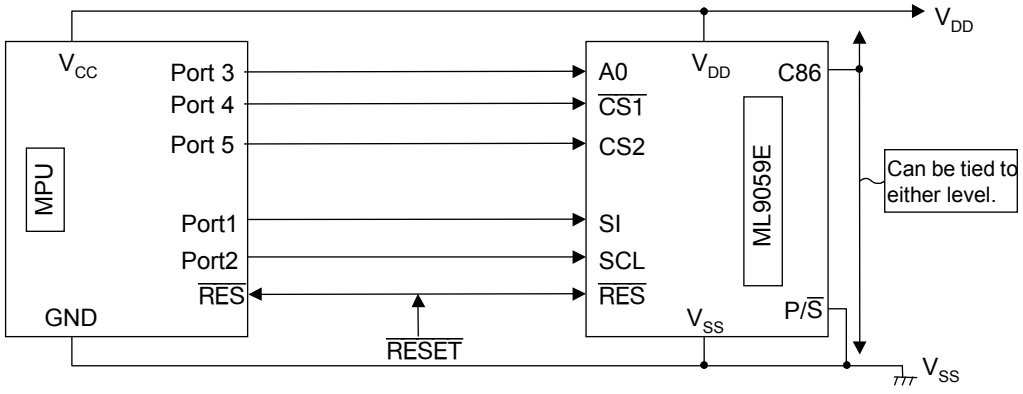
• 80-Series MPU



• 68-Series MPU



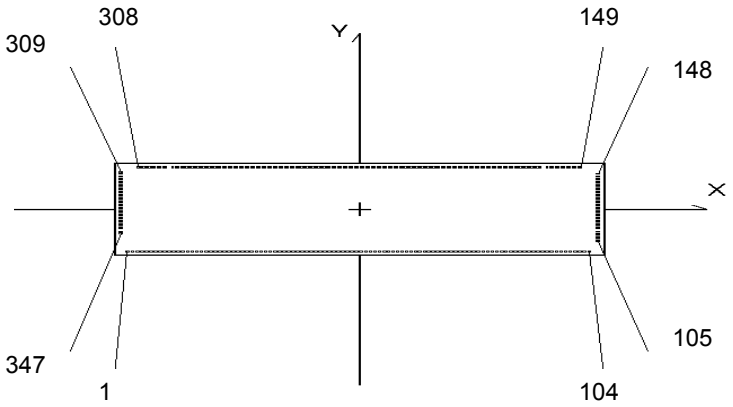
• Serial interface



PAD CONFIGURATION

Pad Layout

Chip Size : 9.164 × 2.982 mm



Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	D UMMY	-4462.5	-1376.0	21	$\overline{CS1}$	-2762.5	-1376.0
2	D UMMY	-4377.5	-1376.0	22	C S2	-2677.5	-1376.0
3	D UMMY	-4292.5	-1376.0	23	V $_{DD}$	-2592.5	-1376.0
4	D UMMY-B	-4207.5	-1376.0	24	$\overline{RES}$	-2507.5	-1376.0
5	D UMMY-B	-4122.5	-1376.0	25	A0	-2422.5	-1376.0
6	D UMMY-B	-4037.5	-1376.0	26	V $_{SS}$	-2337.5	-1376.0
7	D UMMY-B	-3952.5	-1376.0	27	$\overline{WR}$	-2252.5	-1376.0
8	D UMMY-B	-3867.5	-1376.0	28	$\overline{RD}$	-2167.5	-1376.0
9	V $_{SS}$	-3782.5	-1376.0	29	V $_{DD}$	-2082.5	-1376.0
10	D UMMY-B	-3697.5	-1376.0	30	D B0	-1997.5	-1376.0
11	D UMMY-B	-3612.5	-1376.0	31	D B1	-1912.5	-1376.0
12	D UMMY-B	-3527.5	-1376.0	32	D B2	-1827.5	-1376.0
13	D UMMY-B	-3442.5	-1376.0	33	D B3	-1742.5	-1376.0
14	D UMMY-B	-3357.5	-1376.0	34	D B4	-1657.5	-1376.0
15	T EST1	-3272.5	-1376.0	35	D B5	-1572.5	-1376.0
16	FR S	-3187.5	-1376.0	36	D B6	-1487.5	-1376.0
17	FR	-3102.5	-1376.0	37	DB7	-1402.5	-1376.0
18	CL	-3017.5	-1376.0	38	DUMMY-B	-1317.5	-1376.0
19	$\overline{DOF}$	-2932.5	-1376.0	39	V_{DD}	-1232.5	-1376.0
20	V_{SS}	-2847.5	-1376.0	40	V_{DD}	-1147.5	-1376.0

Note: Leave DUMMY and DUMMY-B pads open.
Do not run tr aces aro und. Run trac es thr ough D UMMY and D UMMY-B pads individually, not in common.

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
41	V_{DD}	-1062.5	-1376.0	81	V1	2337.5	-1376.0
42	V_{DD}	-977.5	-1376.0	82	V1	2422.5	-1376.0
43	V_{DD}	-892.5	-1376.0	83	V2	2507.5	-1376.0
44	V_{DD}	-807.5	-1376.0	84	V2	2592.5	-1376.0
45	V_{IN}	-722.5	-1376.0	85	V3	2677.5	-1376.0
46	V_{IN}	-637.5	-1376.0	86	V3	2762.5	-1376.0
47	V_{IN}	-552.5	-1376.0	87	V4	2847.5	-1376.0
48	V_{IN}	-467.5	-1376.0	88	V4	2932.5	-1376.0
49	V_{IN}	-382.5	-1376.0	89	V5	3017.5	-1376.0
50	V_{SS}	-297.5	-1376.0	90	V5	3102.5	-1376.0
51	V_{SS}	-212.5	-1376.0	91	VR	3187.5	-1376.0
52	V_{SS}	-127.5	-1376.0	92	VR	3272.5	-1376.0
53	V_{SS}	-42.5	-1376.0	93	V_{DD}	3357.5	-1376.0
54	V_{SS}	42.5	-1376.0	94	M/$\overline{S}$	3442.5	-1376.0
55	V_{SS}	127.5	-1376.0	95	CLS	3527.5	-1376.0
56	V_{SS}	212.5	-1376.0	96	V_{SS}	3612.5	-1376.0
57	V_{OUT}	297.5	-1376.0	97	C86	3697.5	-1376.0
58	V_{OUT}	382.5	-1376.0	98	P/$\overline{S}$	3782.5	-1376.0
59	VC6+	467.5	-1376.0	99	V_{DD}	3867.5	-1376.0
60	VC6+	552.5	-1376.0	100	DUMMY	3952.5	-1376.0
61	VC6+	637.5	-1376.0	101	V_{SS}	4037.5	-1376.0
62	VC4+	722.5	-1376.0	102	IRS	4122.5	-1376.0
63	VC4+	807.5	-1376.0	103	V_{DD}	4207.5	-1376.0
64	VC4+	892.5	-1376.0	104	DUMMY	4292.5	-1376.0
65	VS2-	977.5	-1376.0	105	DUMMY	4443.0	-1049.9
66	VS2-	1062.5	-1376.0	106	DUMMY	4443.0	-997.9
67	VS2-	1147.5	-1376.0	107	DUMMY	4443.0	-945.9
68	VS1-	1232.5	-1376.0	108	DUMMY	4443.0	-893.9
69	VS1-	1317.5	-1376.0	109	DUMMY	4443.0	-841.9
70	VS1-	1402.5	-1376.0	110	DUMMY	4443.0	-789.9
71	VC5+	1487.5	-1376.0	111	DUMMY	4443.0	-737.9
72	VC5+	1572.5	-1376.0	112	DUMMY	4443.0	-685.9
73	VC5+	1657.5	-1376.0	113	DUMMY	4443.0	-633.9
74	VC3+	1742.5	-1376.0	114	DUMMY	4443.0	-581.9
75	VC3+	1827.5	-1376.0	115	DUMMY	4443.0	-529.9
76	VC3+	1912.5	-1376.0	116	DUMMY	4443.0	-477.9
77	V_{SS}	1997.5	-1376.0	117	DUMMY	4443.0	-425.9
78	V_{RS}	2082.5	-1376.0	118	DUMMY	4443.0	-373.9
79	V_{RS}	2167.5	-1376.0	119	DUMMY	4443.0	-321.9
80	V_{DD}	2252.5	-1376.0	120	DUMMY	4443.0	-269.9

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
121	COM23	4443.0	-217.9	161	DUMMY	3504.7	1352.5
122	COM22	4443.0	-165.9	162	DUMMY	3452.7	1352.5
123	COM21	4443.0	-113.9	163	DUMMY	3400.7	1352.5
124	COM20	4443.0	-61.9	164	SEG0	3348.7	1352.5
125	COM19	4443.0	-9.9	165	SEG1	3296.7	1352.5
126	COM18	4443.0	42.1	166	SEG2	3244.7	1352.5
127	COM17	4443.0	94.1	167	SEG3	3192.7	1352.5
128	COM16	4443.0	146.1	168	SEG4	3140.7	1352.5
129	COM15	4443.0	198.1	169	SEG5	3088.7	1352.5
130	COM14	4443.0	250.1	170	SEG6	3036.7	1352.5
131	COM13	4443.0	302.1	171	SEG7	2984.7	1352.5
132	COM12	4443.0	354.1	172	SEG8	2932.7	1352.5
133	COM11	4443.0	406.1	173	SEG9	2880.7	1352.5
134	COM10	4443.0	458.1	174	SEG10	2828.7	1352.5
135	COM9	4443.0	510.1	175	SEG11	2776.7	1352.5
136	COM8	4443.0	562.1	176	SEG12	2724.7	1352.5
137	COM7	4443.0	614.1	177	SEG13	2672.7	1352.5
138	COM6	4443.0	666.1	178	SEG14	2620.7	1352.5
139	COM5	4443.0	718.1	179	SEG15	2568.7	1352.5
140	COM4	4443.0	770.1	180	SEG16	2516.7	1352.5
141	COM3	4443.0	822.1	181	SEG17	2464.7	1352.5
142	COM2	4443.0	874.1	182	SEG18	2412.7	1352.5
143	COM1	4443.0	926.1	183	SEG19	2360.7	1352.5
144	COM0	4443.0	978.1	184	SEG20	2308.7	1352.5
145	COMS1	4443.0	1030.1	185	SEG21	2256.7	1352.5
146	DUMMY	4443.0	1082.1	186	SEG22	2204.7	1352.5
147	DUMMY	4443.0	1134.1	187	SEG23	2152.7	1352.5
148	DUMMY	4443.0	1186.1	188	SEG24	2100.7	1352.5
149	DUMMY	4128.7	1352.5	189	SEG25	2048.7	1352.5
150	DUMMY	4076.7	1352.5	190	SEG26	1996.7	1352.5
151	DUMMY	4024.7	1352.5	191	SEG27	1944.7	1352.5
152	DUMMY	3972.7	1352.5	192	SEG28	1892.7	1352.5
153	DUMMY	3920.7	1352.5	193	SEG29	1840.7	1352.5
154	DUMMY	3868.7	1352.5	194	SEG30	1788.7	1352.5
155	DUMMY	3816.7	1352.5	195	SEG31	1736.7	1352.5
156	DUMMY	3764.7	1352.5	196	SEG32	1684.7	1352.5
157	DUMMY	3712.7	1352.5	197	SEG33	1632.7	1352.5
158	DUMMY	3660.7	1352.5	198	SEG34	1580.7	1352.5
159	DUMMY	3608.7	1352.5	199	SEG35	1528.7	1352.5
160	DUMMY	3556.7	1352.5	200	SEG36	1476.7	1352.5

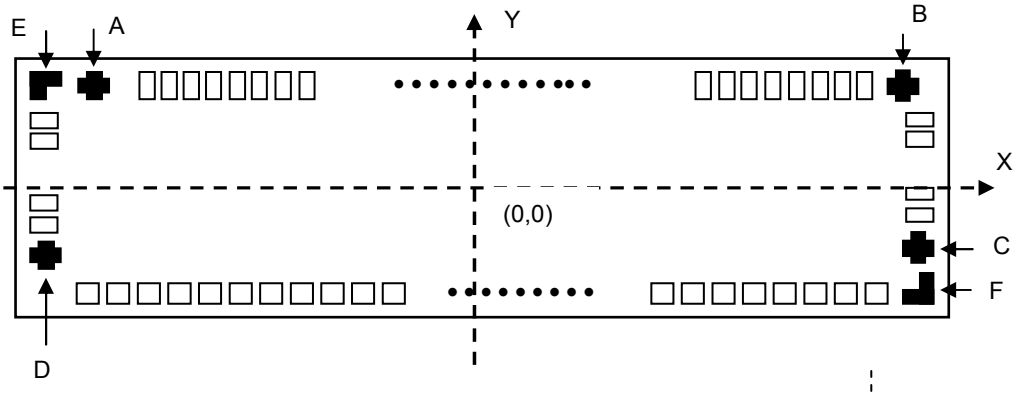
Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
201	SEG37	1424.7	1352.5	241	SEG77	-655.3	1352.5
202	SEG38	1372.7	1352.5	242	SEG78	-707.3	1352.5
203	SEG39	1320.7	1352.5	243	SEG79	-759.3	1352.5
204	SEG40	1268.7	1352.5	244	SEG80	-811.3	1352.5
205	SEG41	1216.7	1352.5	245	SEG81	-863.3	1352.5
206	SEG42	1164.7	1352.5	246	SEG82	-915.3	1352.5
207	SEG43	1112.7	1352.5	247	SEG83	-967.3	1352.5
208	SEG44	1060.7	1352.5	248	SEG84	-1019.3	1352.5
209	SEG45	1008.7	1352.5	249	SEG85	-1071.3	1352.5
210	SEG46	956.7	1352.5	250	SEG86	-1123.3	1352.5
211	SEG47	904.7	1352.5	251	SEG87	-1175.3	1352.5
212	SEG48	852.7	1352.5	252	SEG88	-1227.3	1352.5
213	SEG49	800.7	1352.5	253	SEG89	-1279.3	1352.5
214	SEG50	748.7	1352.5	254	SEG90	-1331.3	1352.5
215	SEG51	696.7	1352.5	255	SEG91	-1383.3	1352.5
216	SEG52	644.7	1352.5	256	SEG92	-1435.3	1352.5
217	SEG53	592.7	1352.5	257	SEG93	-1487.3	1352.5
218	SEG54	540.7	1352.5	258	SEG94	-1539.3	1352.5
219	SEG55	488.7	1352.5	259	SEG95	-1591.3	1352.5
220	SEG56	436.7	1352.5	260	SEG96	-1643.3	1352.5
221	SEG57	384.7	1352.5	261	SEG97	-1695.3	1352.5
222	SEG58	332.7	1352.5	262	SEG98	-1747.3	1352.5
223	SEG59	280.7	1352.5	263	SEG99	-1799.3	1352.5
224	SEG60	228.7	1352.5	264	SEG100	-1851.3	1352.5
225	SEG61	176.7	1352.5	265	SEG101	-1903.3	1352.5
226	SEG62	124.7	1352.5	266	SEG102	-1955.3	1352.5
227	SEG63	72.7	1352.5	267	SEG103	-2007.3	1352.5
228	SEG64	20.7	1352.5	268	SEG104	-2059.3	1352.5
229	SEG65	-31.3	1352.5	269	SEG105	-2111.3	1352.5
230	SEG66	-83.3	1352.5	270	SEG106	-2163.3	1352.5
231	SEG67	-135.3	1352.5	271	SEG107	-2215.3	1352.5
232	SEG68	-187.3	1352.5	272	SEG108	-2267.3	1352.5
233	SEG69	-239.3	1352.5	273	SEG109	-2319.3	1352.5
234	SEG70	-291.3	1352.5	274	SEG110	-2371.3	1352.5
235	SEG71	-343.3	1352.5	275	SEG111	-2423.3	1352.5
236	SEG72	-395.3	1352.5	276	SEG112	-2475.3	1352.5
237	SEG73	-447.3	1352.5	277	SEG113	-2527.3	1352.5
238	SEG74	-499.3	1352.5	278	SEG114	-2579.3	1352.5
239	SEG75	-551.3	1352.5	279	SEG115	-2631.3	1352.5
240	SEG76	-603.3	1352.5	280	SEG116	-2683.3	1352.5

Pad No.	Pad Name	X (μm)	Y (μm)
281	SEG117	-2735.3	1352.5
282	SEG118	-2787.3	1352.5
283	SEG119	-2839.3	1352.5
284	SEG120	-2891.3	1352.5
285	SEG121	-2943.3	1352.5
286	SEG122	-2995.3	1352.5
287	SEG123	-3047.3	1352.5
288	SEG124	-3099.3	1352.5
289	SEG125	-3151.3	1352.5
290	SEG126	-3203.3	1352.5
291	SEG127	-3255.3	1352.5
292	SEG128	-3307.3	1352.5
293	SEG129	-3359.3	1352.5
294	SEG130	-3411.3	1352.5
295	SEG131	-3463.3	1352.5
296	DUMMY	-3515.3	1352.5
297	DUMMY	-3567.3	1352.5
298	DUMMY	-3619.3	1352.5
299	DUMMY	-3671.3	1352.5
300	DUMMY	-3723.3	1352.5
301	DUMMY	-3775.3	1352.5
302	DUMMY	-3827.3	1352.5
303	DUMMY	-3879.3	1352.5
304	DUMMY	-3931.3	1352.5
305	DUMMY	-3983.3	1352.5
306	DUMMY	-4035.3	1352.5
307	DUMMY	-4087.3	1352.5
308	DUMMY	-4139.3	1352.5
309	DUMMY	-4443.0	1186.1
310	DUMMY	-4443.0	1134.1
311	DUMMY	-4443.0	1082.1
312	COM24	-4443.0	1030.1
313	COM25	-4443.0	978.1
314	COM26	-4443.0	926.1

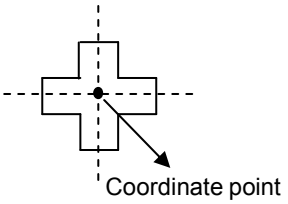
Pad No.	Pad Name	X (μm)	Y (μm)
315	COM27	-4443.0	874.1
316	COM28	-4443.0	822.1
317	COM29	-4443.0	770.1
318	COM30	-4443.0	718.1
319	COM31	-4443.0	666.1
320	COM32	-4443.0	614.1
321	COM33	-4443.0	562.1
322	COM34	-4443.0	510.1
323	COM35	-4443.0	458.1
324	COM36	-4443.0	406.1
325	COM37	-4443.0	354.1
326	COM38	-4443.0	302.1
327	COM39	-4443.0	250.1
328	COM40	-4443.0	198.1
329	COM41	-4443.0	146.1
330	COM42	-4443.0	94.1
331	COM43	-4443.0	42.1
332	COM44	-4443.0	-9.9
333	COM45	-4443.0	-61.9
334	COM46	-4443.0	-113.9
335	COM47	-4443.0	-165.9
336	COMS0	-4443.0	-217.9
337	DUMMY	-4443.0	-269.9
338	DUMMY	-4443.0	-321.9
339	DUMMY	-4443.0	-373.9
340	DUMMY	-4443.0	-425.9
341	DUMMY	-4443.0	-477.9
342	DUMMY	-4443.0	-529.9
343	DUMMY	-4443.0	-581.9
344	DUMMY	-4443.0	-633.9
345	DUMMY	-4443.0	-685.9
346	DUMMY	-4443.0	-737.9
347	DUMMY	-4443.0	-789.9

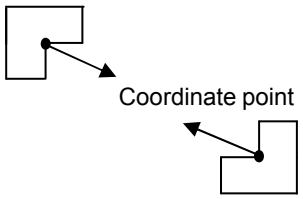
ML9059E ALIGNMENT MARK SPECIFICATION 1

Alignment Mark Coordinates



Alignment mark	X(μm)	Y(μm)
A	–4270.3	1364.5
B	4259.7	1364.5
C	4455	–1180.9
D	–4455	–1180.9
E	–4458.5	1368
F	4458.5	–1368



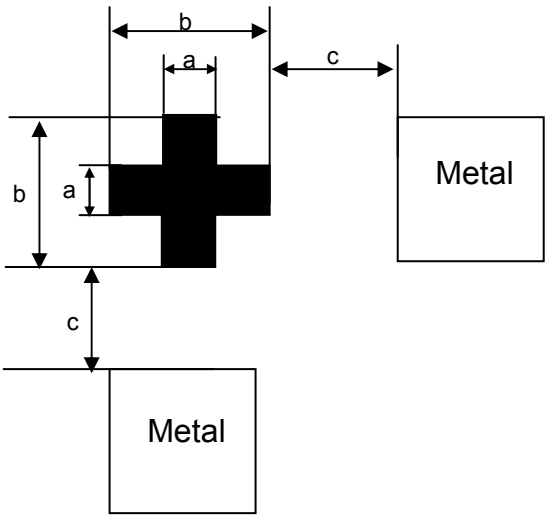


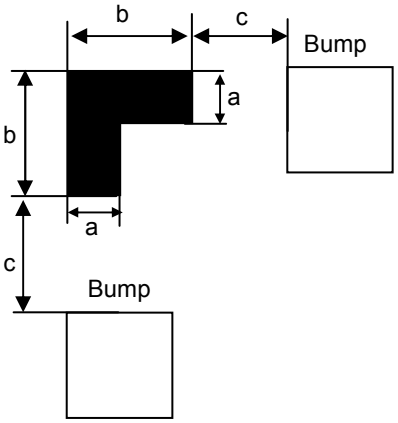
Alignment Mark Construction Layer

A, B, C, D: Metal Layer E,F:Bump Layer

Alignment Mark Specification

Symbol	Parameter	Mark	Size(μm)
a	Alignment mark Width	A, B, C, D	34
		E, F	43
b	Alignment mark Size	A, B, C, D	100
		E, F	98
c	Alignment mark-to-adjacent pad metal Distance (MIN.)	A, B, C	60
		D	106.6
	Alignment mark-to-adjacent pad bump Distance (MIN.)	E	109.4
		F	77





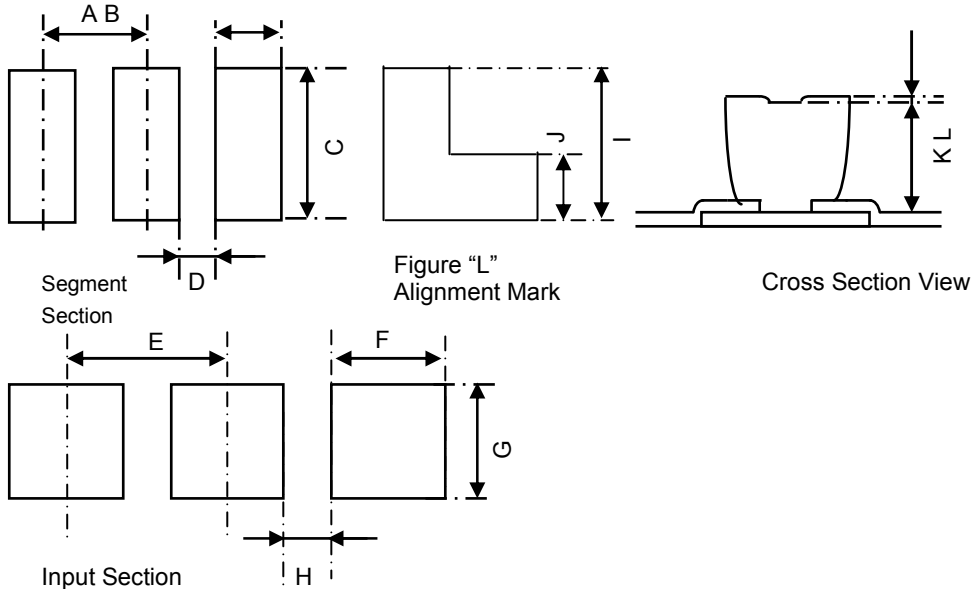
ML9059E GOLD BUMP SPECIFICATION

Gold Bump Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
A	Bump Pitch (Min.Section:Segment Section)	52	—	—	μm
B	Bump Size (Segment Section:Pitch Direction)	29	32	35	μm
C	Bump Size (Segment Section:Depth Direction)	114	117	120	μm
D	Bumo-to-Bump Distance (Segment Section:Pitch Direction)	17 20		23	μm
E	Bump Pitch (Min.Section:Input Section)	85	—	—	μm
F	Bump Size (Input Section:Pitch Direction)	57	60	63	μm
G	Bump Size (Input Section:Depth Direction)	67	70	73	μm
H	Bumo-to-Bump Distance (Input Section:Pitch Direction)	22 25		28	μm
I	Bump Size (Figure “L” alignment mark: Length)	95	98	101	μm
J	Bump Size (Figure “L” alignment mark: width)	40	43	46	μm
—	Pad center-to-Bump center allowable error	—	—	2	μm
K	Bump Height	12	15	18	μm
—	Bumph Height Dispersion Inside Chip (Range)	—	—	3	μm
L	Bump Edge Height	—	—	3	μm
—	Shear Strength (g)	18	—	—	g
—	Bump hardness: High (Hv: 25g load)	50	—	110	Hv
—	Bump hardness: Low (Hv: 25g load)	30	—	70	Hv

- Chip Thickness: 625 ±15 μm
- Chip Size: 9.164mm × 2.982mm

Top View and Cross Section View



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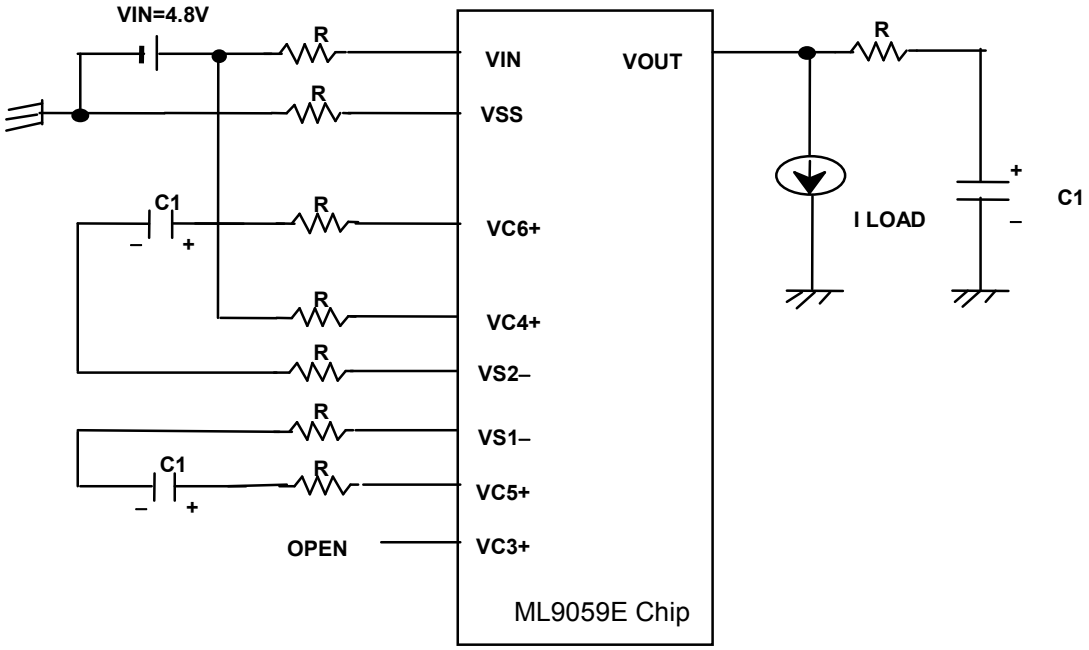
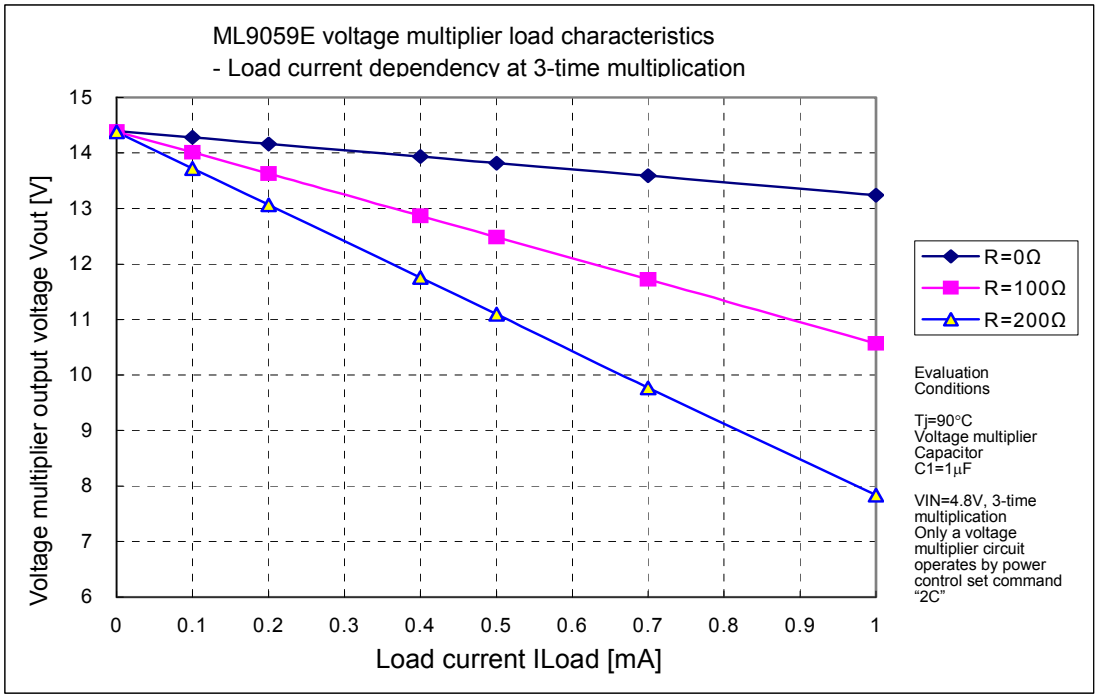


Equivalent circuit to 3-time voltage multiplier with trace resistances external to COG-mounted chip



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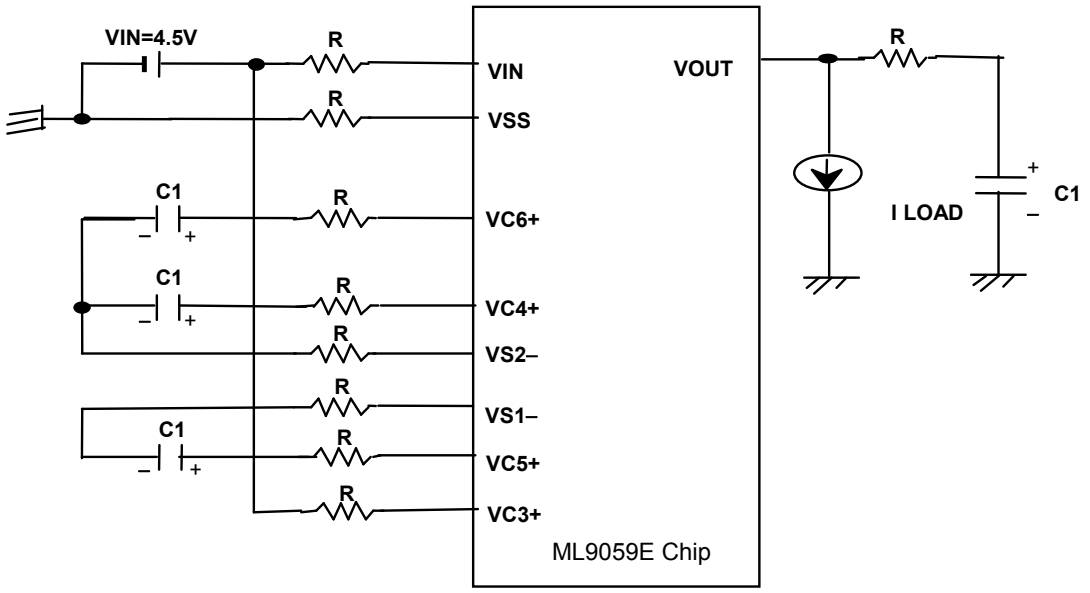
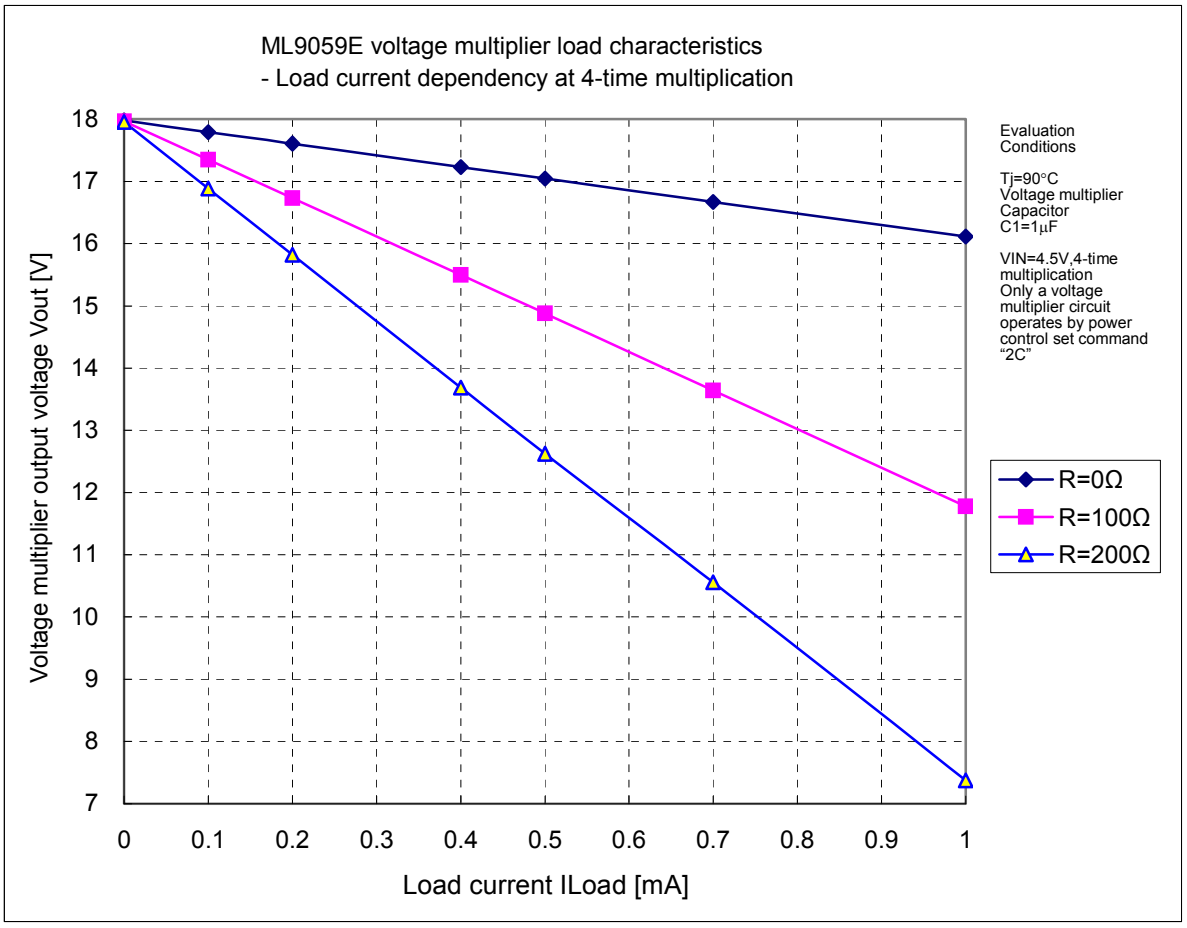
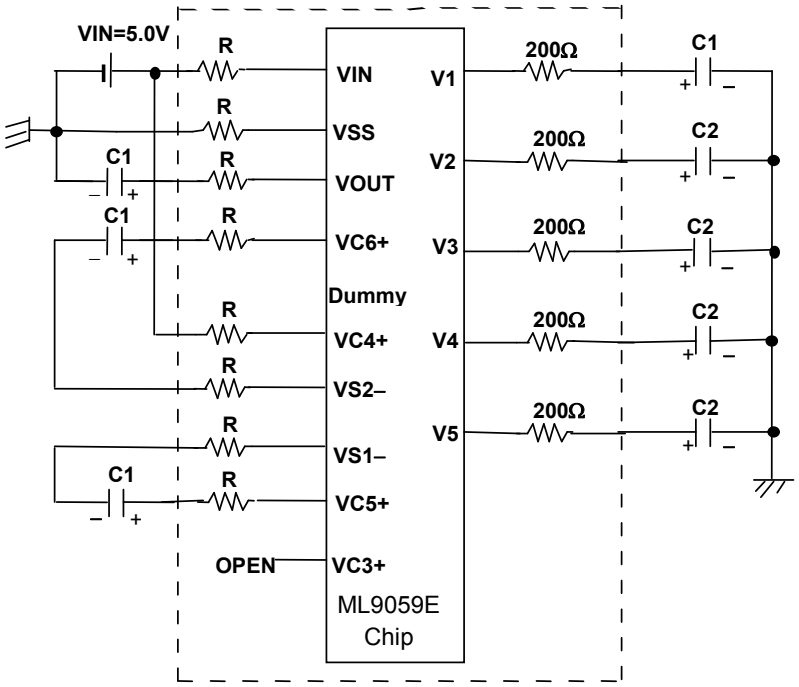


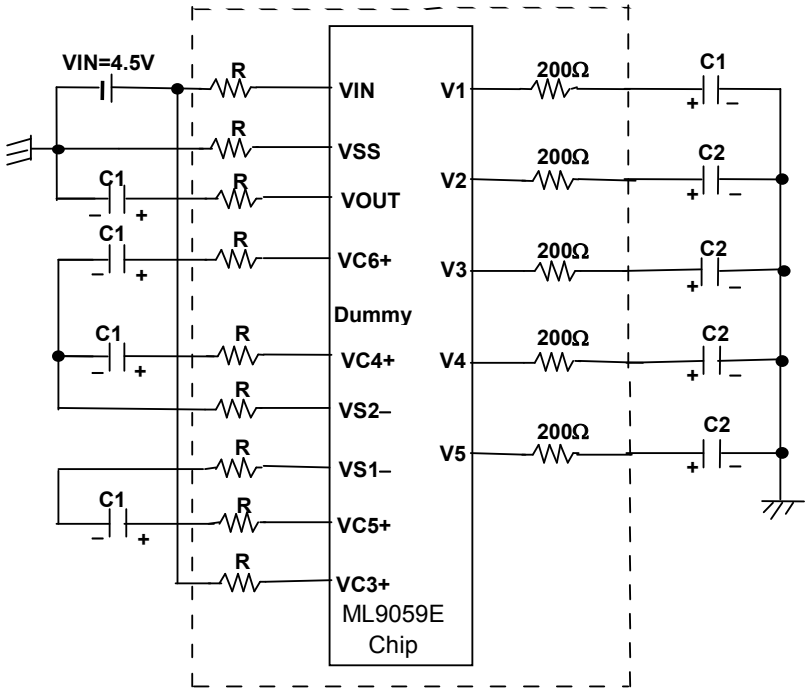
Equivalent circuit to 4-time voltage multiplier with trace resistances external to COG-mounted chip



EQUIVALENT CIRCUIT FOR EVALUATING POWER-UP STABILIZATION TIME IN COG MOUNTING



Equivalent circuit to 3-time voltage multiplier with trace resistances external to COG-mounted chip

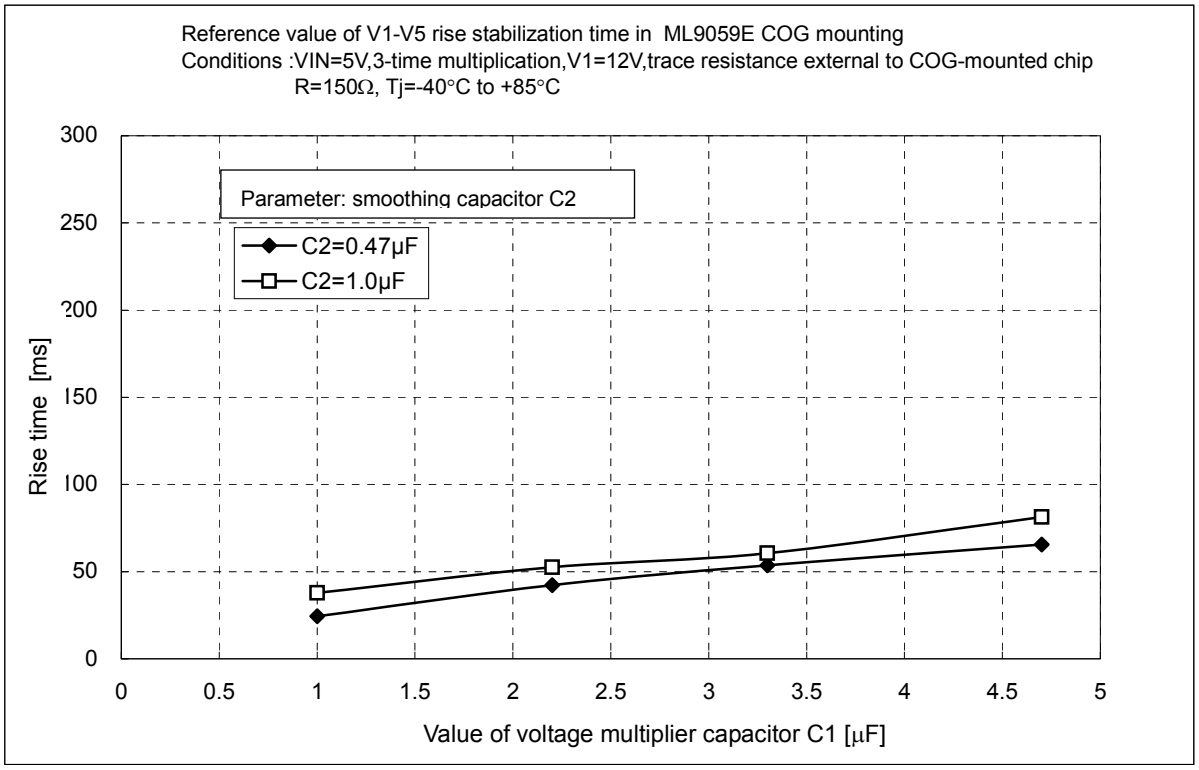


Equivalent circuit to 4-time voltage multiplier with trace resistances external to COG-mounted chip

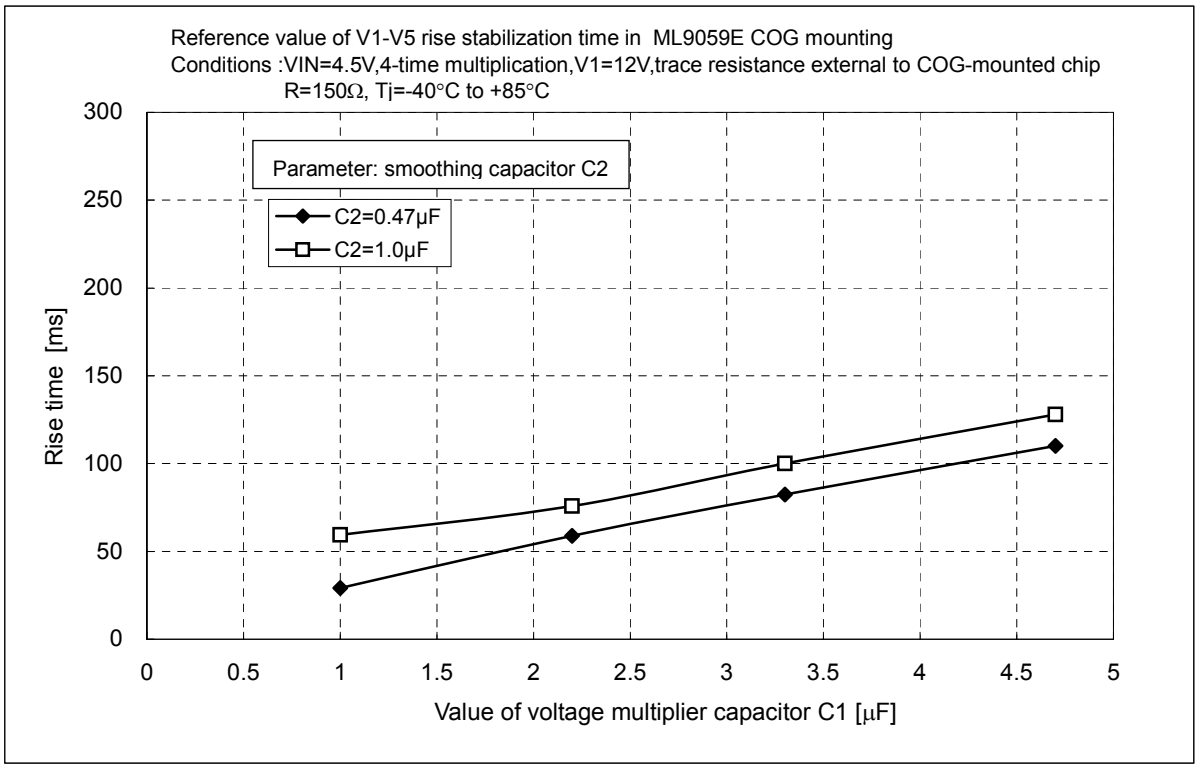
REFERENCE DATA

(The rise time until V1-V5 is stabilized when command “2F” is input after power-on in COG mounting.)

3-time voltage multiplication



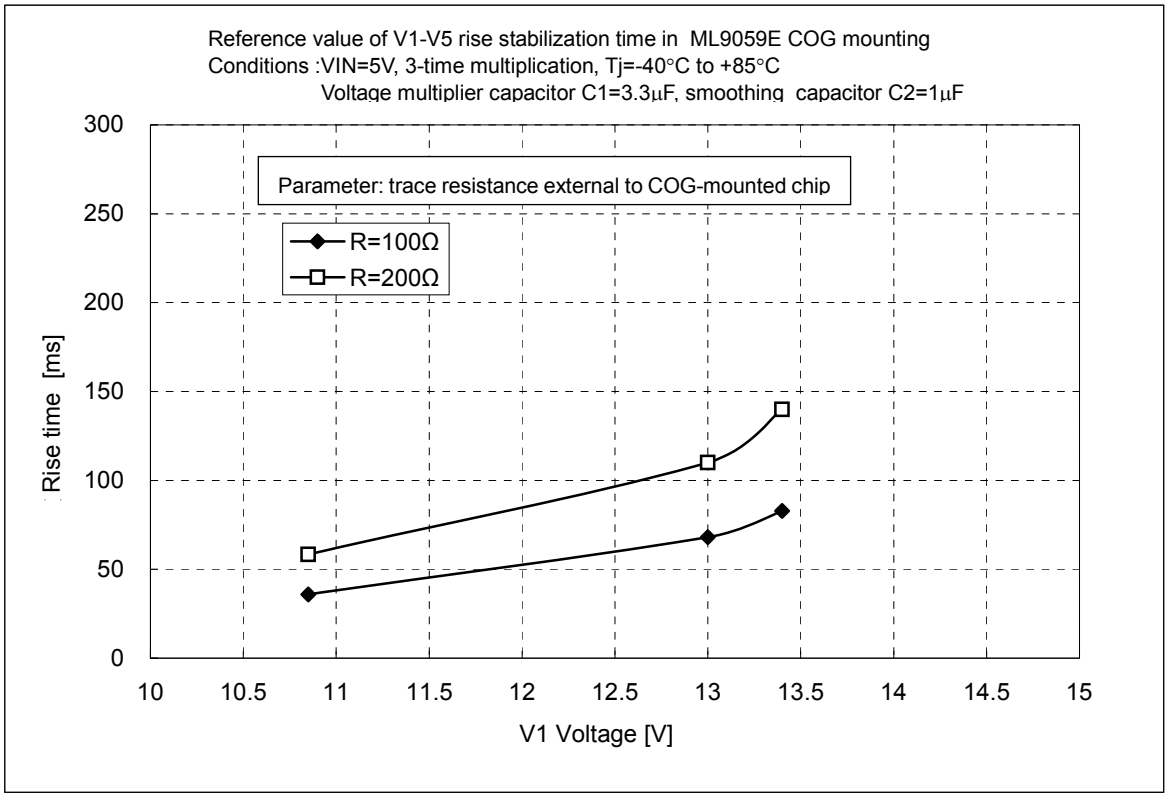
4-time voltage multiplication



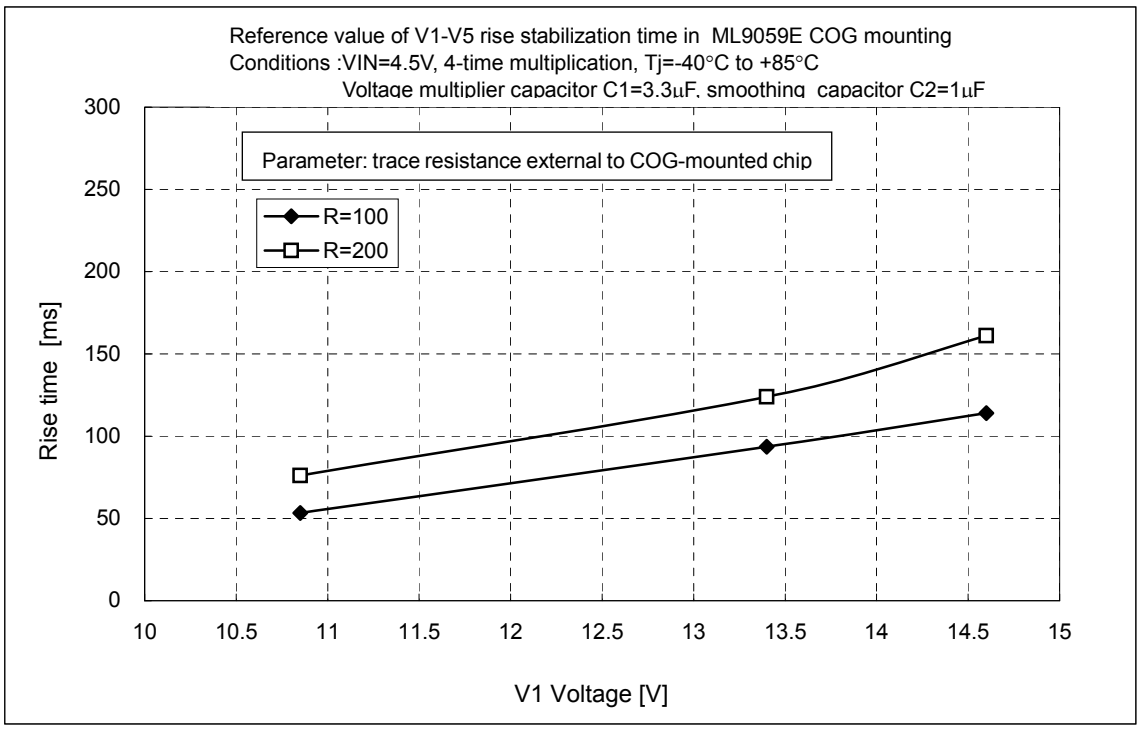
REFERENCE DATA

(The rise time until V1-V5 is stabilized when command “2F” is input after power-on in COG mounting.)

3-time voltage multiplication



4-time voltage multiplication



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9059E-01	April. 13, 2007	–	–	Final edition 1

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