ML2723

900MHz Low-IF 1.5Mbps FSK Transceiver
Preliminary Datasheet

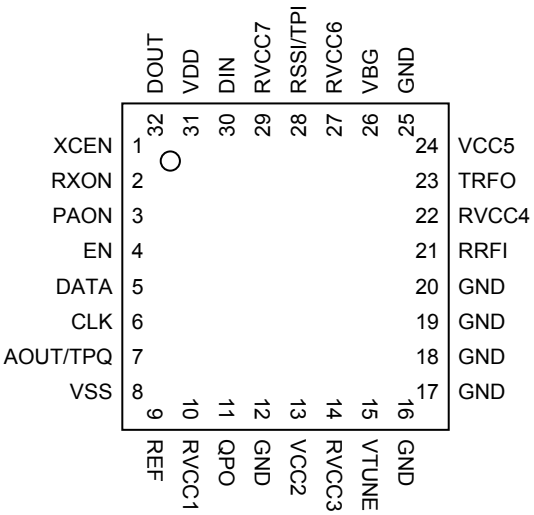
GENERAL DESCRIPTION

The ML2723 is a fully integrated 1.5Mbps frequency shift keyed (FSK) transceiver that operates in the unlicensed 900MHz ISM frequency band. The device has been optimized for digital cordless telephone applications and includes all the frequency generation, receive and transmit functions. Automatically adjusted filters eliminate mechanical tuning. The transmitter generates a -1dBm FSK output signal. The single conversion Low-IF receiver has all the sensitivity and selectively advantages of a traditional super-heterodyne without requiring costly, bulky external filters, while providing the integration advantages of direct conversion.

The phase locked loop (PLL) synthesizer is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator. This allows the ML2723 to be used in frequency hopped spread spectrum (FHSS) applications.

The ML2723 contains internal voltage regulation. It also contains PLL and transmitter configuration registers. The device can be placed in a low power standby mode for current sensitive applications.

PIN CONFIGURATION



ORDERING INFORMATION

PART #	TEMP RANGE	PACKAGE	PACK (QTY)
ML2723DM	-10°C to +60°C	32 LPCC 5x5mm	Tray (490)
ML2723DM-T	-10°C to +60°C	32 LPCC 5x5mm	Tape & Reel (2500)

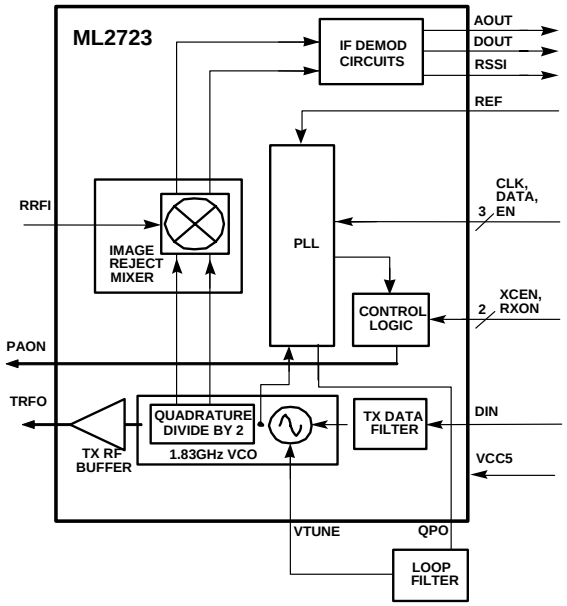
FEATURES

- Single Chip ISM Band 900MHz Radio Transceiver with –1dBm Transmit Output Power
- 1.5Mbps Maximum Data Rate
- Analog And Digital (Sliced) Data Output
- Typical Receiver Sensitivity: -95dBm At 12.5% BER
- Fully Integrated Frequency Synthesizer With Internal VCO Resonator
- Automatic Filter Calibration: Requires No Mechanical Tuning Adjustments During Manufacturing
- Low IF Receiver: No External IF Filters Required
- Control Outputs Correctly Sequence And Control External PA
- 3-Wire Control Interface
- Analog RSSI Output
- “Green” (Pb-Free) 32 LPCC package (5mm x 5mm)

APPLICATIONS

- 900MHz FSK Data Transceivers
  - Digital Cordless Phones/Headsets
  - Wireless Streaming Media
  - Wireless PC Peripherals

BLOCK DIAGRAM



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SIMPLIFIED APPLICATIONS DIAGRAM

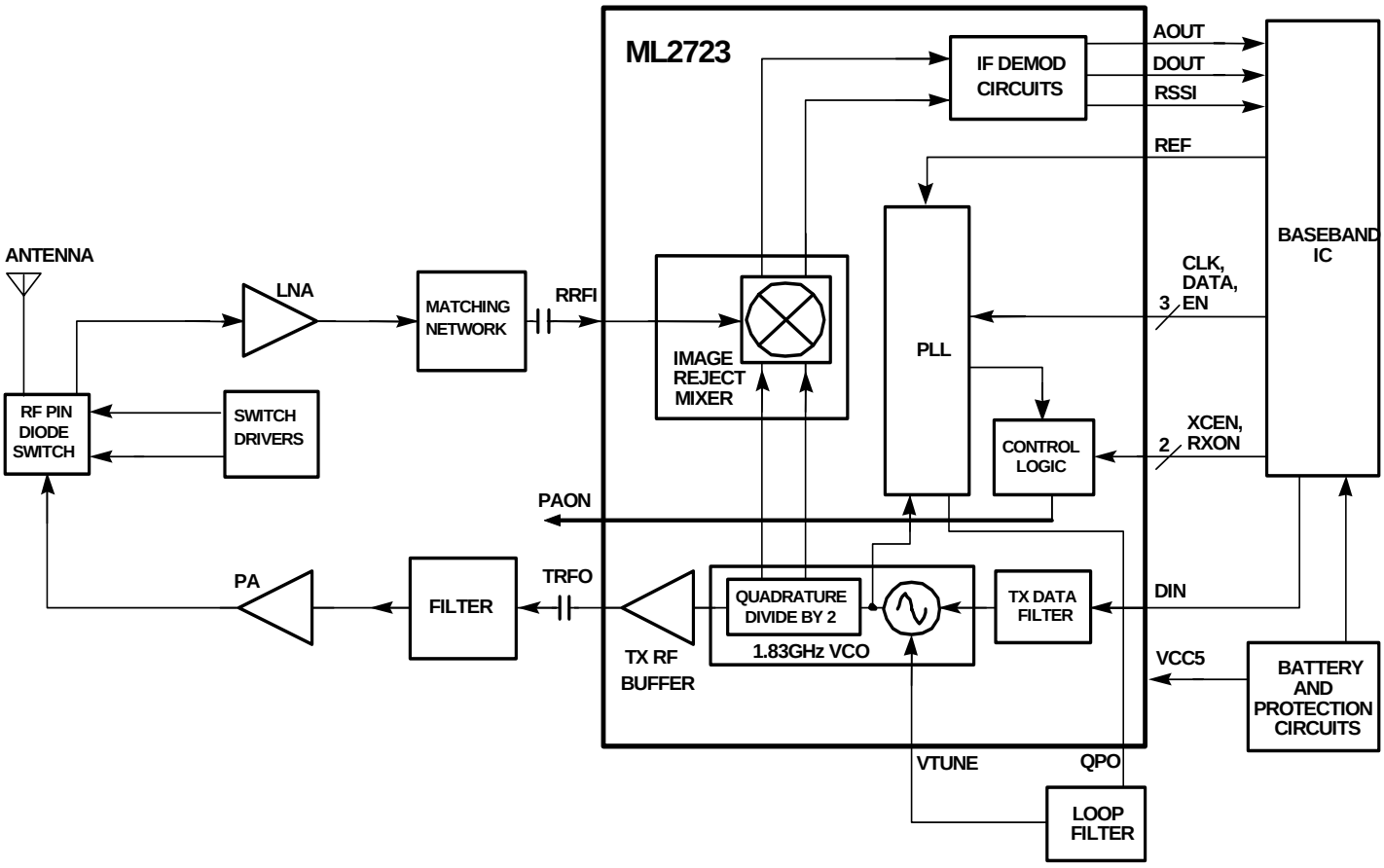


Figure 1. Simplified Application Diagram

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

VDD, VCC5 ..... 6.0V
VSS, GND ..... 0 ± 0.3V
Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Package Pin Temperature (Soldering, 10s) ..... 260°C

OPERATING CONDITIONS

Normal Temperature Range ..... -10°C to 60°C
VCC5 Range ..... 2.7V to 4.5V
Thermal Resistance (θ_{JA}) ..... 36°C/W
VDD Range (VCC5 ≥ VDD) ..... 2.7V to 4.5V

Test conditions unless otherwise specified, VCC5 & VDD = 2.8V to 3.8V, T_A = -10°C to 60°C, reference frequency = 6.144 or 12.288MHz .

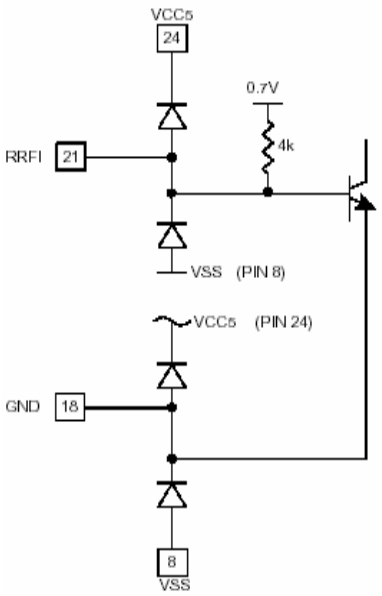
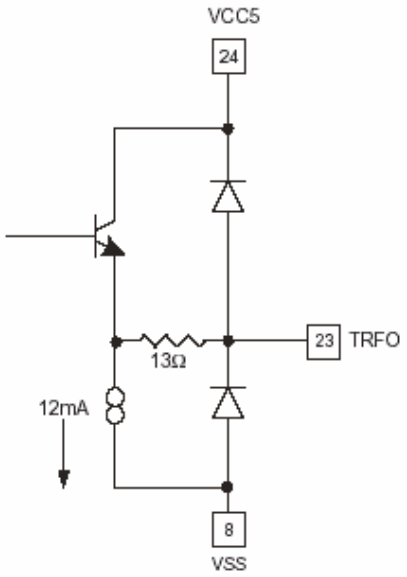
SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER CONSUMPTION						
I_{STBY}	All Circuits, Standby Mode			10	100	µA
I_{RX}, I_{TX}	Receive or Transmit Mode	T_A = 25°C, VCC5 & VDD = 3.3V	30	50	63.5	mA
I_{RX}, I_{TX}	Receive or Transmit Mode	T_A = Operating Temperature Range	20	50	70	mA
SYNTHESIZER						
f_C	LO output frequency	In 512kHz steps	902		928	MHz
Φ_N	Phase noise at driver output 1.2MHz 3MHz >7MHz	VCO phase locked, loop bandwidth 50kHz. Discontinuities, other than reference spurs, not allowed.		 -100 -120 -125		 dBc/Hz
f_{REF}	LO PLL reference frequency at phase detector	PLL main divider input is at 1.83GHz		1.024		MHz
N	LO division range integer	PLL divider limits	1024		4093	Count
I_P	LO charge pump sink/source current			5.5		mA
t_{TX2RX}	LO lock up time for Transmit/Receive frequency change	From RXON asserted		50		µs
t_{FH}	LO lock up time for channel switch	From EN asserted, any channel change in 902 to 928MHz band		100		µs
t_{WAKE}	LO lock up time from sleep	From XCEN, PLL dividers programmed		240		µs
V_{FREF}	Reference signal input level	6.144 or 12.288MHz sine wave, capacitively coupled	2.0		3.0	Vp-p

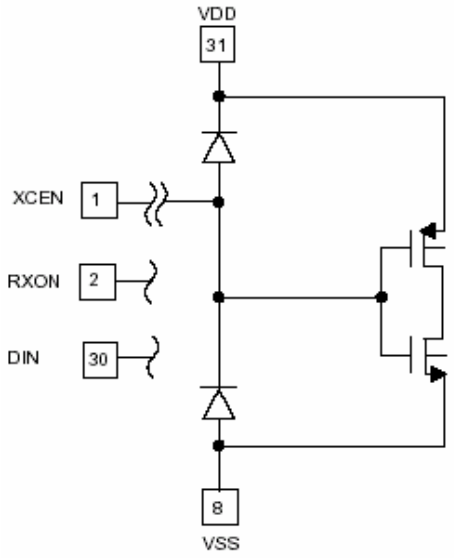
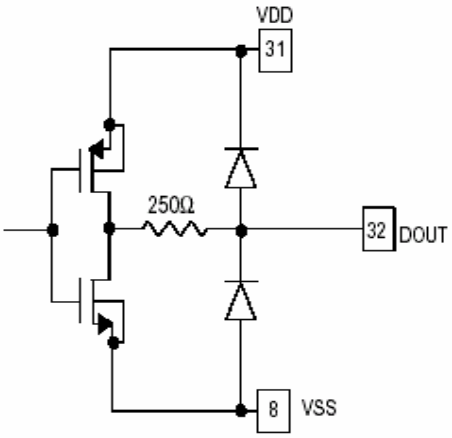
SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER						
Z_{IN}	Receiver RF impedance	f_c=915MHz		17-j50		Ω
NF	Receiver RF noise figure	f_c=915MHz		9		dB
DR_{RX}	Data Rate	FSK modulation, fdev=+/-460kHz		1.536		Mbps
S	Input Sensitivity	<12.5% CER at 1.536Mchips/s <1% BER at 1.536Mbps		-95 -89		dBm
BW_{RX}	Bandwidth	3dB nominal		770		kHz
P_{IMAX}	Maximum RX RF input	<12.5% BER at 1.536Mchip/s		8		dBm
I_{IP3}	Receiver input IP3	Test tones 2 and 4 channels away		-12		dBm
	LO Leakage at RXI			-80		dBm
IRR	Receive RF mixer image rejection	Measured at 3.5MHz offset		35		dB
	Adjacent channel rejection	-80dBm wanted signal <12.5% BER (a single interferer with 2GFSK modulation to give a -20dBc bandwidth of 1.5MHz) 1 channel 2 channels 3 or more channels		 15 40 45		dB
	Receiver settling time	RXON high to valid data			120	µs
IF FILTERS						
f_{IFC}	IF filter center frequency	After Automatic Filter Alignment		1.024		MHz
BW_{IF}	IF filter 3dB bandwidth	After Automatic Filter Alignment		1405		kHz
LIMITER, AGC, AND FM DEMODULATOR						
t_{OVLD}	Recovery from overload	From 0dBm at input		5	12	µs
	Eb/No	For 12.5% BER		3		dB
	Co-Channel rejection, 12.5% BER	-80dBm, modulated with 1.536Mbps GFSK, BT=0.5, PRBS data		4		dB
V_{ODC}	Mean DC voltage @ AOUT	R_L=100KΩ		0.8		V
V_{OPK}	AC output voltage swing @ AOUT	R_L=100KΩ		0.7		V_{PP}
RSSI PERFORMANCE						
t_{RRSSI}	RSSI rise time: < -100dBm to -15dBm into the IF mixer	20pF load, 20% to 80%	1	5.3	10	µs
t_{FRSSI}	RSSI fall time: <-15dBm to <-100dBm into the IF mixer	20pF load, 20% to 80%	1	4.4	10	µs
V_{RSMX}	RSSI maximum voltage	-15dBm in	2.2	2.8		V
V_{RSMN}	RSSI minimum voltage	No signal		0.05		V
G_{RSMID}	RSSI sensitivity, mid range		28	35	42	mV/dB
P_{RSMX}	RSSI maximum signal	Sensitivity is >50% mid range		-20		dBm
P_{RSMN}	RSSI minimum signal	Sensitivity is >50% mid range		-95		dBm
	RSSI accuracy	Measured at -40dBm input power	1.5	1.9	2.1	V

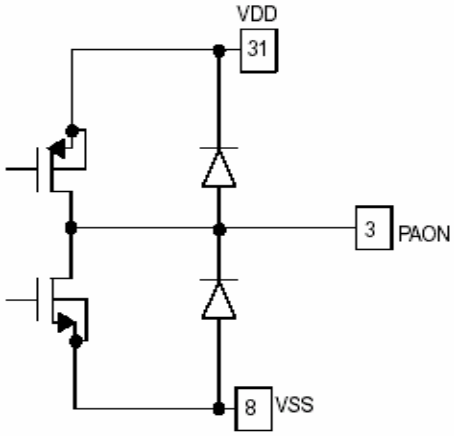
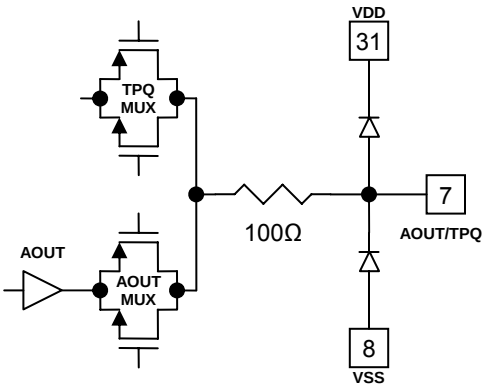
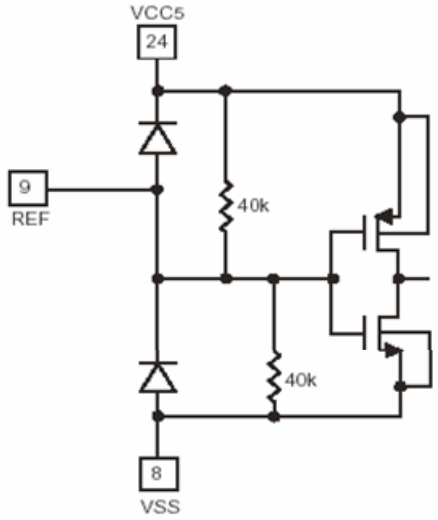
SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT RF BUFFER						
P_{OUT}	Driver amplifier output power	When matched into 50Ω	-4.5	-1.0	+2.0	dBm
	Driver amplifier output return loss	902 to 928MHz		14		dB
TRANSMIT MODULATION						
f_{DEV}	Modulation Deviation, internal VCO	5 consecutive 1 or 0 bits	400	460	560	kHz
f_{OS}	Modulation center frequency offset	Between 50µs and 10ms after PAON high	-100		+100	kHz
TRANSMIT DATA FILTER						
BW_{TX}	Transmit data filter bandwidth	3dB Bandwidth		1.4		MHz
INTERFACE LOGIC LEVELS						
V_{IH}	Input high voltage	Never exceed VDD	0.75 * VDD		VDD	V
V_{IL}	Input low voltage				0.25 * VDD	V
I_B	Input bias current		-5	0	5	µA
C_{IN}	Input capacitance	Measured at 1MHz		4	6	pF
V_{OH}	DOUT high voltage	Sourcing 0.1mA Typical value assumes 3.3V VDD	VDD - 0.6	3.08		V
V_{OL}	DOUT low voltage	Sinking 0.1mA		0.18	0.6	V
INTERFACE TIMING						
t_{RX2PA}	RX to TX switching time	Time from RXON low to PAON high		62.5	70	µs
t_{TX2EN}	TX to RX switching time	Time from RXON high to receiver enabled		72	80	µs
t_{RXEN}	Channel switching time	Time from write to PLL tuning register (EN high) to receiver enabled		320	342	µs
t_{XCEN}	Chip enable time	From XCEN high to receiver enabled with continuous reference applied		320	342	µs

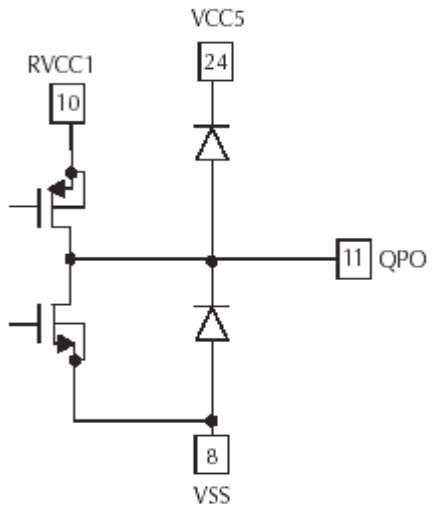
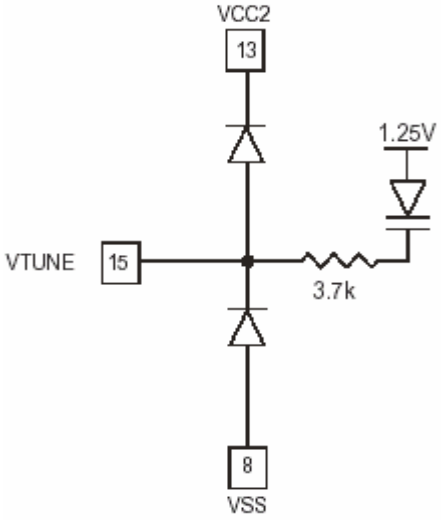
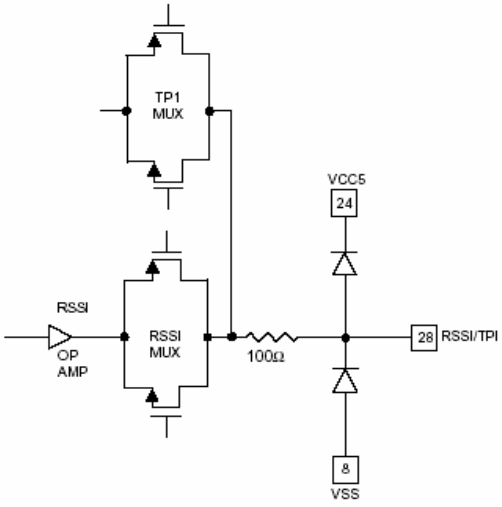
PIN DESCRIPTIONS

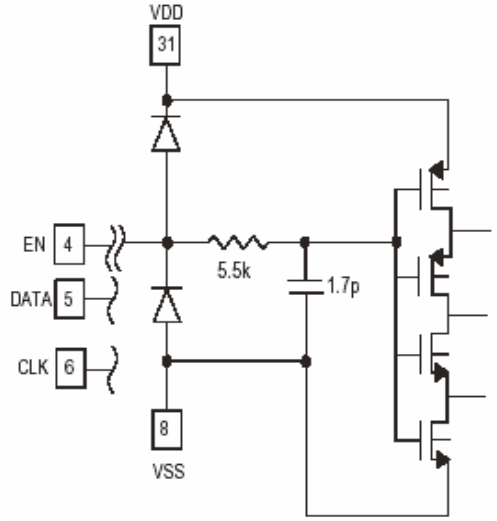
PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
POWER & GROUND				
8	VSS	I (digital)	Ground for digital I/O circuits and control logic.	
10	RVCC1	O (analog)	DC power supply decoupling point for the PLL dividers, phase detector, and charge pump. This pin is connected to the output of the regulator and to the PLL supplies. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator.	
12	GND	I (analog)	Ground for the PLL dividers, phase detector, and charge pump.	
13	VCC2	I (analog)	DC Power Supply Input to the VCO voltage regulator. Must be connected to RVCC6 (pin 27) or RVCC7 (pin 29) via decoupling network.	
14	RVCC3	O (analog)	DC power supply decoupling point for the VCO. Connected to the output of the VCO regulator. A capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
16	GND	I (analog)	DC ground for VCO and LO circuits.	
17	GND	I (analog)	Signal ground for RF small signal circuits. Pins 17, 18, and 19 should have short, direct connections to each other and additional connections to ground.	
18	GND	I (analog)	Ground return for the Receive RF input.	
19	GND	I (analog)	Signal ground for the Receive mixers.	
20	GND	I (analog)	DC and Signal ground for the Transmit RF Output buffer.	
22	RVCC4	O (analog)	DC power supply decoupling point for the LO chain. Connected to the output of a regulator. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator.	
24	VCC5	I (analog)	DC power supply input to voltage Regulators and unregulated loads. VCC5 is the main (or master) analog VCC pin. There must be a capacitor to ground from this pin to decouple (bypass) noise and to stabilize the regulator.	
25	GND	I (analog)	DC ground to IF, Demodulator, and Data Slicer circuits.	
27	RVCC6	O (analog)	DC power supply decoupling point for Quadrature Mixer and IF filter circuits. A capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
29	RVCC7	O (analog)	DC power supply decoupling point for IF, Demodulator, and Data Slicer circuits. A capacitor must be tied between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
31	VDD	I (digital)	DC power supply input to the interface logic and control registers. This supply is not connected internally to any other supply pin, but its voltage must be less than or equal to the VCC5 supply and greater than 2.7V. A capacitor must be tied between this pin and ground to decouple (bypass) noise.	
TRANSMIT/RECEIVE				
21	RRFI	I (analog)	Receive RF Input. Nominal impedance at 902 to 928MHz is 17-50j Ω with a simple matching network required for optimum noise figure. This input is to the base of an NPN transistor and should be AC coupled.	
23	TRFO	O (analog)	Transmit RF Output. This output is an emitter follower and should be AC coupled.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
DATA				
30	DIN	I (CMOS)	Transmit Data Input. Drives the transmit pulse shaping circuits. Serial digital data on this pin becomes FSK modulation on the Transmit RF output. The logic timing on this pin controls data timing. Internal circuits determine the modulation deviation. This is a standard CMOS input referenced to VDD and VSS.	
32	DOUT	O (CMOS)	Serial digital output after demodulation, chip rate filtering and center data slicing. A CMOS level output (VSS to VDD) with controlled slew rates. A low drive output designed to drive a PCB trace and a CMOS logic input while generating minimal RFI. In digital test modes this pin becomes a test access port controlled by the serial control bus.	
MODE CONTROL AND INTERFACE LINES				
1	XCEN	I (CMOS)	Enables the bandgap reference and voltage regulators when high. With XCEN low the device consumes only leakage current in STANDBY mode when low. XCEN low also preserves register contents and allows register writes. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	**See Pin 30**
2	RXON	I (CMOS)	Switches the transceiver between TRANSMIT and RECEIVE modes. Circuits are powered up and signal paths reconfigured according to the operating mode. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	**See Pin 30**

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
3	PAON	O (CMOS)	Enables the off-chip PA at the correct times in a Transmit slot. Goes high when transmit RF is present at TRFO; goes low 5µs before transmit RF is removed from TRFO. Has interlock logic to shut down the PA if the PLL does not lock.	
7	AOUT/TPQ	O (analog)	Analog data output after chip rate filtering. Output must be data-sliced using eternal discrete circuitry or a data slicer resident on an accompanying baseband chip. In analog test modes, this pin and the RSSI output become test access points controlled by the serial control bus.	
9	REF	I	Input for the 12.288MHz or 6.144MHz reference frequency. This input is used as the reference frequency for the PLL and as a calibration frequency for the on-chip filters. This is a self-biased CMOS input that is designed to be driven either by an AC-coupled sine wave.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
11	QPO	O	Charge Pump Output of the phase detector. This is connected to the external PLL loop filter.	
15	VTUNE	I	VCO Tuning Voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents.	
26	VBG	O	Internal Bandgap Reference Voltage. Decoupled to ground with a 220nF capacitor.	
28	RSSI/TPI	O	Buffered Analog RSSI output with a nominal sensitivity of 35mV/dB. An RF input signal range of –95 to –20dBm gives an RSSI voltage output of zero to 2.7V.	

PIN	SIGNAL NAME	I/O	FUNCTION	DIAGRAM
SERIAL BUS SIGNALS				
4	EN	I (CMOS)	Enable pin for the three-wire serial control bus that sets the operating frequency and programmable options. The control registers are loaded on a low-to-high transition of the signal. Serial control bus data is ignored when this signal is high. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
5	DATA	I (CMOS)	Serial Control Bus Data. 16-bit words, which include programming data and the two-bit address of a control register. This is a CMOS input, and the thresholds are referenced to VDD and VSS.	
6	CLK	I (CMOS)	Serial control bus data is clocked in on the rising edge when EN is low. This is a CMOS input; the thresholds are referenced to VDD and VSS.	

FUNCTIONAL DESCRIPTION

The ML2723 enables the design and manufacture of low-cost, high-performance FSK transceivers. It can also be used as a 900MHz digital cordless telephone transceiver. Integral to the ML2723 is a low-IF receiver whose LO port is driven from an internal synthesizer. Included are image rejection IF filters, limiters, discriminator, data slicers, and baseband low-pass data filters. It also contains internal voltage regulators to protect critical circuits from power supply noise and transmit modulation circuits.

The ML2723 is designed to transmit and receive 1.536M chips per second in 2.048MHz spaced channels in the 902 to 928MHz ISM band. A single synthesizer is used for both the receiver and the FSK transmitter. The phase locked loop (PLL) is completely integrated, including the voltage controlled oscillator (VCO), tuning circuits, and VCO resonator.

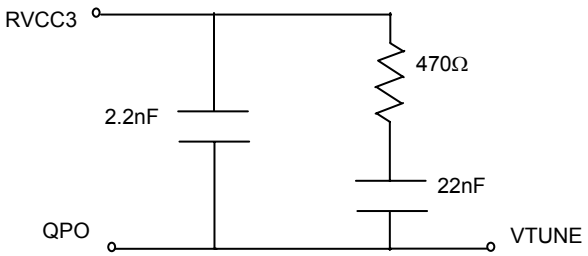
The ML2723 has an internal control interface that programs the synthesizer, the mode of operation, the external LNA and PA, and provides a convenient and flexible interface to various baseband processors. For power level monitoring an RSSI block is included.

In **RECEIVE MODE**, the ML2723 is a single conversion low IF receiver. The demodulation is followed by a matched bit rate filter (to AOUT/TPQ) and a data slicer (to DOUT). The sliced data is provided to a baseband chip for despreading. All channel filtering and demodulation is performed using active filters, which are automatically aligned. A matched bit rate filter and a data slicer follow the demodulator.

In **TRANSMIT MODE**, the ML2723 uses the Receive mode VCO and frequency division, with a driver amplifier providing typically -1 dBm output to feed the power amplifier. The PLL frequency synthesizer loop is opened during the transmit time slot, and the VCO is directly modulated by low-pass filtered circuits from the internal modulation filter.

The ML2723 uses multiple voltage regulators to protect sensitive internal circuits from power supply noise. Separate regulators supply the PLL dividers, RF circuits and IF circuits. Each of these regulators takes its power from VCC5, and supplies power internally to its respective RVCCn pin. External capacitors are required at each RVCCn pin to decouple the outputs of the internal regulators. The VCO regulator takes its power from the VCC2 pin, which is normally connected, to the RVCC6 (pin 27) or RVCC7 (pin 29). An external decoupling capacitor is also used on the internal bandgap voltage reference to improve the noise performance of the regulators.

The integrated PLL frequency synthesizer includes a fully integrated VCO, prescaler, phase detector and charge pump. The reference frequency is generated from the incoming signal at the REF pin, which can be either 6.144MHz or 12.288MHz. The loop filter is external to allow customers to optimize their loop bandwidth to their system's lock time and in-band phase noise requirements. This frequency-agile synthesizer allows the ML2723 to be used in frequency hopped spread spectrum (FHSS) applications with nominal channel spacing of 2.048MHz. Carrier frequency is programmed via the configuration registers and 3-wire serial interface. The VCO tank circuit (inductor and varactor) is fully integrated.



Example 38kHz Loop Filter

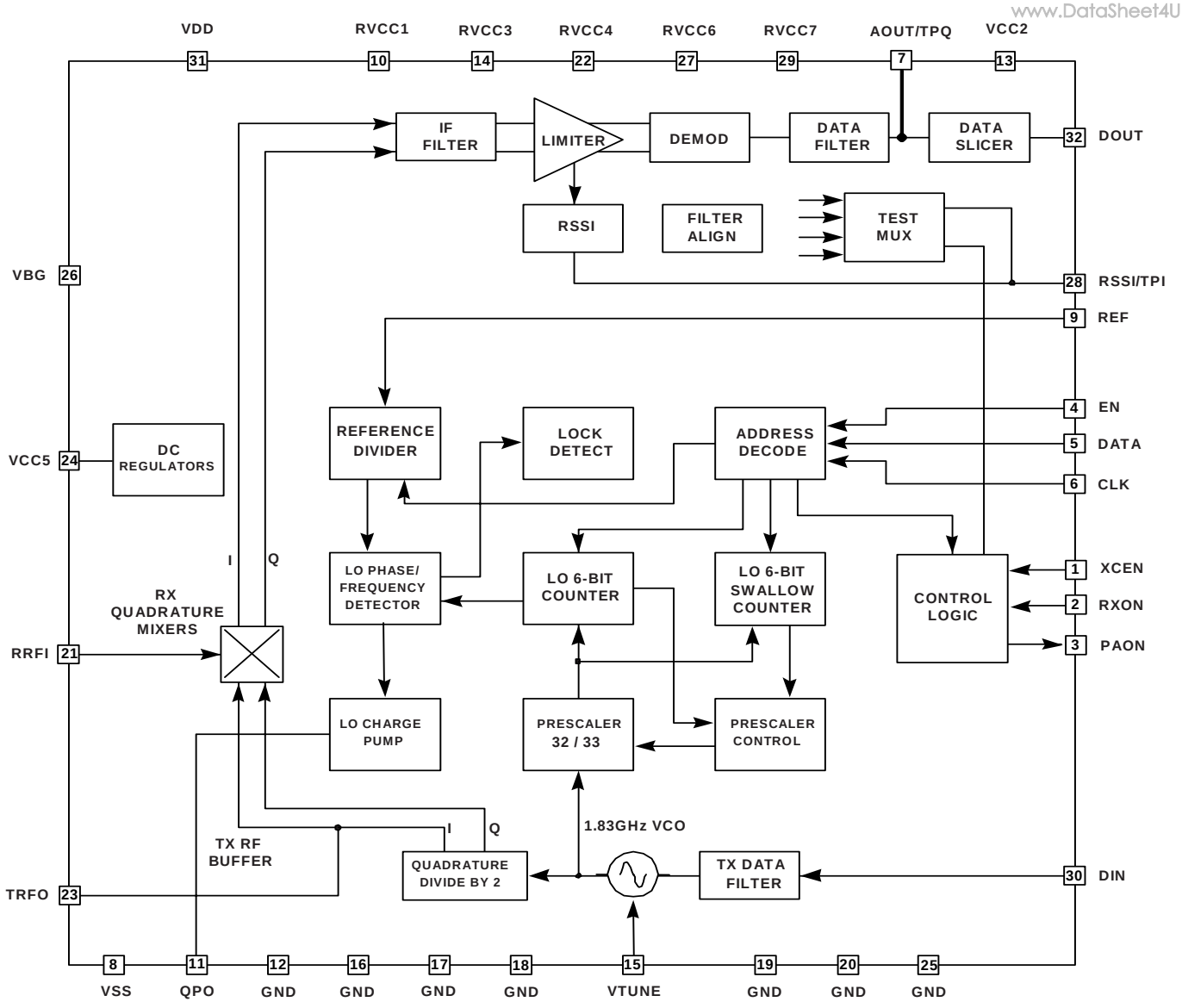


Figure 2. ML2723 Block Diagram

MODES OF OPERATION

OVERVIEW

- **STANDBY:** All circuits powered down, except the control interface (Static CMOS)
- **RECEIVE:** Receiver circuits active
- **TRANSMIT:** PLL open loop, modulated RF output available from the IC

The two operational modes are RECEIVE and TRANSMIT. They are set by the RXON control (pin 2). XCEN (pin 1) is the chip enable/disable and can be set for standby operation. The relationship between the parallel control lines and the mode of operation of the IC is given in Table 1.

XCEN	RXON	MODE	TRANSCEIVER MODE
0	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	RECEIVE	Receiver time slot
1	0	TRANSMIT	Transmit time slot

Table 1: Modes of Operation

MODE CONTROL

The ML2723 is intended for use in TDD and TDMA radios in battery-powered equipment. To minimize power consumption it is designed to switch rapidly from a low power mode (STANDBY) to receive or transmit. The ML2723 can also make a quick transition from receive to transmit for TDD operation. Prior to transmitting or receiving, time should be allowed for the PLL to lock up and for the filters to be aligned. When the ML2723 is operated in single-carrier TDD mode, the LO is automatically shifted by the second (low) IF frequency when the device is switched between RECEIVE and TRANSMIT modes.

ML2723 carrier frequency can be changed (hopped) between transmissions. Carrier frequency (channel) is modified in the ML2723 by writing a corresponding new value to the PLL frequency register.

RECEIVE

The ML2723 uses a single-conversion heterodyne receiver with a nominal IF of 1.024MHz. The signal flow in RECEIVE mode is from the RF input, through an image reject quadrature mixer, limiter, frequency-to-voltage converter, and data filter. The received analog data is then output on the AOUT/TPQ pin as well as sent to the internal data slicer, which presents digital NRZ data at the DOUT pin. A 20dB step AGC extends the dynamic range of the receiver.

The ML2723 receive chain is a Low IF receiver using advanced integrated radio techniques to eliminate external IF filters and minimize external RF filter requirements. The precision filtering and demodulation circuits give improved performance over conventional radio design using external filters while providing integration comparable to advanced direct conversion radio designs.

Receive Signal Strength Indication (RSSI)

RSSI is an indication of field strength. It is typically used to control transmit power to conserve battery life. It may also be used to determine if a given channel is occupied (see Figure 3).

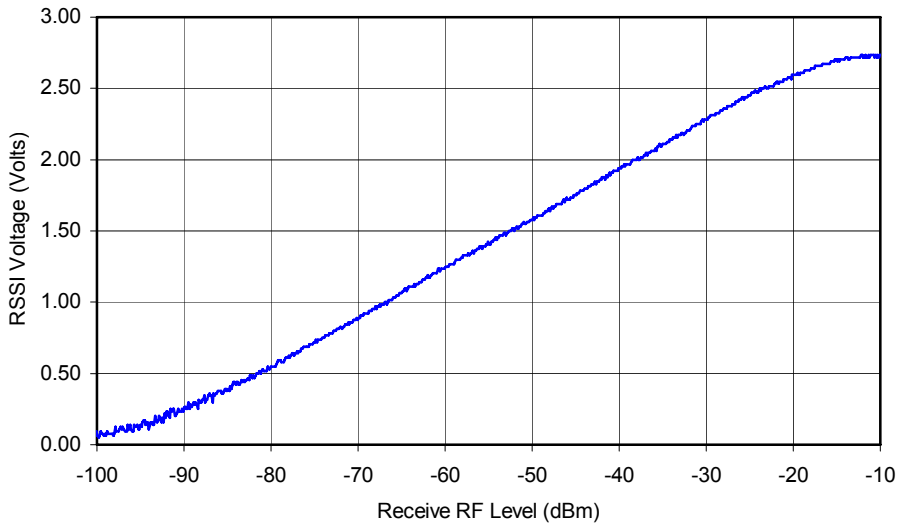


Figure 3. Typical RSSI Response

Automatic Filter Alignment

When the ML2723 is placed in RECEIVE mode, it automatically tunes all the internal filters using the reference frequency from the REF pin. This self-calibration sets:

- Discriminator center frequency
- IF filter center frequency and bandwidth
- Receiver data low-pass filter bandwidth
- Transmit data low pass filter bandwidth

TRANSMIT MODE

In TRANSMIT mode, the VCO is directly modulated with filtered FSK transmit data. The ML2723 transmitter is a 2-FSK transmitter using a directly modulated open loop VCO. The ML2723 design supports transmit time slot lengths up to 10ms, and the time required to set up the transmitter for a new time slot (TXCAL mode) is 62.5µs. This type of transmitter is simple, low power, and well suited to a time-time slotted system. The transmitter uses the stored VCO tuning voltage on the PLL loop filter to set the VCO frequency for the duration of the transmitter time slot. The modulation is introduced through a second VCO tuning port. This modulation port has a much lower tuning sensitivity than the main tuning port in order to produce the ±460kHz FSK deviation. Compensation circuits stabilize the modulation deviation over the VCO tuning range, and internal logic manages the correct transition from TXCAL to TRANSMIT mode.

The operating cycle of the transmitter starts with the falling edge of RXON. In the first 62.5µs after the falling edge of RXON, a calibration mode (TXCAL) is triggered. The data filter input is zeroed and the PLL locks the VCO frequency to the desired RF channel center frequency. A CW signal at the selected RF channel frequency comes out of the Transmit RF output. When the internally generated PLLEN control line changes state, the transmitter starts its transition to TRANSMIT mode. The PLL charge pump is disabled, leaving the PLL loop filter to hold the correct tuning voltage for this channel. The data formatter injects an NRZ bipolar data waveform into the Transmit data filter. The Transmit data filter band-limits this waveform, and feeds it to the modulation compensation circuits. These scale the modulation voltage (depending on the VCO tuning voltage) and drive the VCO tuning port with the scaled, filtered modulation. The voltage on the modulation port swings above and below its central value to produce 2-FSK modulation on the VCO. The modulation filtering is sufficient to meet the FCC occupied bandwidth and out-of-band emissions requirements, and does not introduce significant ISI (Inter Symbol Interference).

The transmit modulation filter is automatically tuned during the first part of every RX and TX time (RXCAL&TXCAL) to remove the need for production alignment. When the chip is first powered up, the tuning information is reset to mid-range. The ML2723 should then be enabled with RXON high. The rising edge on XCEN will trigger a complete calibration of all the on chip filters, which takes 320µs. This ensures the modulation filters are aligned to prevent unwanted spurious emissions.

Prior to transmitting the PLL must tune to the intended RF center frequency of the transmission. This occurs in TXCAL mode. The Transmit modulation is disabled and any input on the DIN (pin 30) is ignored. The transmit output buffer is enabled during TXCAL mode. To prevent spurious emissions due to the PLL locking, any external antenna switch or PA should be disabled during TXCAL mode. For optimum performance we recommend that the second harmonic level reflected back into the output TRFO (pin 23), be less than –30dBm.

Phase Locked Loop (PLL) and Channel Selection

The PLL synthesizes channel frequencies to a 512kHz resolution, which is more finely spaced than the 1.536MHz signal bandwidth. Non-overlapping channels are spaced by 2.048MHz where the IF filter and image reject mixer give a typical adjacent channel rejection of 25dB. There are twelve non-overlapping channels in the 902 to 928MHz ISM band (see Table 2).

CHANNEL	FREQUENCY IN MHz	CHANNEL	FREQUENCY IN MHz
1	903.680	7	915.968
2	905.728	8	918.016
3	907.776	9	920.064
4	909.824	10	922.112
5	911.872	11	924.160
6	913.920	12	926.208

Table 2. Non-Overlapping Channel Frequencies

The LO PLL is programmed via a 3-wire serial control bus. Program words are clocked in on the DATA line (pin 5) by the CLK (pin 6), and loaded into the dividers or control circuits when EN (pin 4) is asserted. There is no check for errors in the program words. Once loaded, register contents are preserved while VDD is present. The register status and operation is independent of the mode of operation of the PLL.

The reference signal from an external crystal oscillator at either 6.144MHz or 12.288MHz is fed to a programmable reference divider. The 1.024MHz reference divider output is fed to the LO phase frequency detector. The PLL prescaler input comes from the VCO at 1.83GHz, so the 1.024MHz comparison frequency gives 512kHz frequency resolution at 902 to 928MHz.

STANDBY MODE

In STANDBY the ML2723 transceiver is powered down. The only active circuits are the control interfaces, which are static CMOS to minimize power consumption. The serial control interface (and control registers) remain powered up and will accept and retain programming data as long as the digital supply is present. The ML2723 serial control registers should be loaded with control and configuration data before any active mode is selected. The filter alignment registers are reset at power up.

TEST MODE

The RF to digital functionality of the ML2723 requires special test mode circuitry for IC production test and radio debugging. A test register, available via the 3-wire serial interface, controls the test multiplexers.

CONTROL INTERFACES

There are two control interfaces: PARALLEL and SERIAL.

PARALLEL INTERFACE

The parallel interface provides immediate control and monitoring of the ML2723. Input signals include:

- **XCEN:** Transceiver enable. Places the ML2723 in Standby or Active (when asserted) modes.
- **RXON:** Receive On. Places an Active ML2723 in Receive mode when asserted.
- **REF:** Reference frequency input

Output signals include:

- **RSSI:** Received Signal Strength Indicator: indicates the power of the received signal
- **PAON:** External Power Amplifier Control Pin

SERIAL INTERFACE

A 3-wire serial interface (EN, DATA, CLK) is used for programming the ML2723 configuration registers, which control device mode, pin functions, PLL and reference dividers, internal test modes, and filter alignment. Data words are entered beginning with the MSB (“big-endian”). The word is divided into a leading 14-bit data field followed by a 2-bit address field. When the address field has been decoded the destination register is loaded on the rising edge of EN. **Providing less than 16 bits of data will result in unpredictable behavior when EN goes high.**

Data and clock signals are ignored when EN is high. When EN is low, data on the DATA pin is clocked into a shift register by rising edges on the CLK pin. The information is latched when EN goes high. This serial interface bus is similar to that commonly found on PLL devices. The data latches are implemented in static CMOS and use minimal power when the bus is inactive. Table 3 and Figure 4 provide timing and register programming illustrations.

SYMBOL	PARAMETER	TIME (ns)
t_R	Clock input rise time	15
t_F	Clock input fall time	15
t_{CK}	Clock period	>50
t_W	Minimum pulse width	2000
t_D	Delay from last clock falling edge	>15
t_{SE}	Enable setup time to ignore next rising clock	>15
t_S	Data-to-clock setup time	>15
t_H	Data-to-clock hold time	>15

Table 3. 3-Wire Bus Timing Characteristics

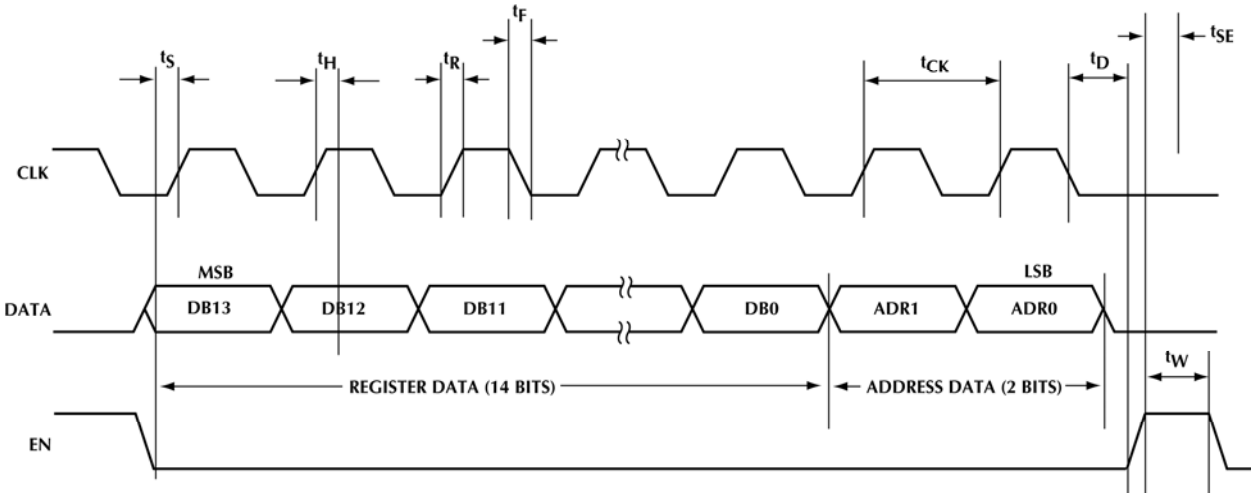


Figure 4. Serial Bus Timing for Address and Data Programming

CONTROL INTERFACES AND REGISTER DESCRIPTIONS

REGISTER INFORMATION

A unidirectional 3-wire serial bus sets the ML2723's transceiver parameters and programs the PLL circuits. Programming is performed by entering 16-bit words into the ML2723 serial interface. Three 16-bit registers are partitioned such that 14 bits are dedicated for data to program the operation and two bits identify the register address.

The three registers are:

- **Register 0:** PLL Configuration
- **Register 1:** Channel Frequency Data
- **Register 2:** Internal Test Access

Figure 5 shows a register map. Table 4 through Table 6 provide detailed diagrams of the register organization: Table 4 and Table 5 outline the PLL configuration and channel frequency registers, and Table 6 displays the filter tuning and test mode register.

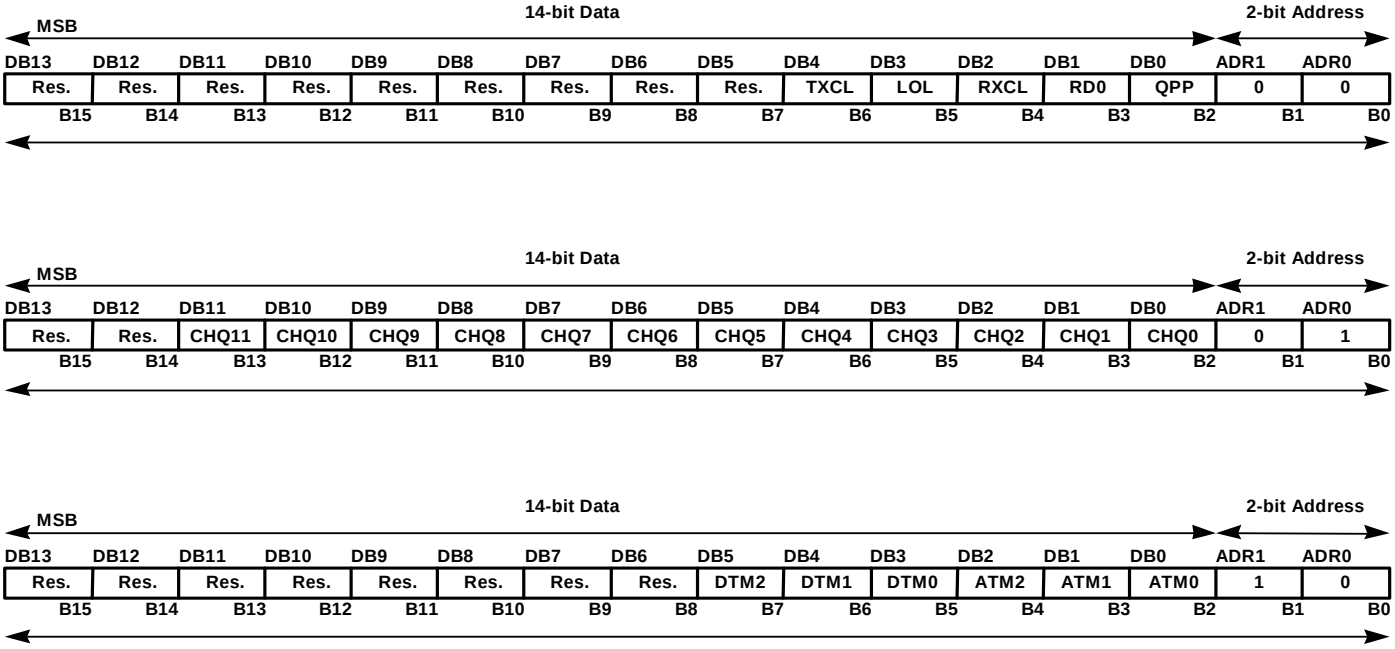


Figure 5. Register Organization

DATA BIT	NAME	DESCRIPTION	USE
B15 (MSB) / DB13	Reserved	Reserved	Set all bits to 0 (zero)
B14 / DB12	Reserved	Reserved	
B13 / DB11	Reserved	Reserved	
B12 / DB10	Reserved	Reserved	
B11 / DB9	Reserved	Reserved	
B10 / DB8	Reserved	Reserved	
B9 / DB7	Reserved	Reserved	
B8 / DB6	Reserved	Reserved	
B7 / DB5	Reserved	Reserved	Set to 0 (zero)
B6 / DB4	TXCL	Transmit Test Mode	0: FSK modulation in Transmit mode 1: CW (no modulation in Transmit mode)
B5 / DB3	LOL	PLL Frequency Shift	0: LO shift is 0 Hz for Transmit, 1.024MHz for Receive 1: LO shift is 1.024MHz for Transmit, 0Hz for Receive
B4 / DB2	RXCL	PLL Mode in Normal Receive Operation	0: PLL open loop during Receive 1: PLL closed loop during Receive
B3 / DB1	RD0	Reference Frequency Select	0: 6.144MHz nominal reference frequency 1: 12.288MHz nominal reference frequency
B2 / DB0	QPP	PLL Charge Pump Polarity	0: Freq. sig. < freq. ref.; Charge pump sources current 1: Freq. sig. < freq. ref.; Charge pump sinks current
B1 / ADB1	ADR1	MSB Address Bit	ADR1 = 0
B0 (LSB) / ADB0	ADR0	LSB Address Bit	ADR0 = 0

Table 4. Register 0 -- PLL Configuration Register

DATA BIT	NAME	DESCRIPTION	USE
B15 (MSB) / DB13	Reserved	Channel Frequency select bits	Set all bits to 0 (zero)
B14 / DB12	Reserved		
B13 / DB11	CHQ11		Divide ratio = f_c / 0.512
B12 / DB10	CHQ10		
B11 / DB9	CHQ9		
B10 / DB8	CHQ8		
B9 / DB7	CHQ7		
B8 / DB6	CHQ6		
B7 / DB5	CHQ5		
B6 / DB4	CHQ4		
B5 / DB3	CHQ3		
B4 / DB2	CHQ2		
B3 / DB1	CHQ1		
B2 / DB0	CHQ0		
B1 / ADB1	ADR1	MSB Address Bit	ADR1 = 0
B0 (LSB) / ADB0	ADR0	LSB Address Bit	ADR0 = 1

Table 5. Register 1 – Channel Frequency Register

DATA BIT	NAME	DESCRIPTION	USE
B15 (MSB) / DB13	Reserved	Reserved	Set all bits to 0 (zero)
B14 / DB12	Reserved		
B13 / DB11	Reserved		
B12 / DB10	Reserved		
B11 / DB9	Reserved		
B10 / DB8	Reserved		
B9 / DB7	Reserved		
B8 / DB6	Reserved		
B7 / DB5	DTM2	Digital Test Control Bits	See Table 15
B6 / DB4	DTM1		
B5 / DB3	DTM0		
B4 / DB2	ATM2	Analog Test Control Bits	See Table 14
B3 / DB1	ATM 1		
B2 / DB0	ATM 0		
B1 / ADB1	ADR1	MSB Address Bit	ADR1 = 1
B0 (LSB) / ADB0	ADR0	LSB Address Bit	ADR0 = 0

Table 6. Register 2 – Test Mode Register

CONTROL REGISTER DESCRIPTIONS

Power-On State

All register values are set to 0 (zero) on Power Up. Power up is defined as occurring when VDD (pin 31) ≥ 2.0V (typical). The register default values are valid after power up. The PLL divide ratio and PLL configuration registers must be programmed before XCEN is asserted for the first time.

Address and Data Bits (ADR)

Each of the three registers is identically configured. Each is divided into a fourteen (14) bit data field and a two (2) bit address field. The 16 bits are input serially (see Figure 5) with the 14 data bits, most significant bit (DB13) first followed by the two address bits, most significant bit (ADR1) first. The last 16 bits clocked into the ML2723 will be loaded into the specified register. Loading less than 16 bits into any register will cause unpredictable device functionality.

RES Bit Locations (Reserved)

Bits identified as reserved must always have a logic 0 (zero) value for correct device operation. Power-on reset clears all reserved bits to zero. Each reserved bit must be programmed to logic zero whenever any of the three registers are reprogrammed.

REGISTER #0, PLL CONFIGURATION

PLL Charge Pump Polarity (QPP): DB0

This bit sets the charge pump polarity to sink or source current. For a majority of applications, this bit is cleared (QPP = 0). For applications where an external amplifier is in the loop filter, this bit is set to 1 to change the charge pump polarity (see Table 7).

QPP	PLL CHARGE PUMP POLARITY
0	Frequency signal < frequency reference. Charge pump sources current.
1	Frequency signal < frequency reference. Charge pump sinks current.

Table 7. PLL Charge Pump Polarity

Reference Divide Bit Zero (RD0): DB1

This bit sets the reference division of the PLL to either 6 or 12 (see Table 8).

RD0	REFERENCE DIVISION	NOMINAL REFERENCE FREQUENCY
0	6	6.144MHz
1	12	12.288MHz

Table 8. Reference Frequency Select

Receive Closed Loop Bit (RXCL): DB2

This bit is used in Receive mode to put the PLL into either open loop or closed loop (see Table 9).

RXCL	RECEIVE PLL MODE
0	PLL open loop
1	PLL closed loop

Table 9. PLL Mode in Normal Receive Operation

PLL Frequency Shift Bit (LOL): DB3

LO shift for transmit and receive. For normal operations, it is recommended that LOL = 0 (see Table 10).

LOL	LO SHIFT FOR TRANSMIT	LO SHIFT FOR RECEIVE
0	0	+1.024MHz
1	+1.024MHz	0

Table 10. PLL Frequency Shift

Transmit Closed Loop Bit (TXCL): DB4

Used to produce a continuous CW transmitter output for product test with RXON low (see Table 11).

TXCL	TRANSMIT PLL MODE
0	PLL Open Loop, FSK Output
1	PLL Closed Loop, CW Output

Table 11. PLL Mode in Transmit Operation

REGISTER #1, CHANNEL FREQUENCY REGISTER

Channel Frequency Selection Bits (CHQ): <DB11:DB0>

These bits set the channel frequency for the transceiver (see Table 13). With a 6.144MHz or 12.288MHz input to the REF pin (pin 9), the channel frequency value is calculated by multiplying the CHQ value by 0.512. A 1.024MHz offset is automatically added in the RECEIVE mode to accommodate the IF frequency. The recommended operating range value of the CHQ is from 1,024 (400 hex) to 4093 (FFD hex). These bits should be programmed to a valid channel frequency before XCEN is asserted. The divide ratio is calculated as f_C /0.512, where f_C is the channel frequency in MHz.

B15	B14	B13 TO B2	B1	B0
0	0	PLL divide ratio	0	1

Table 13. Main Divider

REGISTER #2, FILTER TUNING SELECT TEST MODE

Analog Test Control Bits (ATM): <DB2:DB0>

The test mode selected is described in Table 14. The performance of the ML2723 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power-up) state of these bits is ATM<2:0> = <0,0,0>. When a non-zero value is written to the field, RSSI/TPI (pin 28) and AOUT/TPQ (pin 7) become an analog test access port, giving access to the outputs of key signal processing stages in the transceiver. During normal operation, the ATM field should be set to zero.

ATM2	ATM1	ATM0	RSSI/TPI	AOUT/TPQ
0	0	0	RSSI	AOUT
0	0	1	I No Connect	Q No Connect
0	1	0	I IF Buffer Output	Q IF Buffer Output
0	1	1	I IF Buffer Output	Q IF Buffer Output
1	0	0	I IF Buffer Output	Q IF Buffer Output
1	0	1	I Data Slicer Input	Q Data Slicer Input
1	1	0	I IF Limiter Outputs	Q IF Limiter Outputs
1	1	1	1.67V Ref.	VCO Mod. Voltage

Table 14. Analog Test Control Bits

Digital Test Control Bits (DTM): <DB2:DB0>

The DTM<2:0> bit functions are described in Table 15. The performance of the ML2723 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power-up) state of these bits is DTM<2:0> = <0,0,0>. When a non-zero value is written to these fields, DOUT (pin 32) becomes a digital test access port for key digital signals in the transceiver. During normal operation, the DTM field should be set to zero.

DTM2	DTM1	DTM0	DOUT
0	0	0	Demodulated data
0	0	1	Receiver AGC state
0	1	0	PLL Main Divider Output
0	1	1	PLL Reference Divider Output

Table 15. Digital Test Control Bits

TRANSMIT AND RECEIVE DATA INTERFACES

The DIN and DOUT CMOS logic levels are serial data that correspond to FSK modulated data on the radio channel. The ML2723 operates as an FSK transceiver in the 902 to 928MHz ISM band. The chip rate, bit rate and spreading code are controlled by the baseband processor, and the FM deviation and transmit filtering are controlled by the transceiver.

DIN provides data to the Transmit data filter, which band limits the transmitted chips or bits before they are FM modulated. There is no re-timing of the chips or bits, so the transmitted FSK chips or bits take their timing from DIN (pin 30). In the Receive chain, FM demodulation, data filtering, and data slicing take place in the ML2723 receiver, with chip, bit and word rate timing recovery performed in the baseband processor.

RSSI AND REF

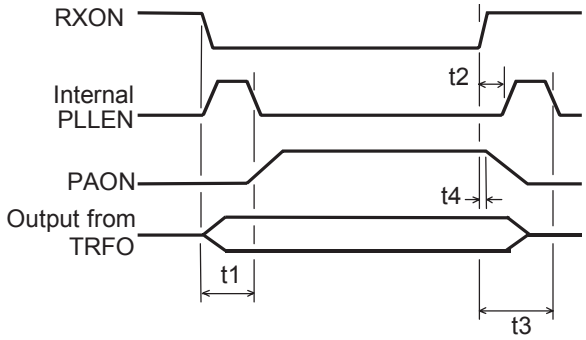
There are two other interface pins between the ML2723 transceiver and the baseband IC: the RSSI/TPI (pin 28) and REF (pin 9).

REF is the master reference frequency for the transceiver. It supplies the frequency reference for the RF channel frequency and the filter tuning. The REF pin is a CMOS input with internal biasing resistors. It can be AC coupled through a 470pF coupling capacitor to a sine wave source of at least 2.0V peak-to-peak. The PLL comparison and the IF filter center frequency are both equal to the REF input frequency divided by either 6 or 12, depending on the setting of the RDIV bit in the PLL configuration control word. The IF filter and data filter bandwidths track the IF filter center frequency.

The Received Signal Strength Indicator (RSSI) pin supplies a voltage indicating the amplitude of the received RF signal. It is normally connected to the input of a low-speed ADC on an external baseband IC, and is used during channel scanning to detect clear channels on which the radio may transmit. The RSSI voltage is proportional to the logarithm of the received power level. A voltage of 0V to 2.7V typically corresponds to an RF input power of –95 to –20dBm with a nominal slope of 35mV/dB.

CONTROL OUTPUTS TO THE PA – PAON

The ML2723 has one output pin to control and sequence the power amplifier – PAON (see Figure 6).



SYMBOL	PARAMETER	TIME/µS
t1	RXON falling edge to PAON rising edge	62.5
t2	RXON rising edge to PLL recalibration	6.5
t3	RXON rising edge to receive mode	70
t4	RXON rising edge to PAON falling edge	< 0.1

Figure 6. Power Amplifier Interface

The PAON (PA control) is a CMOS output to control an off-chip RF PA (power amplifier). It outputs a logic high when the PA should be enabled, and a logic low at all other times. This output is inhibited if the PLL fails to lock, or the power supply to the ML2723 falls below 2.6V. The PLL lock detect or low voltage signals are latched, so that the transmitter is inhibited for the entire transmit time slot. These latches are reset at the end of the transmit time slot, so that the ML2723 will transmit in the next time slot following a transient fault condition.

In analog test modes, RSSI/TPI (pin 28) and AOUT/TPQ (pin 7) become analog test access ports that allow the user to observe internal signals in the ML2723.

RF INTERFACES

The RRFI receive input (pin 21) and the TRFO transmit output (pin 23) are the only RF I/O pins. The RRFI pin requires a simple impedance matching network for best input noise figure, and the TRFO pin is matched to 50Ω by an AC coupling capacitor. The associated RF input and output ground pins must have direct connections to an RF ground plane, and the RF block supply pins must be well decoupled to the RF ground pins.

f	S_{11}	
GHZ	MAG	ANGLE
0.9	0.757	-83.0

RRFI S-PARAMETERS AT 3.3V, OPERATING TEMPERATURE 25°C

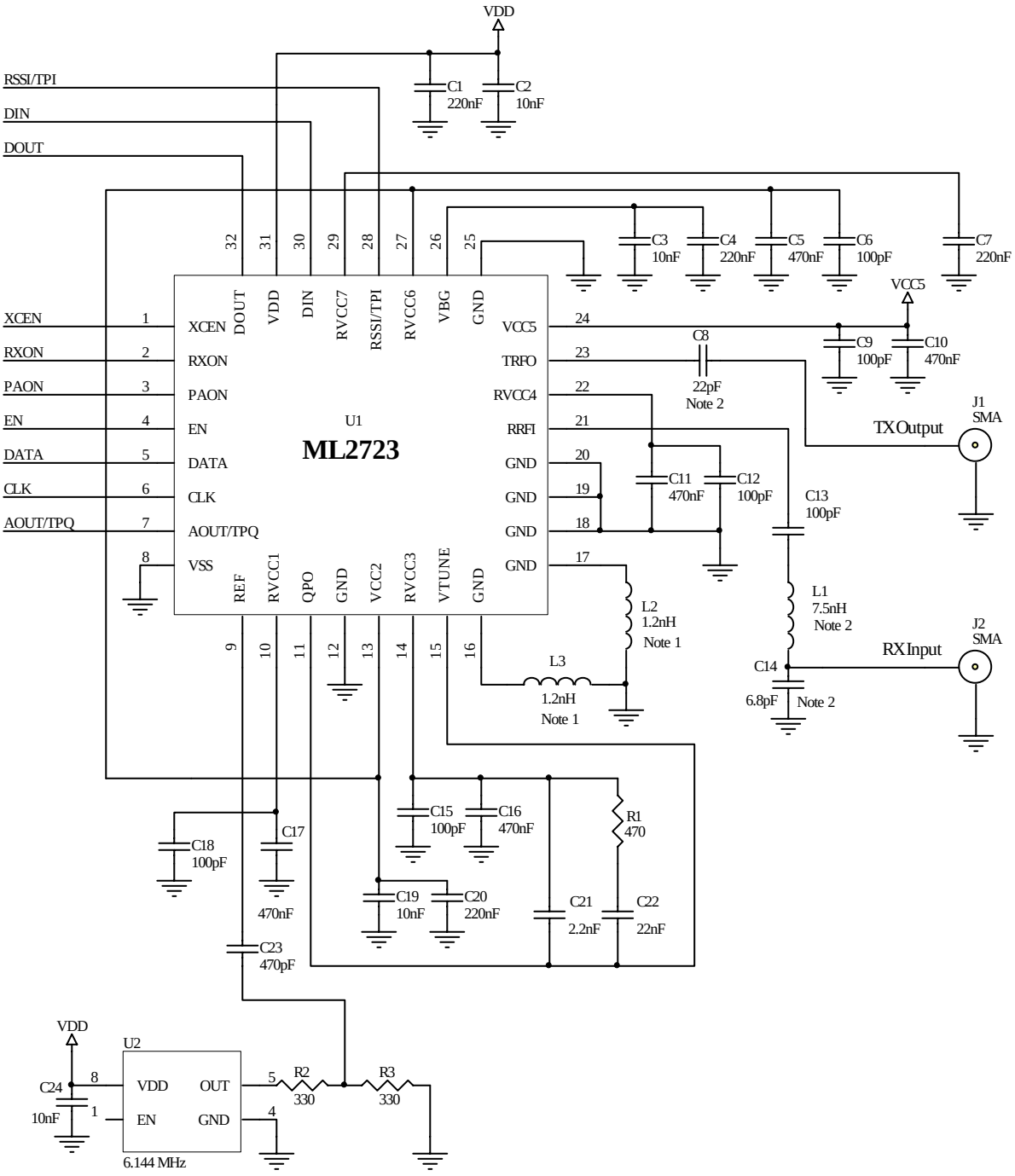
Table 16. Typical Receive RF Input

f	S_{11}	
GHZ	MAG	ANGLE
0.9	0.208	139.5

TRFO S-PARAMETERS AT 3.3V, OPERATING TEMPERATURE 25°C

Table 17. Typical Transmit RF Output

APPLICATION SCHEMATIC

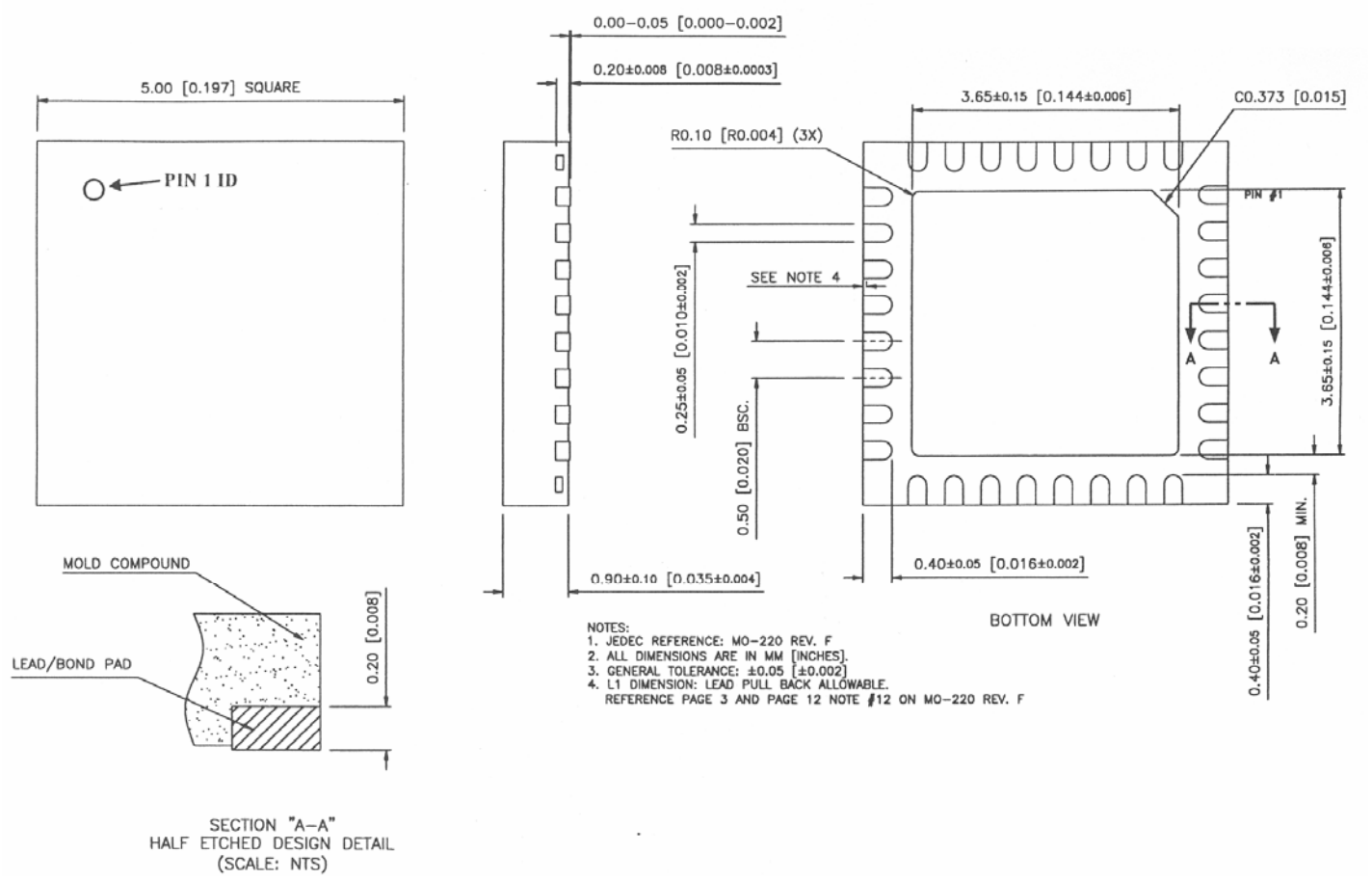


Note 1: RX frequency response and RX gain is dependant on L2 & L3. The Inductance values are dependant on Layout and PCB Material.

Note 2: Matching components L1, C8 & C14 values are dependant on layout and PCB material.

Figure 7. ML2723 Application Schematic

PHYSICAL DIMENSIONS (INCHES/MILLIMETERS)



Note: This package meets “Green” Pb-Free requirements and is compliant with the European Union directives WEEE (Waste Electrical and Electronic Equipment) and RoHS (Restriction of the use of certain Hazardous Substances in electrical and electronic equipment). The package pins are finished with 100% matte tin.

Figure 8. 32 LPCC Package Drawing

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

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