ML22420MB/ML22460MB

Speech Synthesis LSI with Serial ROM Interface Including 4-Channel Mixing Function

GENERAL DESCRIPTION

ML22420 and ML22460 are voice synthesis LSIs with serial interface to the external ROM that stores voice data.
These LSIs include edit ROM, ADPCM2 decoder, 16-bit DA converter, low pass filter and monaural speaker amplifier. Also, ML22420 supports the synchronous serial interface and ML22460 supports the I2C interface.
By integrating all the functions required for voice output into a single chip, these LSIs can be more easily incorporated in compact portable devices.

- Maximum External ROM capacity: 128Mbits
- External ROM capacity and maximum vocal reproduction time:

(at the case of 4-bit ADPCM2 algorithm)

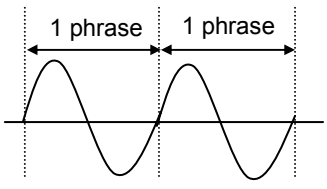
External ROM capacity	Maximum vocal reproduction time (sec)		
	F_S = 4.0 kHz	F_S = 8.0 kHz	F_S = 16 kHz
128 Mbits	8,352	4,176	2,088
64 Mbits	4,176	2,088	1,044
16 Mbits	1,044	522	261

- Voice synthesis method: 4-bit ADPCM2
  8-bit Nonlinear PCM
  8-bit PCM, 16-bit PCM
  Can be specified for each phrase.
- Sampling frequency(F_S): 4.0 / 5.3 / 6.4 / 8.0 / 10.6 / 12.0 / 12.8 / 16.0 / 21.3 / 24.0 / 25.6 / 32.0 / 48.0 kHz
  F_S can be specified for each phrase.
- Built-in low-pass filter and 16-bit DA converter
- Speaker driving amplifier: 0.7 W (when Z=8Ω , DV_{DD}=5 V, Ta=25°C)
  2ch analog inputs (internal: 1ch, external: 1ch)
- CPU command interface: 3-wired serial clock-synchronized (ML22420)
  I2C interface (ML22460)
- Maximum number of phrases: 1024 phrases from 000h to 3FFh
- Volume control: 32 levels (OFF is included) can be set by CVOL command.
  50 levels (OFF is included) can be set by AVOL command.
- Repeat function: LOOP commands
- 4-channel mixing function: Available when F_S for each channel is 16kHz or less
- Master clock frequency: 4.096 MHz
- Power supply voltage: 2.7 V to 5.5 V
- Operating temperature range: –40°C to +85°C
- Package: 30-pins plastic SSOP (SSOP30-P-56-0.65-K-MC)
- Product name: ML22420, ML22460

The following table shows the differences among the other speech synthesis LSIs.

Item	MSM9841	ML2240	ML22420/460
CPU interface	Parallel	Parallel/Serial	Serial/I2C
Voice memory	external	←	←
Memory interface	8/16-bits parallel	8-bits parallel	Serial
Voice synthesis algorithm	4-bit ADPCM2 8-bit nonlinear PCM 8-bit straight PCM 16-bit straight PCM	←	←
Maximum number of phrases	-	256	1024
Sampling frequency (kHz)	4.0/ 6.4/ 8.0/ 12.8/ 16.0/ 32.0	4.0/ 5.3/ 6.4/ 8.0/ 10.7/ 12.8/ 16.0	4.0/5.3/6.4/8.0/10.6/ 12.0/12.8/16.0/21.3/ 24.0/25.6/32.0/48.0
Clock frequency	4.096MHz (with a built-in crystal oscillator circuit)	←	←
D/A converter	14 bits	←	16 bits
Low-pass filter	2nd order comb. filter	FIR interpolation filter	←
Speaker driving amplifier	N.A.	N.A.	Built-in 0.7W (8Ω, DV_{DD} = 5 V)
Edit ROM function	Available	←	←
Simultaneous sound production function (mixing function)	Monaural	4-channels	←
Volume control	8 levels	29 levels	32 levels
Silence insertion	N.A.	20 ms to 1024 ms (4 ms step)	←
Repeat function	Available	←	←
Silent interval for seam during continuous playback (*1)	No (Seamless)	←	←
Power supply voltage	2.7 V to 5.5 V	←	←
Package	56-pins QFP	80-pins TQFP	30-pins SSOP

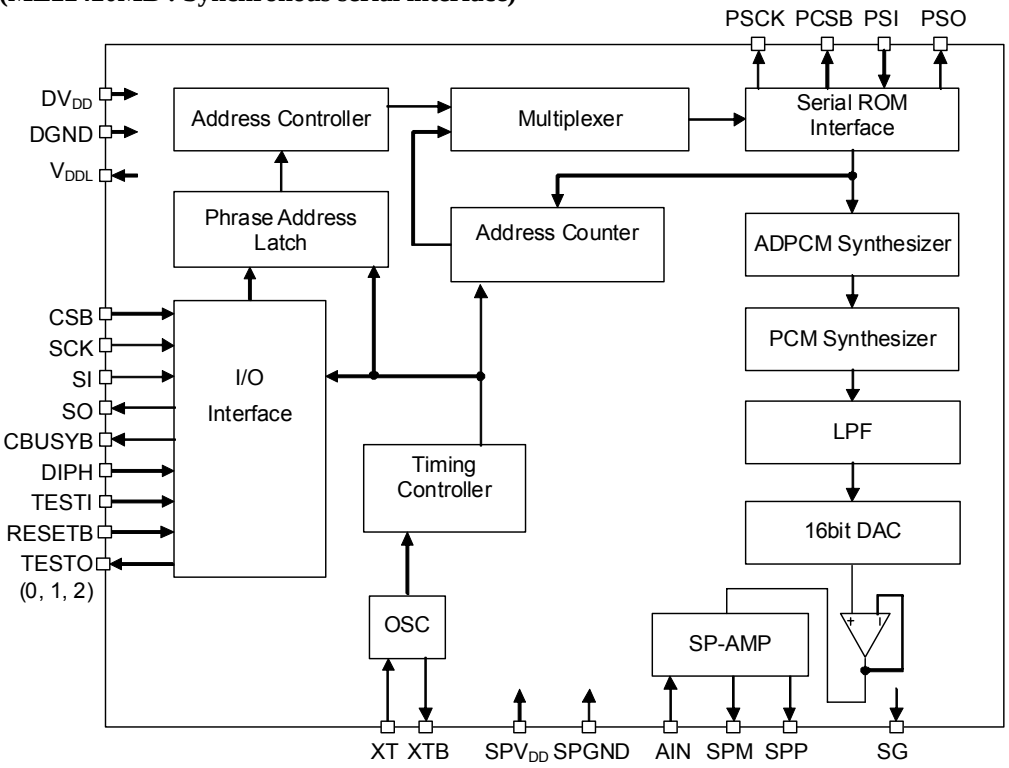
*1: Continuous playback as shown below is possible.



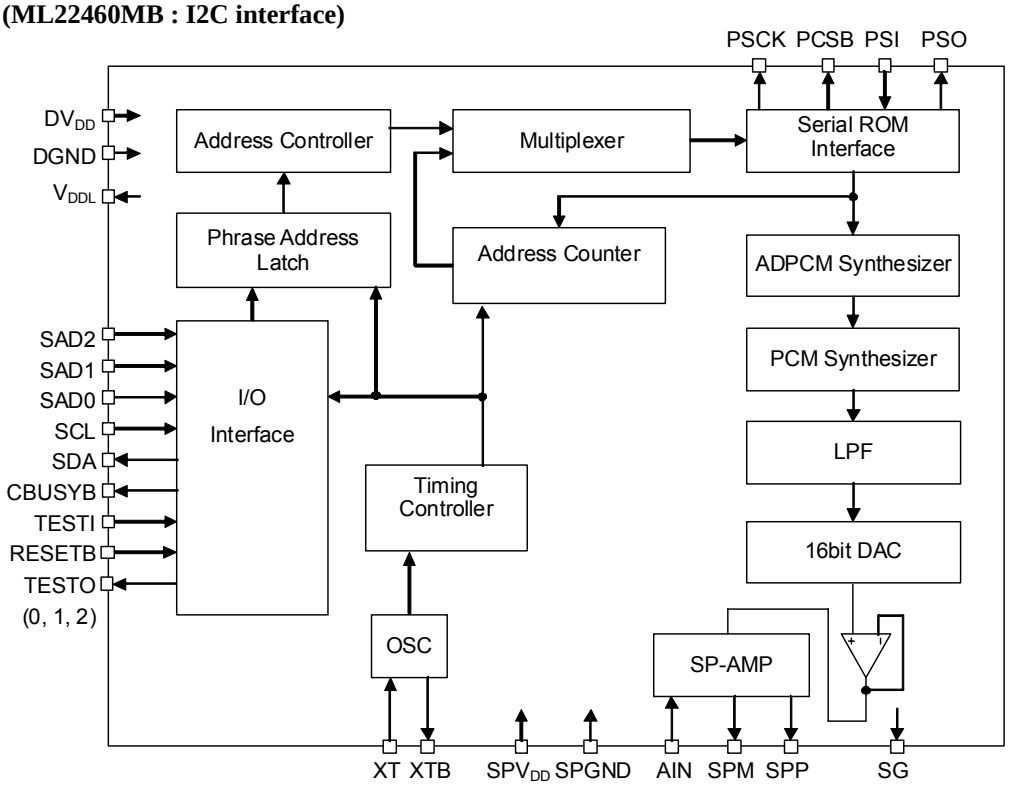
No silent interval

BLOCK DIAGRAMS

(ML22420MB : Synchronous serial interface)

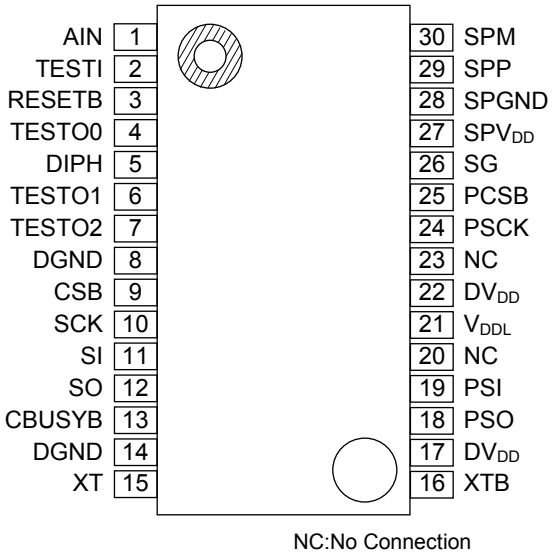


(ML22460MB : I2C interface)



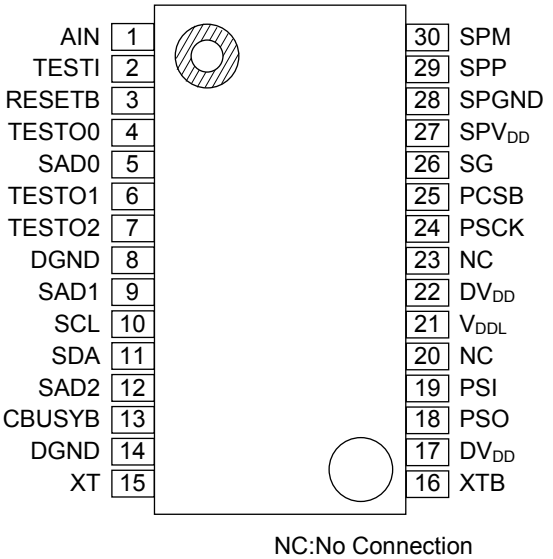
PIN CONFIGURATIONS (TOP VIEW)

(ML22420MB : Synchronous serial interface)



30-Pin Plastic SSOP

(ML22460MB : I2C interface)



30-Pin Plastic SSOP

PIN DESCRIPTION (COMMON TO ALL PRODUCTS)

Pin	Symbol	I/O	Initial value (*1)	Description
1	AIN	I	0	Input pin for speaker amplifier.
2	TESTI	I	0	Input pin for testing. Fix this pin to "L" level (DGND level). This pin has a pull-down resistor built in.
3	RESETB	I	0 (*2)	Input pin for reset. At the "L" level, the LSI enters initial state. During reset, the entire circuitry stops and enters power down state. Input "L" level when power is supplied. After the power supply voltage is stable, drive this pin to "H" level. Then the entire circuitry can be powered up. This pin has a pull-up resistor built in.
4,6,7	TESTO (0,1,2)	O	Hi-Z	Output pins for testing. Leave these pins open.
8,14	DGND	—	—	Ground pins for logic circuitry.
13	CBUSYB	O	1	Output pin for command processing status. This pin outputs "L" level during command processing. Any command should be entered when this pin is "H" level.
15	XT	I	0	Connect to the crystal or ceramic resonator. A feedback resistor around 1 MΩ is built in between this pin and the XTB pin. Use this pin if need to use an external clock. If the resonator is used, connect it as close to this pin as possible.
16	XTB	O	1	Connect to the crystal or ceramic resonator. When to use an external clock, leave this pin open. If the resonator is used, connect it as close to this pin as possible.
17, 22	DV_{DD}	—	—	Power supply pins for logic circuitry. Connect a capacitor of 0.1μF or more between these pins and DGND pins.
18	PSO	O	1	Serial data output pin for voice ROM interface.
19	PSI	I	Hi-Z	Serial data input pin for voice ROM interface.
20,23	N.C.			Non connected pins. Leave these pins open.
21	V_{DDL}	—	—	Regulator output pin for internal logic circuitry. Connect a capacitor recommended between this pin and DGND pin.
24	PSCK	O	1	Clock output pin for voice ROM interface.
25	PCSB	O	1	Chip select output pin for voice ROM interface. At the "L" level, ROM access is available.
26	SG	—	0	Reference voltage output pin for the speaker amplifier built-in. Connect a capacitor recommended between this pin and DGND pin.
27	SPV_{DD}	—	—	Power supply pin for the speaker amplifier. Connect a bypass capacitor of 0.1μF or more between this pin and SPGND pin.
28	SPGND	—	—	Ground pin for the speaker amplifier.
29	SPP	O	0	Positive(+) output pin of the speaker amplifier built-in. Serves as the LINE output (*3), if built-in speaker amplifier is not used.
30	SPM	O	Hi-Z	Negative(-) output pin of the speaker amplifier built-in.

*1: Indicate the initial value during reset input or power down.
*2: "H" during power down.
*3: Output a voice signal before amplified by the speaker amplifier built-in.

PIN DESCRIPTION (FOR ML22420 SYNCHRONOUS SERIAL INTERFACE)

Pin	Symbol	I/O	Initial value (*1)	Description
5	DIPH	I	0	Set pin of the SCK clock edge. When this pin is “L” level, rising edge is available for input(SI) and falling edge is available for output(SO). When this pin is “H” level, falling edge is available for input(SI) and rising edge is available for output(SO).
9	CSB	I	1	Chip select pin. At the “L” level, data input/output is available.
10	SCK	I	0	Synchronous clock input pin for serial interface.
11	SI	I	0	Input pin of synchronous serial data. When the DIPH pin is “L” level, data is shifted in at the rising edges of the SCK clock pulses. When the DIPH pin is “H” level, data is shifted in at the falling edges of the SCK clock pulses.
12	SO	O	Hi-Z	Output pin of synchronous serial data. When the DIPH pin is “L” level, data is output at the falling edges of the SCK clock pulses. When the DIPH pin is “H” level, data is output at the rising edges of the SCK clock pulses. When the CSB pin is “H” level, this pin is Hi-Z state.

*1: Indicate the initial value during reset or power down.

PIN DESCRIPTION (FOR ML22460 I2C INTERFACE)

Pin	Symbol	I/O	Initial value (*1)	Description
5, 9, 12	SAD0 SAD1 SAD2	I	0	Set pin of the slave address.
10	SCL	I	0	Clock input pin for I2C serial interface. This pin should be connected to pull-up resistor.
11	SDA	IO	0	Input/output pin for I2C serial data. Use for setting the mode of write/read and writing address, writing data or reading data. This pin should be connected to pull-up resistor. (N-ch MOS) open drain, when output mode. High impedance(Hi-Z), when input mode.

*1: Indicate the initial value during reset or power down.

ABSOLUTE MAXIMUM RATINGS

(DGND = SPGND = 0 V, Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	−0.3 to +7.0	V
Input voltage	V_{IN}	—	−0.3 to DV_{DD}+0.3	V
Power dissipation	P_D		938	mW
Output short-circuit current	I_{OS}	Applies to all pins except SPM, SPP and V_{DDL} pins.	10	mA
		Applies to SPM and SPP pins.	300	mA
		Applies to V_{DDL} pin.	50	mA
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = SPGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	2.7 to 5.5			V
Operating temperature	T_{OP}	—	−40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
External capacitors for crystal oscillator	Cd, Cg	—	15	30	45	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics (for the 3V applications)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.14×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD}–0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50 µA	DV_{DD}–0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
"L" output voltage 3 (*2)	V_{OL3}	I_{OL} = 3 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.3	2.0	15	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	2	30	200	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = GND	–15	–2.0	–0.3	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = GND	–200	–30	–2	µA
"H" output leak current 3 (*6)	I_{ILOH}	V_{OH} = DV_{DD}	—	—	10	µA
"L" output leak current 3 (*6)	I_{ILOL}	V_{OL} = GND	–10	—	—	µA
Supply current during playback	I_{DD}	f_{OSC} = 4.096 MHz No output load	—	—	20	mA
Power-down supply current	I_{DDS}	Ta = –40 to +40°C	—	1	10	µA
		Ta = –40 to +85°C	—	1	20	µA

*1: Applies to the XTB pin.
*2: Applies to the SCL and SDA pins.
*3: Applies to the XT pin.
*4: Applies to the TESTI pin.
*5: Applies to the RESETB pin.
*6: Applies to the TESTO(0, 1 and 2) pins.

DC Characteristics (for the 5V applications)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8×DV_{DD}	—	DV_{DD}	V
"L" input voltage	V_{IL}	—	0	—	0.2×DV_{DD}	V
"H" output voltage 1	V_{OH1}	I_{OH} = –1 mA	DV_{DD}–0.4	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	I_{OH} = –50µA	DV_{DD}–0.4	—	—	V
"L" output voltage 1	V_{OL1}	I_{OL} = 2 mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	I_{OL} = 50 µA	—	—	0.4	V
"L" output voltage 3 (*2)	V_{OL3}	I_{OL} = 3 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	µA
"H" input current 2 (*3)	I_{IH2}	V_{IH} = DV_{DD}	0.8	5.0	20	µA
"H" input current 3 (*4)	I_{IH3}	V_{IH} = DV_{DD}	20	100	400	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (*3)	I_{IL2}	V_{IL} = GND	–20	–5.0	–0.8	µA
"L" input current 3 (*5)	I_{IL3}	V_{IL} = GND	–400	–100	–20	µA
"L" output leak current 2 (*6)	I_{ILOH}	V_{OH} = DV_{DD}	—	—	10	µA
"L" output leak current 3 (*6)	I_{ILOL}	V_{OL} = GND	–10	—	—	µA
Supply current during playback	I_{DD}	f_{OSC} = 4.096 MHz No output load	—	—	25	mA
Power-down supply current	I_{DDS}	Ta = –20 to +40°C	—	1	15	µA
		Ta = –20 to +85°C	—	1	30	µA

*1: Applies to the XTB pin.
*2: Applies to the SCL and SDA pins.
*3: Applies to the XT pin.
*4: Applies to the TESTI pin.
*5: Applies to the RESETB pin.
*6: Applies to the TESTO(0, 1 and 2) pins.

Characteristics of Analog Circuitry (for the 3V applications)

DV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}		—	—	DV_{DD}×2/3	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	DV_{DD}/6	—	DV_{DD}×5/6	V
SG output voltage	V_{SG}	—	0.95×V_{DDL}/2	V_{DDL}/2	1.05×V_{DDL}/2	V
SG output resistance	R_{SG}	During power down	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 3.3V, f = 1kHz R_{SPO} = 8Ω, THD≥10%	100	300	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

Characteristics of Analog Circuitry (for the 5V applications)

DV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}		—	—	DV_{DD}×2/3	Vp-p
LINE output load resistance	R_{LA}	During 1/2 DV_{DD} output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	DV_{DD}/6	—	DV_{DD}×5/6	V
SG output voltage	V_{SG}	—	0.95×V_{DDL}/2	V_{DDL}/2	1.05×V_{DDL}/2	V
SG output resistance	R_{SG}	During power down	57	96	135	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	SPV_{DD} = 5.0V, f = 1kHz R_{SPO} = 8Ω, THD≥10% Ta=25°C	500	700	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

AC Characteristics (Common to All Products)

DV_{DD} = SPV_{DD} = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Applicable command	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle		f_{duty}	—	40	50	60	%
RESETB input pulse width		t_{RST}	—	100	—	—	μs
Reset noise rejection pulse width		t_{NRST}	—	—	—	0.1	μs
Command input interval time	STOP, SLOOP, CLOOP, CVOL, AVOL	t_{INT}	f_{OSC} = 4.096 MHz	2	—	—	ms
	PUP	t_{INTP}		10	—	—	ms
	RDSTAT (After status read)	t_{INTRD}		500	—	—	μs
Command input enable time	SLOOP Continuous play by PLAY/MUON	t_{cm}	f_{OSC} = 4.096 MHz	—	—	10	ms
CBUSYB “L” level output time	PUP	t_{PUP1}	f_{OSC} = 4.096 MHz	2.0	2.5	3.0	ms
	PDWN	t_{PD1}	f_{OSC} = 4.096 MHz	—	—	20	μs
	2nd byte of AMODE (POP = “0” DAEN and SPEN = “0” →”1”)	t_{POPA1}	f_{OSC} = 4.096 MHz	58	60	62	ms
	2nd byte of AMODE (POP = “1” DAEN = “0” →”1” SPEN = ”0”)	t_{POPA2}	f_{OSC} = 4.096 MHz	90	93	95	ms
	2nd byte of AMODE (POP = “0” DAEN and SPEN = “1” →”0”)	t_{PDA1}	f_{OSC} = 4.096 MHz	108	110	112	ms
	2nd byte of AMODE (POP = “1” DAEN = “1” →”0” SPEN = “0”)	t_{PDA2}	f_{OSC} = 4.096 MHz	140	142	144	ms
	(*1)	t_{CB1}	f_{OSC} = 4.096 MHz	—	—	2	ms
<Serial ROM interface timing>							
PSCK input enable time from PCSB fall edge		t_{PCSS}	f_{OSC} = 4.096 MHz	180	—	—	ns
PSCK input hold time from PCSB rise edge		t_{PCSH}	f_{OSC} = 4.096 MHz	180	—	—	ns
Data setup time from PSCK rise edge		t_{PDIS}	f_{OSC} = 4.096 MHz	180	—	—	ns
Data hold time from PSCK rise edge		t_{PDIH}	f_{OSC} = 4.096 MHz	26	—	—	ns
Data output delay time from PSCK rise edge		t_{PDOD}	f_{OSC} = 4.096 MHz	—	—	5	ns
PSCK “H” level pulse width		t_{PSCKH}	f_{OSC} = 4.096 MHz	40	—	—	ns
PSCK “L” level pulse width		t_{PSCKL}	f_{OSC} = 4.096 MHz	40	—	—	ns

Note: Output pin load capacitance = 45 pF

*1: Applies to the case that a command is input except after a PUP, PDWN, or 2nd byte of AMODE command input.

AC Characteristics of Synchronous Serial Command Interface (Applied to ML22420)

DV_{DD} = SPV_{DD} = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Applicable command	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input enable time from CSB fall edge		t_{ESCK}	—	100	—	—	ns
SCK hold time from CSB rise edge		t_{CSH}	—	100	—	—	ns
Data floating time from CSB rise edge		t_{DOZ}	R_L = 3 kΩ	—	—	100	ns
Data setup time from SCK rise edge		t_{DIS1}	DIPH = “0”	50	—	—	ns
Data hold time from SCK rise edge		t_{DIH1}	DIPH = “0”	50	—	—	ns
Data output delay time from SCK rise edge		t_{DOD1}	R_L = 3 kΩ	—	—	80	ns
Data setup time from SCK fall edge		t_{DIS2}	DIPH = “1”	50	—	—	ns
Data hold time from SCK fall edge		t_{DIH2}	DIPH = “1”	50	—	—	ns
Data output delay time from SCK rise edge		t_{DOD2}	R_L = 3 kΩ	—	—	80	ns
SCK “H” level pulse width		t_{SCKH}	—	100	—	—	ns
SCK “L” level pulse width		t_{SCKL}	—	100	—	—	ns
CBUSYB output delay time from SCK rise edge		t_{DBSY1}	DIPH = “0”	—	—	150	ns
CBUSYB output delay time from SCK fall edge		t_{DBSY2}	DIPH = “1”	—	—	150	ns

Note: Output pin load capacitance = 45 pF

AC Characteristics of I2C Command Interface (Applied to ML22460)

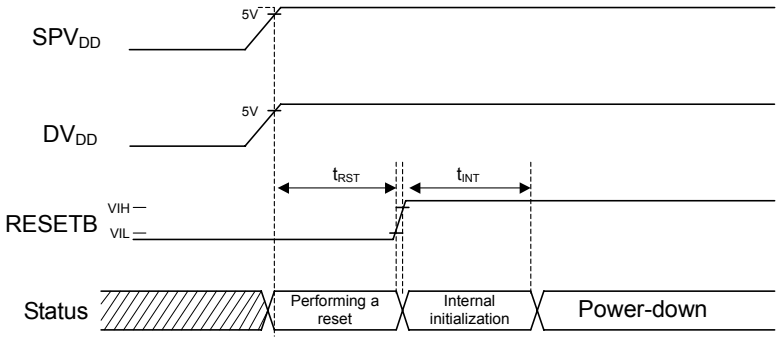
DV_{DD} = SPV_{DD} = 2.7 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	(High-speed mode)		Unit
		Min.	Max.	
SCL clock frequency.	t_{SCL}	0	400	kHz
Hold time for (repeated) START condition After this period, the first clock pulse is generated.	$t_{HD;STA}$	0.6	—	μs
SCL “L” level pulse width	t_{LOW}	1.3	—	μs
SCL “H” level pulse width	t_{HIGH}	0.6	—	μs
Setup time for repeated START condition	$t_{SU;STA}$	0.6	—	μs
Data hold time for I2C bus devices	$t_{HD;DAT}$	0	0.9	μs
Data setup time	$t_{SU;DAT}$	100	—	ns
SDA and SCL signal rise time	t_r	20	300	ns
SDA and SCL signal fall time	t_f	20	300	ns
Setup time for STOP condition	$t_{SU;STO}$	0.6	—	μs
Bus free time between STOP condition and START condition	t_{BUF}	1.3	—	μs
Capacitive load for each bus line	C_b	—	400	PF
Noise margin at the “L” level in each device connected (including hysteresis)	V_{nL}	0.1× DV_{DD}	—	V
Noise margin at the “H” level in each device connected (including hysteresis)	V_{nH}	0.1× DV_{DD}	—	V

Note: Output pin load capacitance = 45 pF

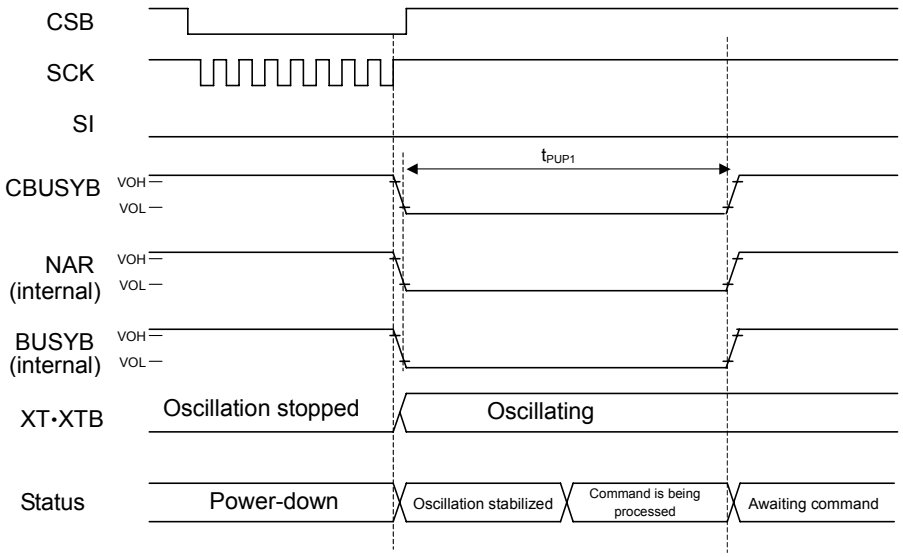
TIMING DIAGRAMS

Power-On Timing

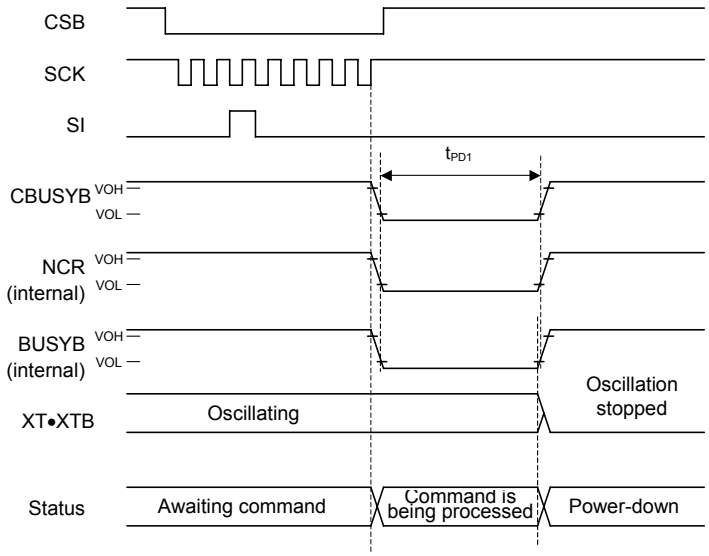


Oscillation is stopped after power-on.

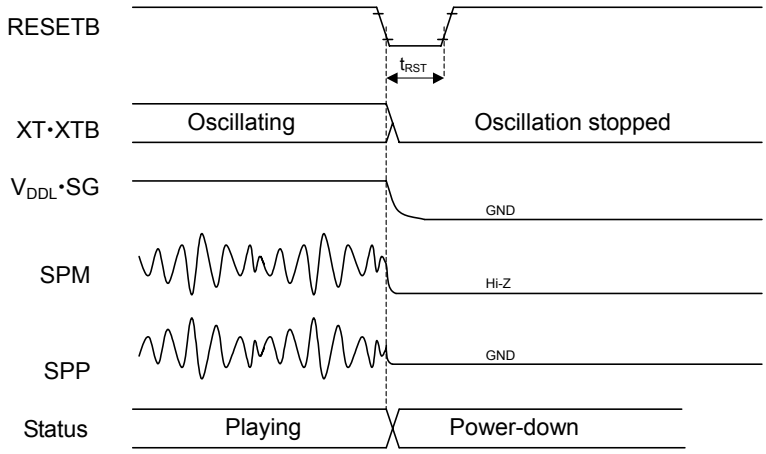
Power-Up Timing



Power-Down Timing (At the PDWN command Input)

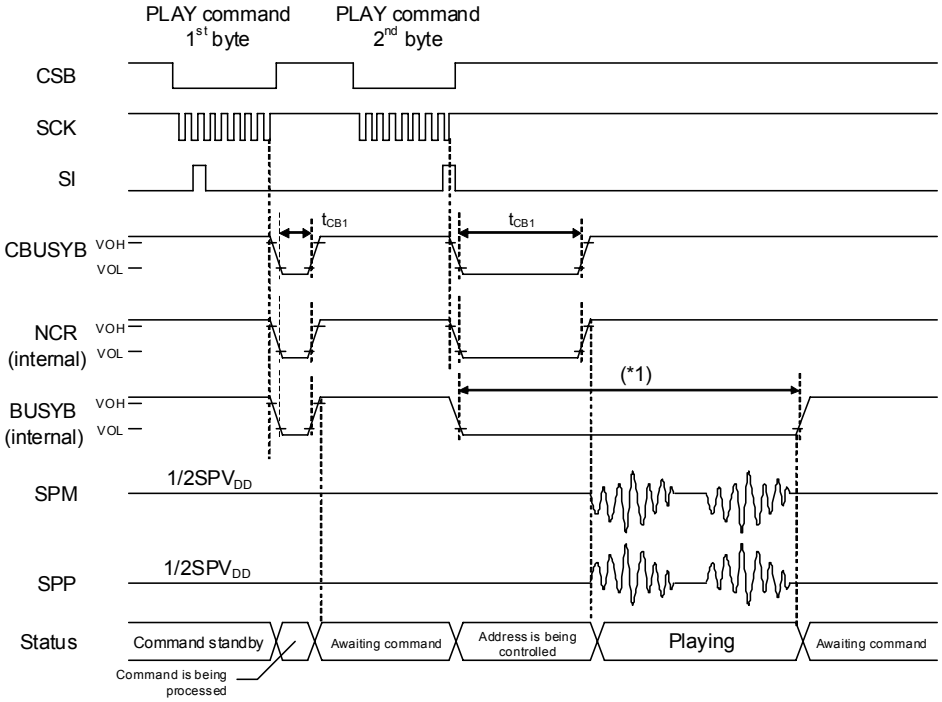


Power-Down Timing (At the RESETB Input)



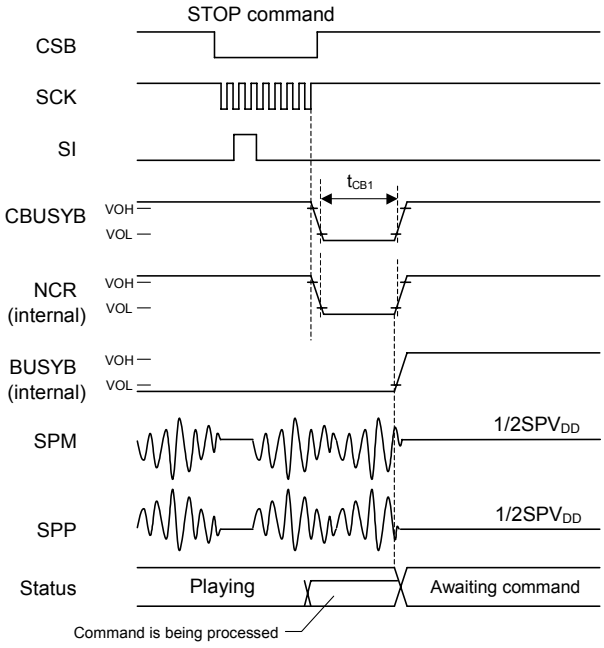
Note: The same timing is applied in the case that the RESETB signal is input during command waiting.

Playback Start Timing by the PLAY Command

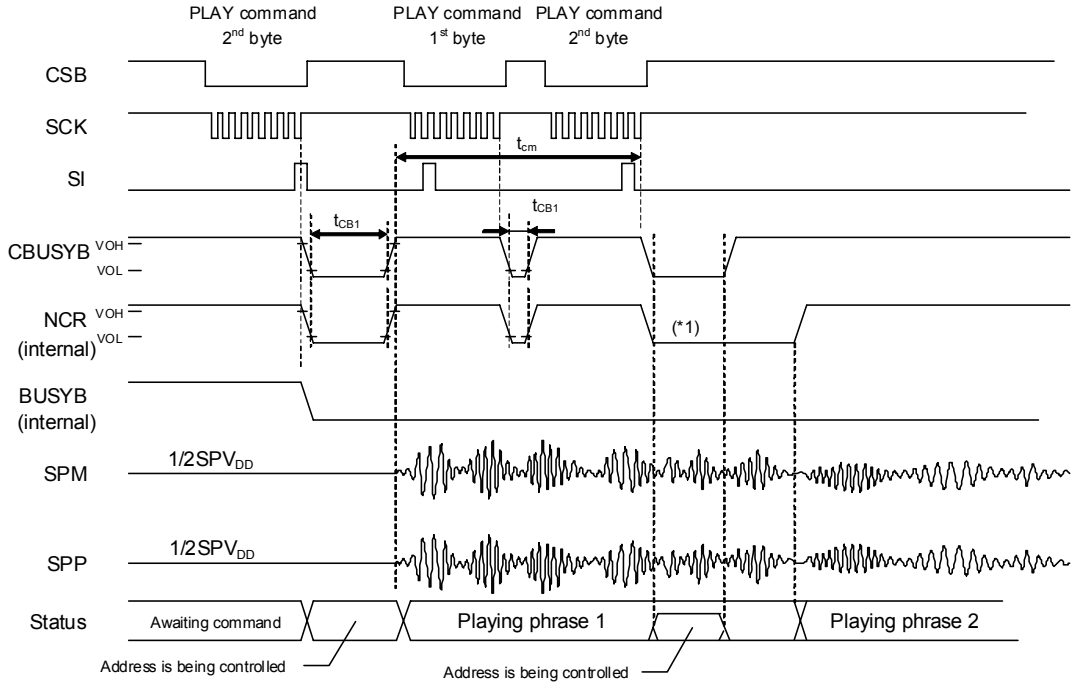


Note: The time length of "L" level of BUSYB is t_{CB1} + voice reproduction time.

Playback Stop Timing

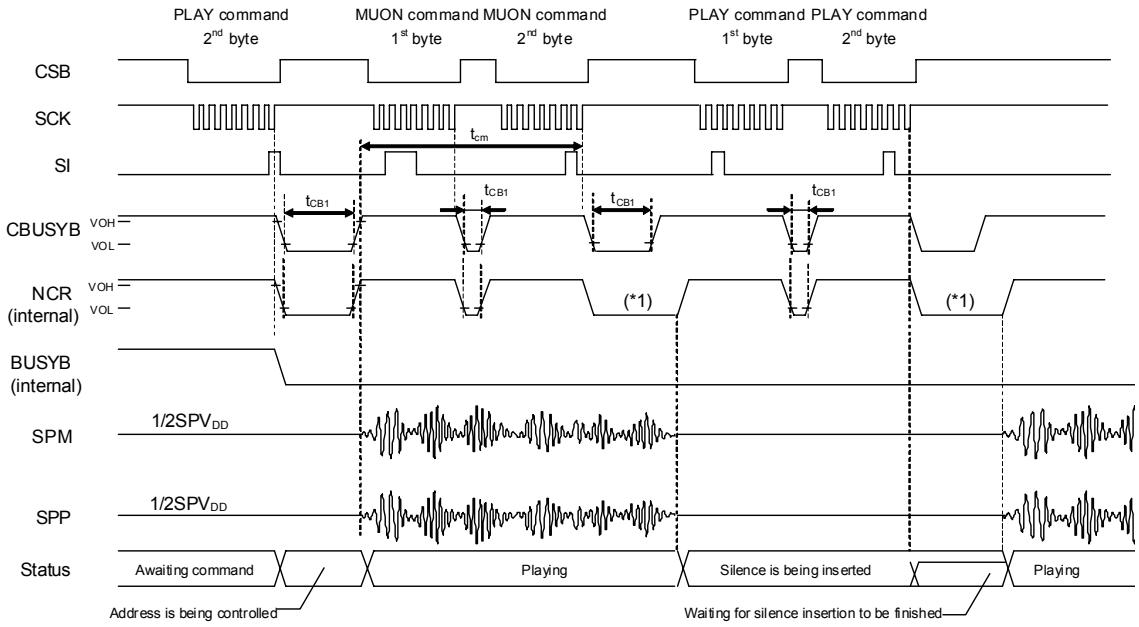


Continuous Playback Timing by the PLAY Command



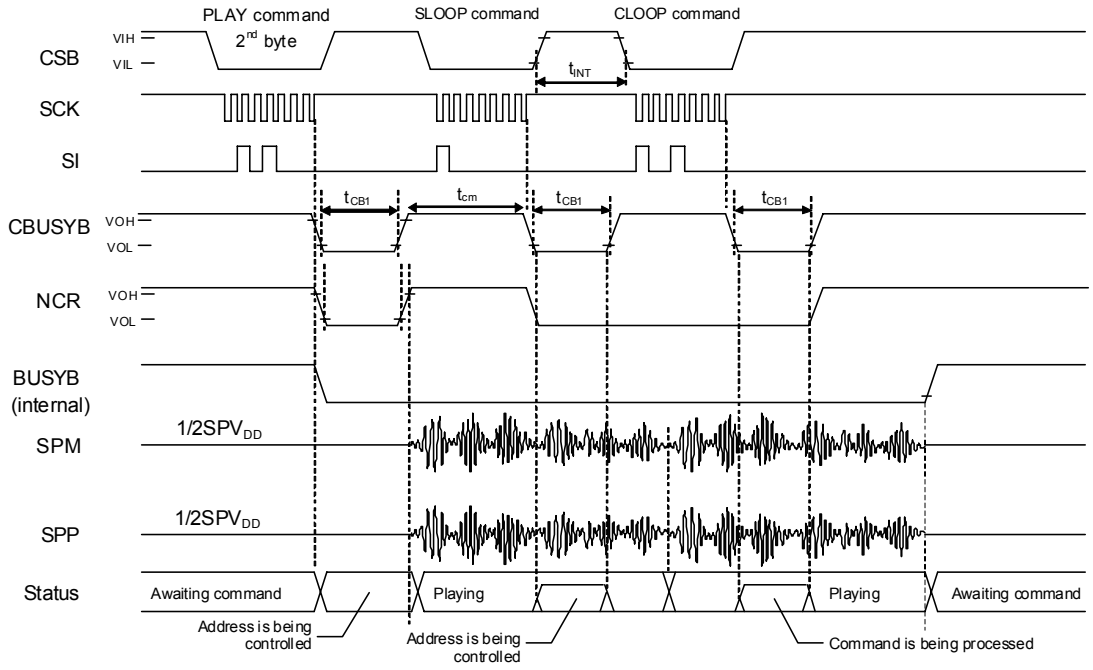
*1: The time length of "L" level of the NCR signal during playback varies depending on the input timing of command.

Silence Insertion Timing by the MUON Command

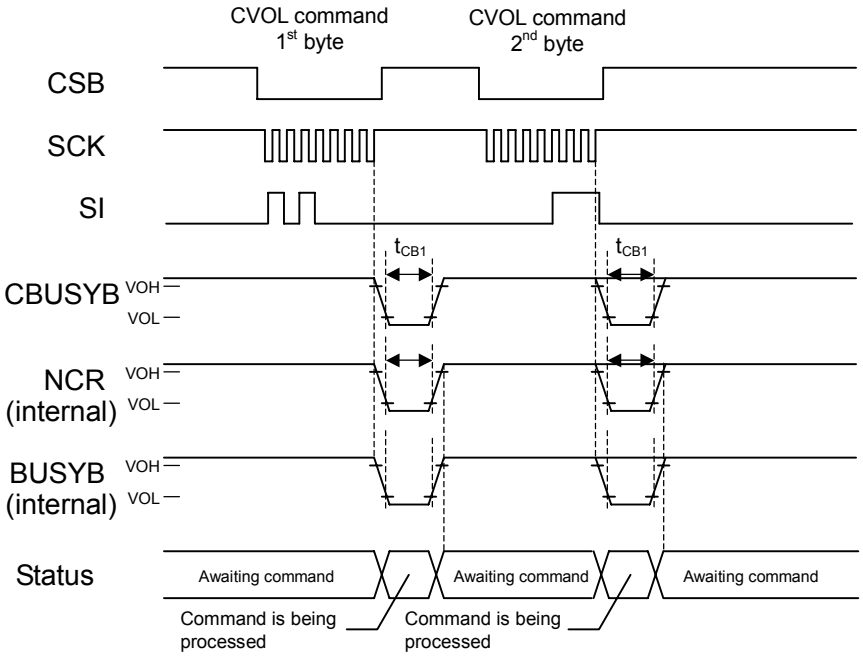


*1: The time length of "L" level of the NCR signal during playback or silence insertion varies depending on the input timing of command.

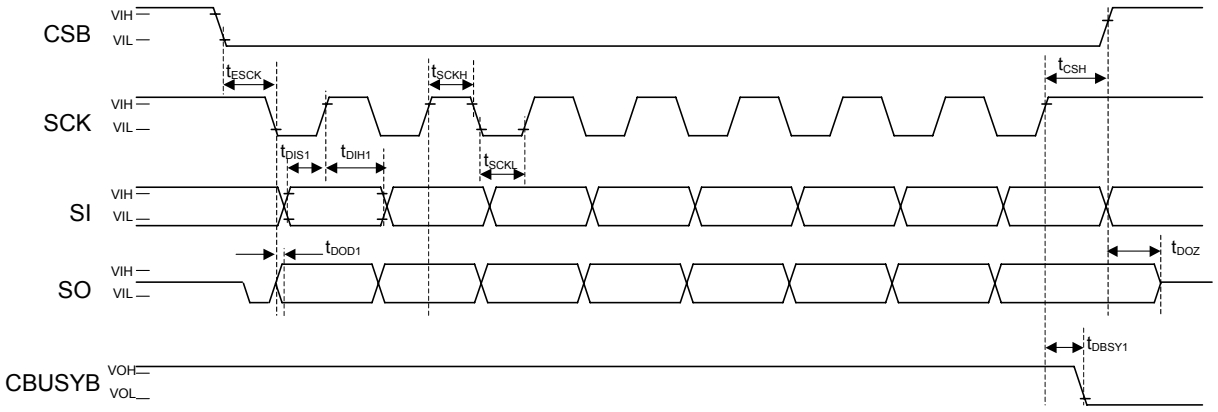
Repeat Playback Set/Release Timing by the SLOOP and CLOOP Commands



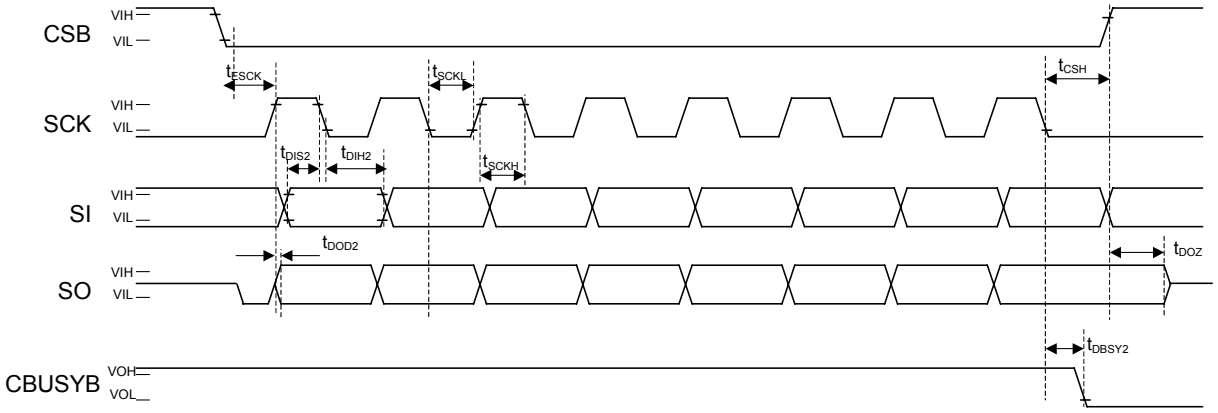
Timing of Volume Change by the CVOL Command



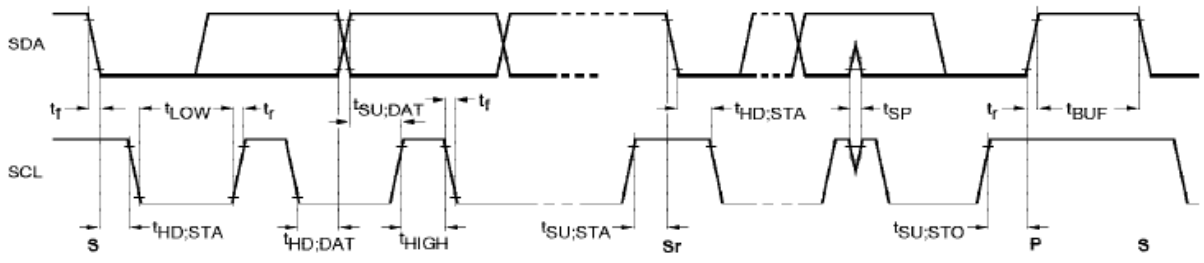
Serial Command Interface Timing (Applied to ML22420)
when DIPH pin is "L" level (: Rise edge for input, fall edge for output)



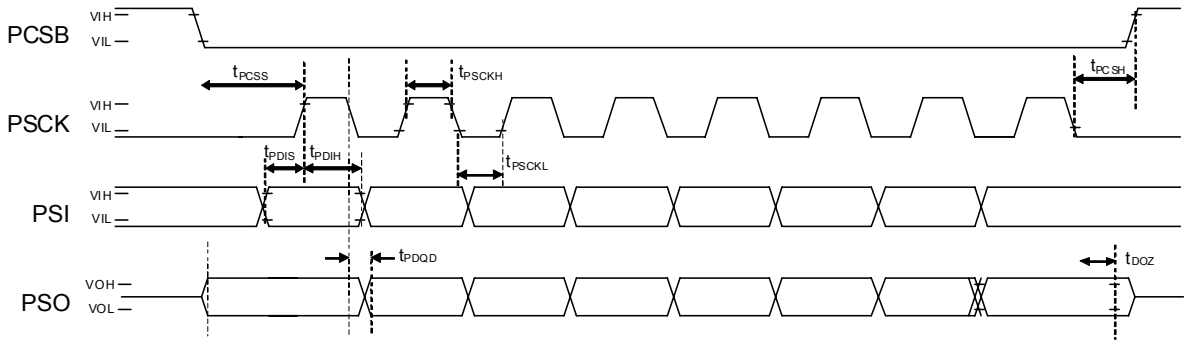
Serial Command Interface Timing (Applied to ML22420)
when DIPH pin is "H" level (: Fall edge for input, rise edge for output)



I2C Command Interface Timing (Applied to ML22460)



Serial ROM Interface Timing (Applied to both ML22420 and ML22460)



FUNCTIONAL DESCRIPTION

Synchronous Serial Command Interface (Applied to ML22420)

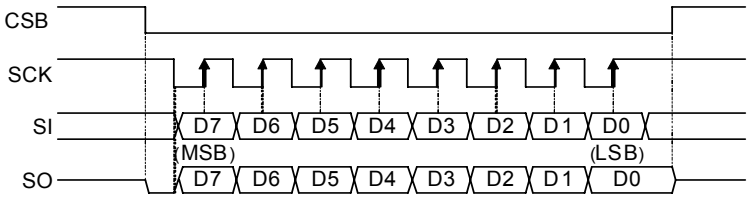
The CSB, SCK, SI, and SO pins are used to input the command data or to read the status. Driving the CSB pin to "L" level enables the serial CPU interface.
After the CSB pin is driven to "L" level, the command data are input through the SI pin from the MSB synchronized with the SCK clock. The command data shifts in through the SI pin at the rising or falling edge of the SCK clock pulse. Then, a command is executed at the rising or falling edge of the eighth pulse of the SCK clock.
As for status reading, status is output from the SO pin, synchronized with the SCK clock after the CSB pin is driven to "L" level.
The SCK clock edge is specified by the input level of the DIPH pin.

- When the DIPH pin is "L" level, rising edge is available for input from SI pin and falling edge is available for output from SO pin.
- When the DIPH pin is "H" level, falling edge is available for input from SI pin and rising edge is available for output from SO pin.

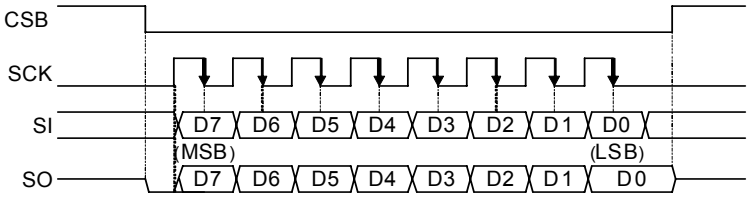
It is possible to input command data, even if the CSB pin is fixed by "L" level. However, if unexpected pulses caused by noise are induced through the SCK pin, SCK clock pulses are incorrectly counted, causing a failure in normal recognition of command. Then it is recommended that the CSB pin is "L" level only for command input.
The count of the SCK clock pulse is initialized when the CSB pin goes to "H" level.

Command Data Input or Status Read Timing

• When DIPH pin is "L" level



• When DIPH pin is "H" level



The following table shows the contents of each data output at a status read.

bit	Output status signal
MSB	Channel 4 BUSYB output (BUSYB3)
7SB	Channel 3 BUSYB output (BUSYB2)
6SB	Channel 2 BUSYB output (BUSYB1)
5SB	Channel 1 BUSYB output (BUSYB0)
4SB	Channel 4 NCR output (NCR3)
3SB	Channel 3 NCR output (NCR2)
2SB	Channel 2 NCR output (NCR1)
LSB	Channel 1 NCR output (NCR0)

The BUSYB output is “L” level when a command is being processed or the playback of a particular channel is going on. In other states, the BUSYB output is “H” level. The NCR output is “L” level when a command is being processed or particular channel is in standby for playback. In other states, the NCR output is “H” level.

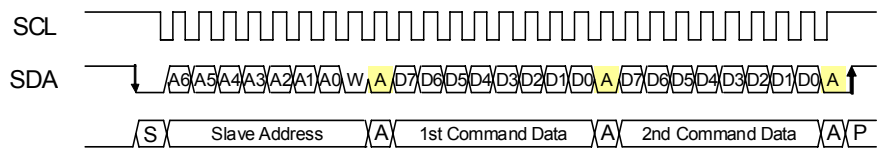
I2C Command Interface (Applied to ML22460)

The I2C Interface built-in is an serial interface (: slave side) that is compliant with I2C bus specification. It supports Fast mode and enables data transmission/reception at 400 kbps. The SCL and SDA pins are used to input the command data or to read the status. Pins (:SAD0, 1 and 2) are used to set the slave address.
Pull-up resister should be connected to SCL pin and SDA pin.
For the master on the I2C bus to communicate with this device (: slave), input the slave address with the first seven bits after setting the start condition. The upper three bits of the slave address can be set using the SAD0 to 2 pins. The eighth bit of slave address is used to set the direction (: write or read) of communication. If the eighth bit is "0" level, it is write mode from master to slave. And, if the eighth bit is "1" level, it is read mode from master.
The communication is made in the unit of byte. And acknowledge is needed for each byte.

The protocol of I2C communication is shown below.

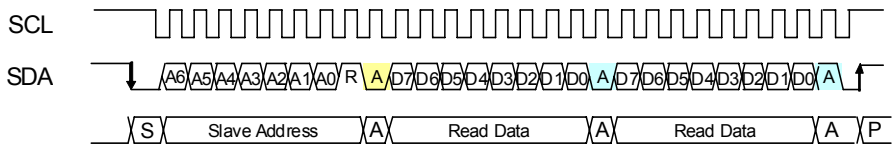
– Command flow at the data write
  Start condition
  Slave address +W(0)
  Write address (ex. 1st byte of the command)
  Write data (ex. 2nd byte of the command)
  STOP condition

• Data write timing



– Command flow at the data read
  Start condition
  Slave address +R(1)
  Read data (ex. Status read)
  STOP condition

• Data read timing



Setting of the slave address using the SAD0 to 2 pins

SAD2	SAD1	SAD0	Lower 4 bits
0	0	0	0101
0	0	1	0101
0	1	0	0101
0	1	1	0101
1	0	0	0101
1	0	1	0101
1	1	0	0101
1	1	1	0101

The following table shows the contents of each data output at the status read. Status is updated by the RDSTAT command, therefore, be sure to input the RDSTAT command in order to read status.

bit	Output status signal
MSB	Channel 4 BUSYB output (BUSYB3)
7SB	Channel 3 BUSYB output (BUSYB2)
6SB	Channel 2 BUSYB output (BUSYB1)
5SB	Channel 1 BUSYB output (BUSYB0)
4SB	Channel 4 NCR output (NCR3)
3SB	Channel 3 NCR output (NCR2)
2SB	Channel 2 NCR output (NCR1)
LSB	Channel 1 NCR output (NCR0)

The BUSYB signal is “L” level when either a command is being processed or the playback of a particular channel is going on. In other states, the BUSYB signal is “H” level. The NCR signal is “L” level when either a command is being processed or a particular channel is in standby for playback. In other states, the NCR signal is “H” level.

Command List

Each command is configured by the unit of byte (:8-bits). The following commands, AMODE, AVOL, FADR, PLAY, MUON and CVOL, use two bytes.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP	0	0	0	0	0	0	0	0	Power-up command. shift from the power down state to the command waiting state
PDWN	0	0	1	0	0	0	0	0	Power-down command. shift from the command waiting state to the power down state
RDSTAT	1	0	1	1	0	0	0	0	Status read command. Read the command status of each channel.
AMODE	0	0	0	0	0	1	0	0	Control command of analog circuitry. Set operation of power-up/dpwn and input/output.
	FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	POP	
PLAY	0	1	0	0	F9	F8	C1	C0	Playback start command. Set phrase address using F9 to F0 bits for each channel. Set channel using C1 and C0 bits.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	CH3	CH2	CH1	CH0	Playback stop command. Can be set for each channel.
FADR	0	0	1	1	F9	F8	C1	C0	Set command of playback phrase. Can be set for each channel. Use START command to start.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	CH3	CH2	CH1	CH0	Playback start command without phrase spec. Use FADR command to set phrase. Can start playback on multiple channels simultaneously. After played back by PLAY command, the same phrase can be played back with this command.
MUON	0	1	1	1	CH3	CH2	CH1	CH0	Silence insertion command. Set the silent time length for each channel using M7 to M0 bits in the 2nd byte.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	CH3	CH2	CH1	CH0	Set command of repeat playback. Setting is enabled during playback. Can be specified for each channel.
CLOOP	1	0	0	1	CH3	CH2	CH1	CH0	Stop command of repeat playback. Can be specified for each channel. Also, repeat playback is released by STOP command automatically.
CVOL	1	0	1	0	CH3	CH2	CH1	CH0	Volume control command. Set volume for each channel using CV4 to CV0 bits in the 2nd byte.
	0	0	0	CV4	CV3	CV2	CV1	CV0	
AVOL	0	0	0	0	1	0	0	0	Analog volume control command. Set volume after channel mixing using AV5 to AV0 bits.
	0	0	AV5	AV4	AV3	AV2	AV1	AV0	

Voice Synthesis Algorithm

Four types of voice synthesis algorithm are supported. They are 4-bit ADPCM2, 8-bit non-linear PCM, 8-bit straight PCM and 16-bit straight PCM. Select the best one according to the characteristics of playback voice.

The following table shows key features of each algorithm.

Voice synthesis algorithm	Applied waveform	Feature
4-bit ADPCM2	Normal voice waveform	Up version of LAPIS Semiconductor's specific voice synthesis algorithm (: 4-bit ADPCM). Voice quality is improved.
8-bit Nonlinear PCM	Waveform including high frequency signals (sound effect, etc.)	Algorithm which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit straight PCM		Normal 8-bit PCM algorithm.
16-bit straight PCM		Normal 16-bit PCM algorithm,

Memory Allocation and Creating Voice Data

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.
The voice control area manages the voice data in the ROM. It contains data for controlling the start/stop addresses of voice data for 1,024 phrases, use/non-use of the edit ROM function and so on.
The test area contains data for testing.
The voice area contains actual waveform data.
The edit ROM area contains data for effective use of voice data. For the details, refer to the section of "Edit ROM Function."
The edit ROM area is not available if the edit ROM is not used.

The ROM data is created using a dedicated tool.

Configuration of ROM data

0x00000 0x01FFF	Voice control area (Fixed 64 Kbits)
0x02000 0x0205F	Test area
0x02060 max: 0xFFFFFF	Voice area
max: 0xFFFFFF	Edit ROM area Depends on creation of ROM data.

Playback Time and Memory Capacity

The playback time depends on the memory capacity, sampling frequency, and playback method.
The equation to know the playback time is shown below. But this is not applied if the edit ROM function is used.

$$\text{Playback time [sec]} = \frac{\text{(Memory capacity – 64) [Kbit] x 1.024}}{\text{Sampling frequency [kHz]} \times \text{Bit length}}$$

(Bit length is 4 at the 4-bit ADPCM2 and 8/16 at the PCM.)

Example) In the case that the sampling frequency is 16 kHz, algorithm is 4-bit ADPCM2 and ROM capacity is 16 Mbits, the playback time is approx. 261 seconds, as shown below.

$$\text{Playback time} = \frac{(16{,}000 \times 1.024 - 64) \times 1.024}{16 \times 4} \cong 261 \text{ [sec]}$$

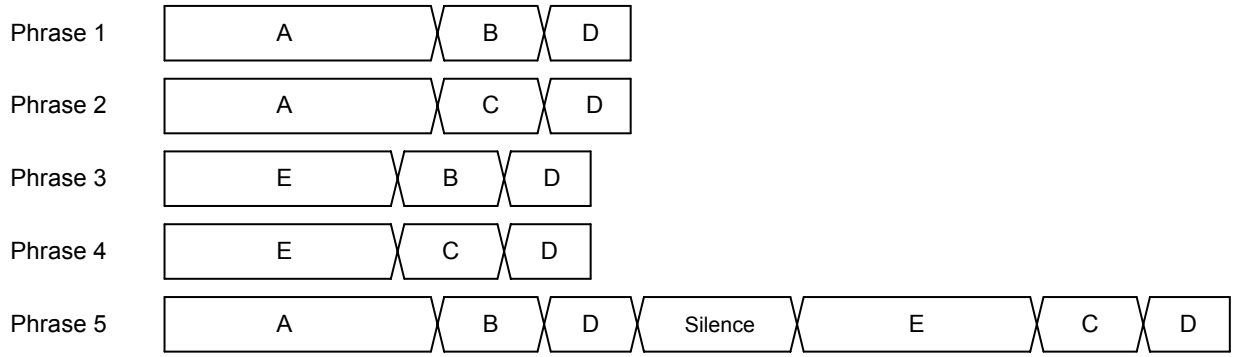
Edit ROM Function

The edit ROM function makes it possible to play back multiple phrases in succession. The following functions are set using the edit ROM function:

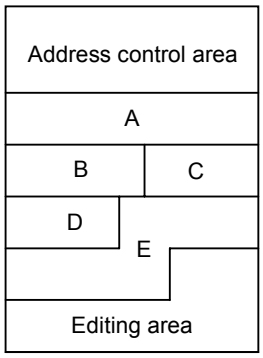
- Continuous playback: There is no limit to set the number of times of continuous playback. It depends on the memory capacity only.
- Silence insertion: 20ms to 1,024 ms

It is possible to use voice ROM effectively to use the edit ROM function.
Below is an example of the ROM structure, case of using the edit ROM function.

Example 1) Phrases using the Edit ROM Function



Example 2) Structure of the ROM that contents of example 1 are stored



Mixing Function

It is possible to perform mixing of four channels simultaneously. And also, it is possible to specify PLAY, STOP, and CVOL commands for each channel respectively. The mixing function is available if the sampling frequency (F_S) is 16 kHz or less.

- Precautions for Waveform Clamp
Adjust the volume of each channel using the CVOL command, if the waveform clamp is increased by channel mixing.

Description of Command Functions

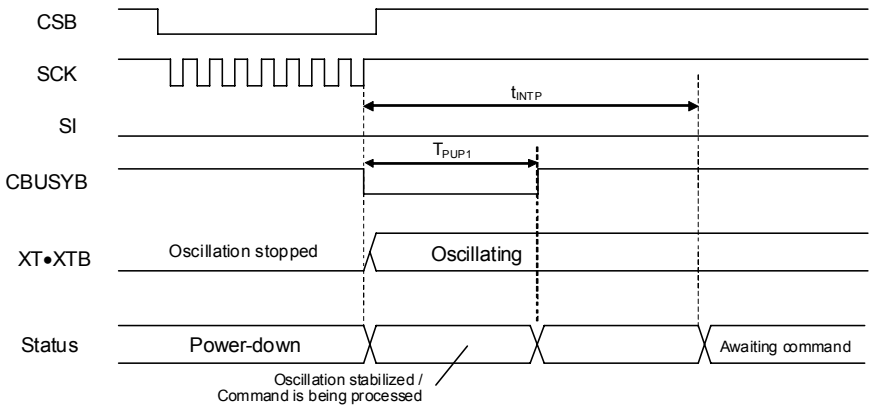
1. PUP command

・command	0	0	0	0	0	0	0	0

The PUP command is used to shift from the power down state to the command waiting state.
This command is only available at the power down state .
Conditions are as follows to enter the power down state.

1) When the power is turned on.
2) When the RESETB input is “L” level (: rest input).
3) When the CBUSYB pin goes to “H” level after inputting the power down command(:PDWN).

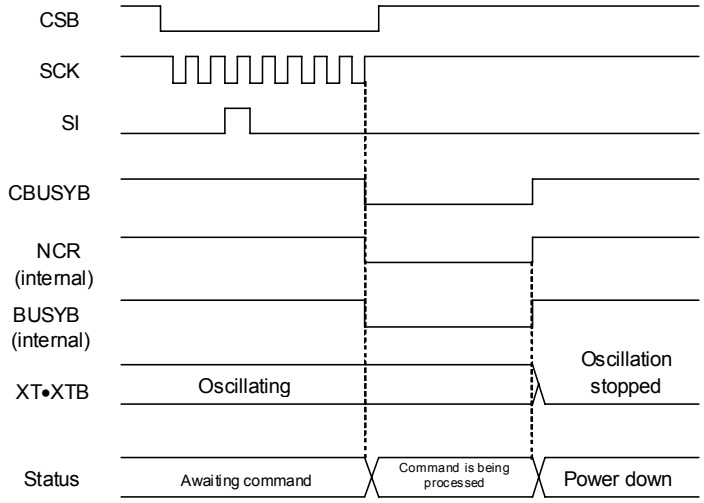
The built-in amplifier is not powered up by this command. It is powered up by the AMODE command.



2. PDWN command

・command	0	0	1	0	0	0	0	0

The PDWN command is used to shift from the command waiting state (: both NCR and BUSYB are “H” level) to the power down state.
Any setting is initialized by this command, so it is necessary to set again after power up.
This command is not available during playback.
To resume playback after entering power down state, input the AMODE and PLAY commands after input the PUP command.



The speaker amplifier stops operation after a lapse of command processing time after the PDWN command is input. At this time, the SPM output of the speaker amplifier goes to “Hi-Z” state to prevent troubles by pop noise .

The status of each output pin is as follows after this command is input or reset pin (:RESETB) is “L” level.

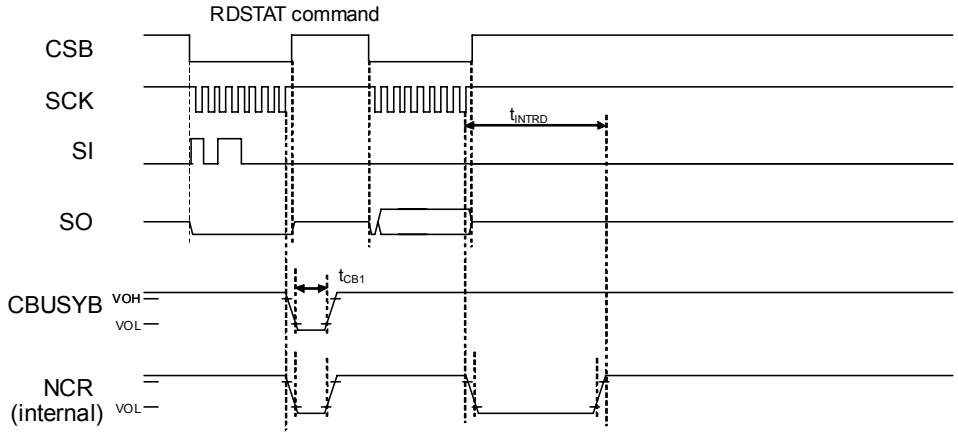
Analog output pin	State
V_{DDL}	GND
SG	GND
SPM	Hi-Z
SPP	GND

3. RDSTAT command

・command	1	0	1	1	0	0	0	0

The RDSTAT command is used to read the NCR and BUSYB signals that indicate the status of internal operation.
The NCR signal is “L” level while commands are processed, and goes to “H” level at the command waiting state.
The BUSYB signal is “L” level during playback voices.
The command interval time (: t_{INTRD}) is needed to input the next command after reading status using this command.
The following table shows the contents of each bit of data output.

bit	Contents
MSB	Channel 4 BUSYB output (BUSYB3)
7SB	Channel 3 BUSYB output (BUSYB2)
6SB	Channel 2 BUSYB output (BUSYB1)
5SB	Channel 1 BUSYB output (BUSYB0)
4SB	Channel 4 NCR output (NCR3)
3SB	Channel 3 NCR output (NCR2)
2SB	Channel 2 NCR output (NCR1)
LSB	Channel 1 NCR output (NCR0)



4. AMODE command

・command

0	0	0	0	0	1	0	0	1st byte
FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	POP	2nd byte

The AMODE command uses 2 bytes. This command is used to perform various settings for analog circuitry. This command is not available during power-down state, transition to power-up state, transition to power down state or playback state.
In the case of performing power down using PDWN command during power up of analog circuitry, the setting of power up by AMODE command is retained. Use the AMODE command to perform power down, if need to use different conditions from power up of analog circuitry.
In the case of power up of analog circuitry, input the AMODE command after setting the CVOL command to "00h" (: initial value).
The setting of each bit is shown below.
The setting is initialized by reset release or power up.

The FAD bit specifies whether to perform fade-out processing when the STOP command is input. If this bit is set to "1", fade-out processing is performed during a period of approx. 3 ms after the STOP command is input. The BUSYB signal goes to "H" level after fade-out processing.

FAD	Fade-out processing
0	Not available (initial value)
1	Available

The DAG1, 0 bits are used to set the gain of the internal DAC signal. The AIG1, 0 bits are used to set the gain of the analog input signal from the AIN pin. They are available only when using the speaker amplifier.

DAG1	DAG0	Volume
0	0	Input OFF
0	1	Input ON (-6 dB)
1	0	Input ON (0 dB) (initial value)
1	1	Prohibited (input ON (0 dB))

AIG1	AIG0	Volume
0	0	Input OFF (initial value)
0	1	Input ON (–6 dB)
1	0	Input ON (0 dB)
1	1	Prohibited (input ON (0 dB))

The DAEN bit controls power-up and power-down of the DAC circuitry.

DAEN	Status of the DAC circuitry
0	Power-down state (initial value)
1	Power-up state

The SPEN bit controls power-up and power-down of the speaker circuitry.
When the SPEN bit is “0”, SPP pin is the LINE output.

SPEN	Status of the speaker circuitry
0	Power-down state (initial value)
1	Power-up state

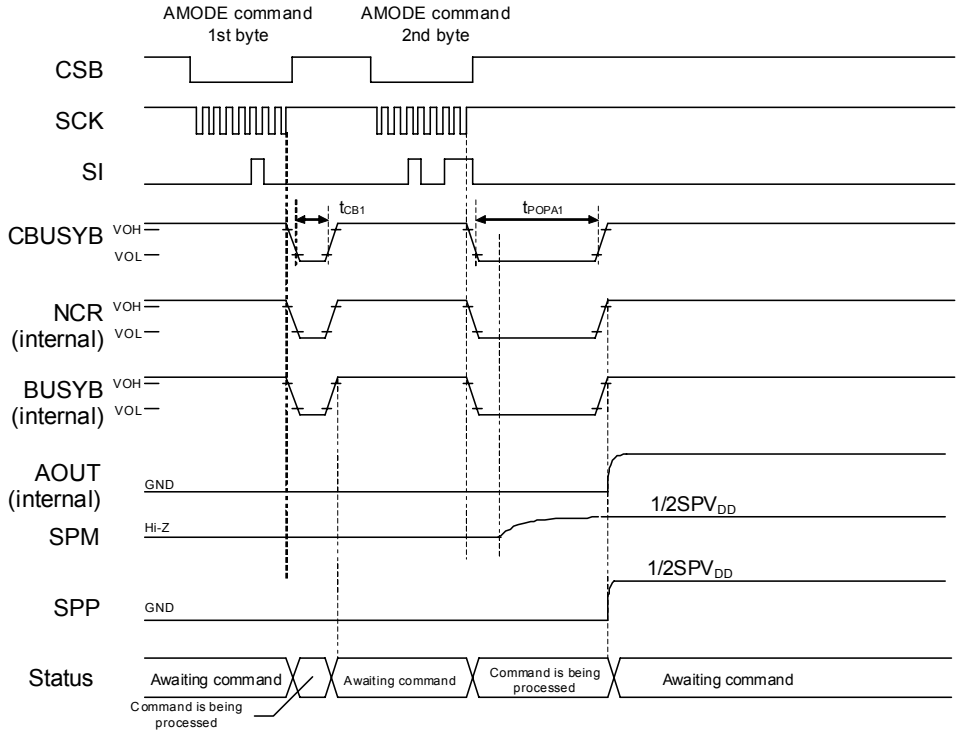
The POP bit sets whether to suppress the “pop” noise of the LINE output.

– In the case of setting the POP bit to “0”
If the DAEN bit is “1”, LINE output rises from the GND level to the SG level during a period of the specified time (:t_{POPA1}) . If the DAEN bit is “0”, LINE output falls from the SG level to the GND level during a period of the specified time (:t_{PDA1}).

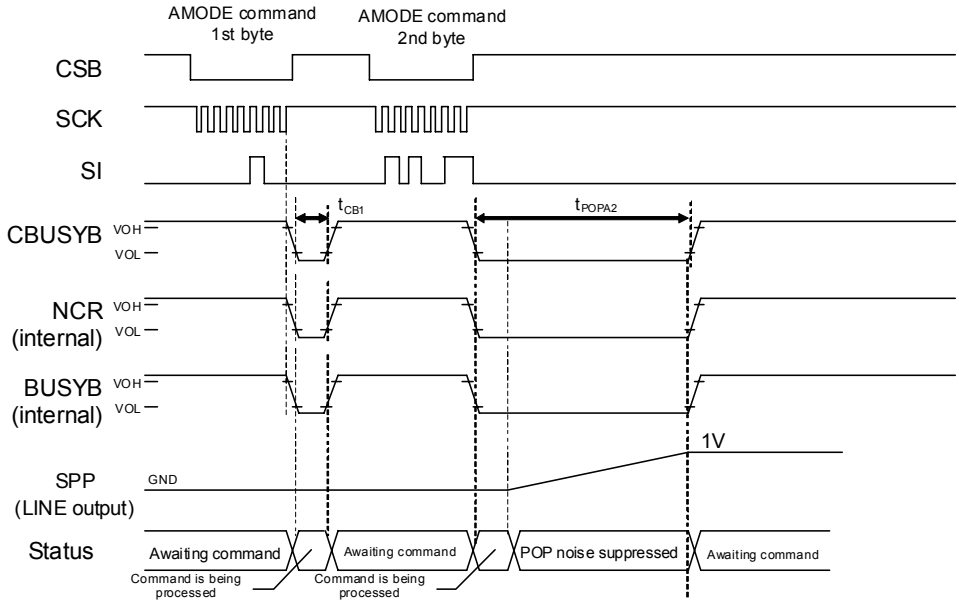
– In the case of setting the POP bit to “1”
If the DAEN bit is “1”, LINE output rises from the GND level to the SG level during a period of the specified time (:t_{POPA2}). If the DAEN bit is “0”, LINE output falls from the SG level to the GND level during a period of the specified time (:t_{PDA2}).

POP	Pop noise suppression
0	Not available (initial value)
1	Available

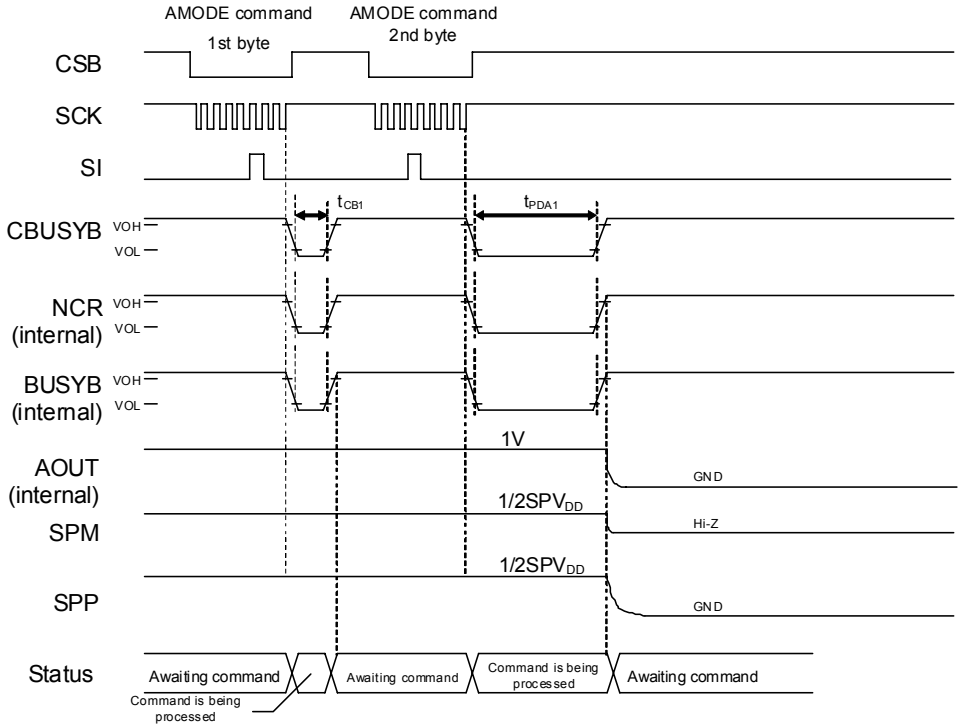
• When POP bit is “0” and DAEN or SPEN bit goes to “1”



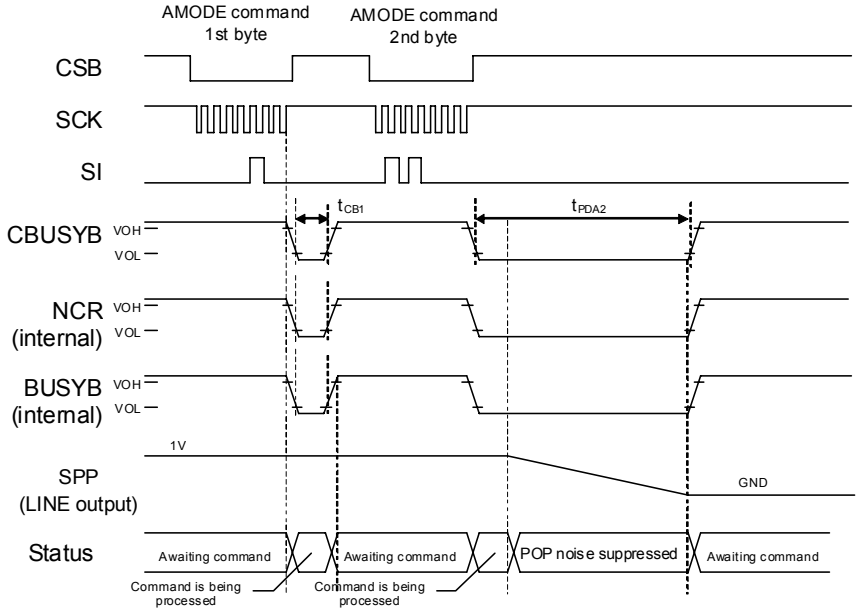
• When POP bit is “1”, SPEN bit is “0” and DAEN bit goes to “1”



• When POP bit is “0” and DAEN or SPEN bit goes to “0”



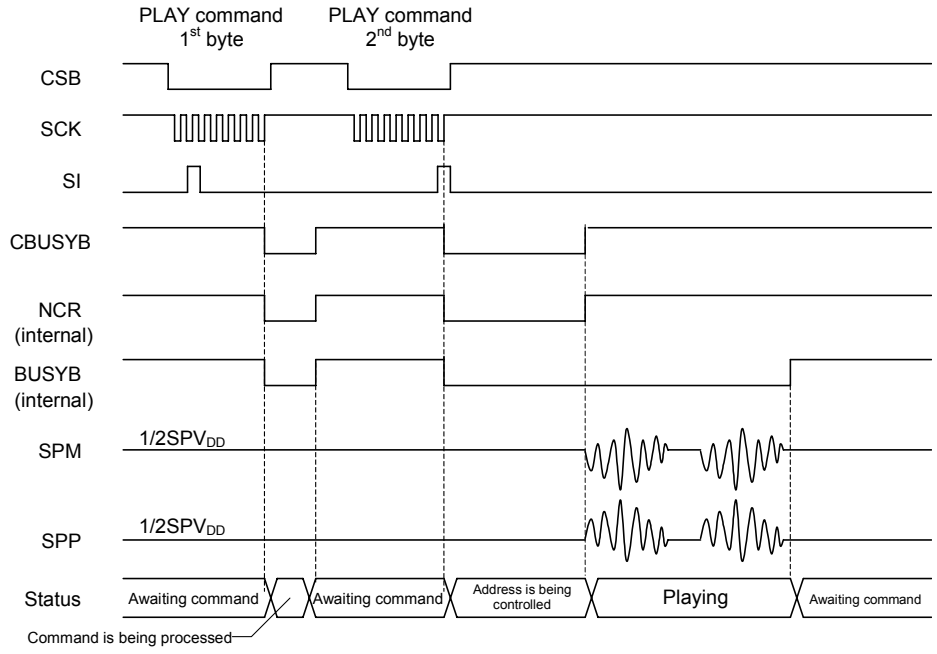
• When POP bit is “1”, SPEN bit is “0” and DAEN bit goes to “0”



5. PLAY command

・command									
	0	1	0	0	F9	F8	C1	C0	1st byte
	F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The PLAY command uses 2 bytes. This command is used to start playback phrase. This command is able to input by each channel when the NCR signal is "H" level. The channel to be played back is specified by C1 and C0 bits.
For the phrase to be played back, set the phrase address of voice data in the ROM using the F9 to F0 bits.
The following figure shows the timing of playback phrase (F9 to F0 is 01h).



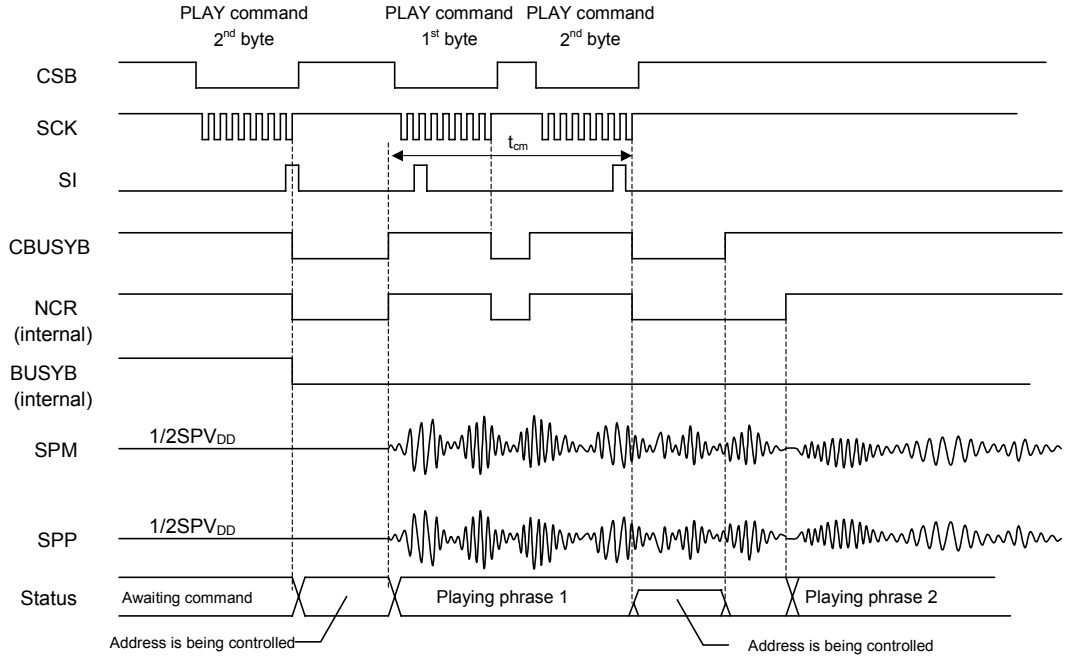
When the 1st byte of the PLAY command is input, the device enters a state awaiting input of the 2nd byte of the PLAY command after a lapse of command processing time. When the 2nd byte of PLAY command is input, the device starts reading the external ROM to get the address information of the phrase to be played back after a lapse of command processing time. Thereafter, playback starts and the playback is performed up to the specified ROM address, then the playback stops automatically.
The NCR signal is "L" level during address control, and goes to "H" level when the address control is completed. Then it is possible to input the PLAY command for the next playback phrase.
The BUSYB signal is "L" level during address control and playback, and goes to "H" level when playback is completed. Then it is possible to know whether the playback is going on by the BUSYB signal.

- Channel setting method

C1	C0	Channel
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

The PLAY Command Input Timing for Continuous Playback

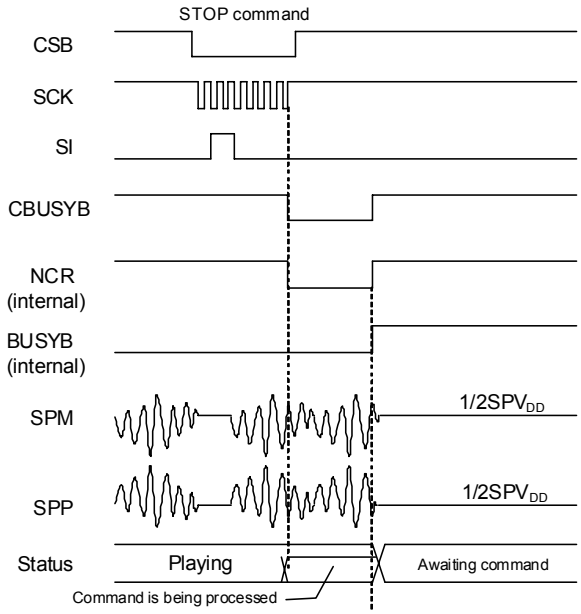
In the case of continuous playback, input the PLAY command for the next phrase within the command input enable time (: t_{cm}) after NCR goes to "H" level. Then it is possible to start playback the next phrase without any silent interval between phrases.



6. STOP command

・command	0	1	1	0	CH3	CH2	CH1	CH0

The STOP command is used to stop playback for each channel. This command can be set to each channel and also to multiple channels simultaneously. The channels are specified by setting CH0 to CH3 bits to "1" state respectively.
If the playback is stopped, the NCR and BUSYB signals go to "H" level.
Although it is possible to input this command regardless of the status of NCR during playback, a prescribed command interval time (:t_{INT}) is needed.
The STOP command is not available during power down, transition to power-up or transition to power-down.
The playback related command (:PLAY, START or MUON) is not available during STOP command processing.



- Channel setting method

bit	Channel
CH0	Channel 1
CH1	Channel 2
CH2	Channel 3
CH3	Channel 4

The playback related command (:PLAY, START or MUON), used on the same channel after the STOP command, should be input after confirming the completion (: NCRn is "H" and BUSYBn is "H", n is the related number of channel concerned) of this command processing by the RDSTAT command, or waiting for 12ms from transition of the CBUSYB to "H" level.

7. FADR command

・command									
	0	0	1	1	F9	F8	C1	C0	1st byte
	F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The FADR command uses 2 bytes. This command is used to specify phrase to be played. The channel and phrase to be played back are set by this command.
The channel for playback is specified by C0 and C1 bits.
Playback will be started by START command after the phrase for each channel is specified.
For the phrase to be played back, set the phrase address of voice data in the ROM using the F9 to F0 bits.
The setting values of the FADR command are initialized at the power-down.

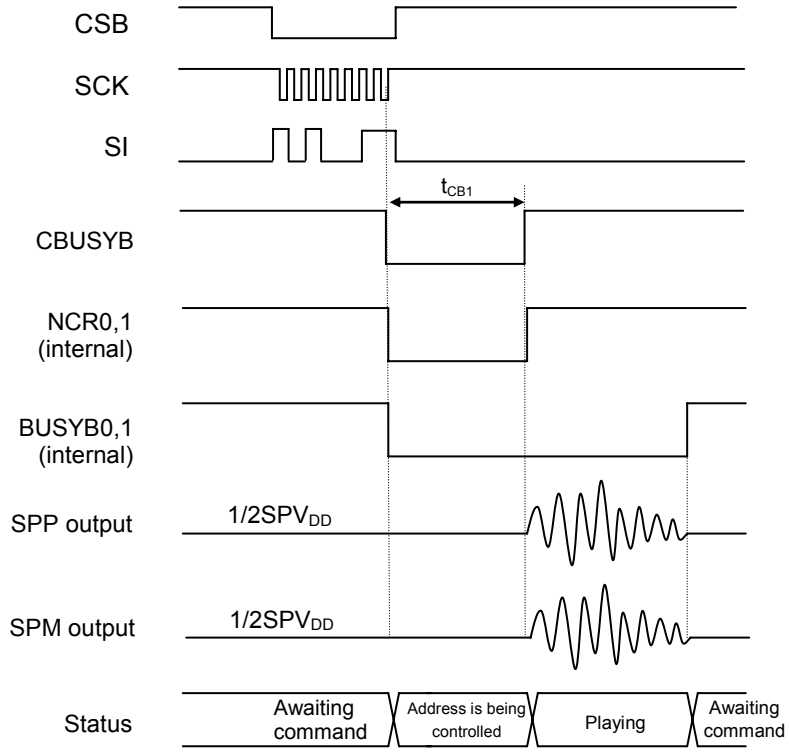
- Channel setting method

C1	C0	Channel
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

8. START command

・command	0	1	0	1	CH3	CH2	CH1	CH0

The START command is used to start playback on the channels specified. It is necessary to specify playback phrase using the FADR command before inputting this command.
Usually, use this command when starting playback on multiple channels simultaneously.
The channels to be played back are specified by setting CH0 to CH3 bits to "1" state respectively.
The following figure shows the timing when starting playback on channel 1 and channel 2 simultaneously.



- Channel setting method

bit	Channel
CH0	Channel 1
CH1	Channel 2
CH2	Channel 3
CH3	Channel 4

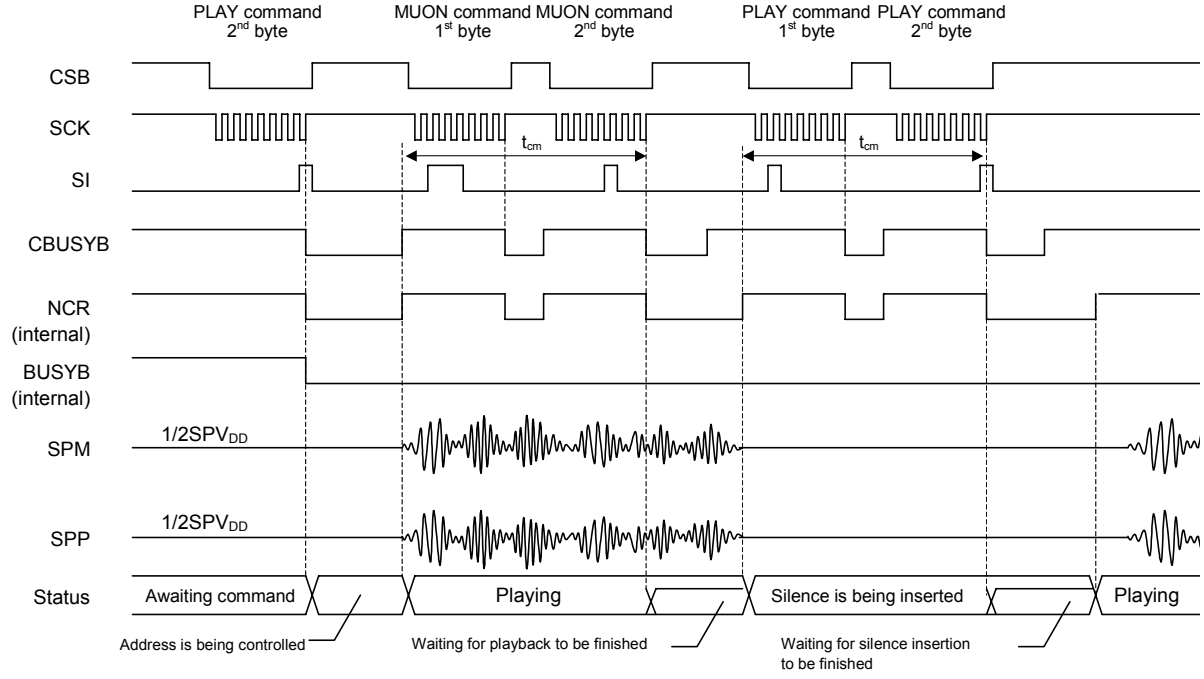
9. MUON command

・command									
	0	1	1	1	CH3	CH2	CH1	CH0	1st byte
	M7	M6	M5	M4	M3	M2	M1	M0	2nd byte

The MUON command uses 2 bytes. This command is used to insert the silence between two playback phrases. This command can be set to each channel and also to multiple channels simultaneously. The channels are specified by setting CH0 to CS3 bits to "1" state respectively.
This command can be input when the NCR signal is "H" level. Set the silent time value after inputting this command.
The silent time length to be specified by M7 to M0 bits is able to be set by 256 steps at 4 ms interval between 20 ms and 1,024 ms.
The silent time length (t_{mu}) is calculated by equation as below.
The silent time length should be set to 04h or higher (:t_{mu} is 20ms or more).

$$t_{mu} = (2^7\times(M7) + 2^6\times(M6) + 2^5\times(M5) + 2^4\times(M4) + 2^3\times(M3) + 2^2\times(M2) + 2^1\times(M1) + 2^0\times(M0) + 1) \times 4ms$$

The following figure shows the timing of inserting the silence of 20 ms between the repetitions of phrase (F7 to F0 is 01h).



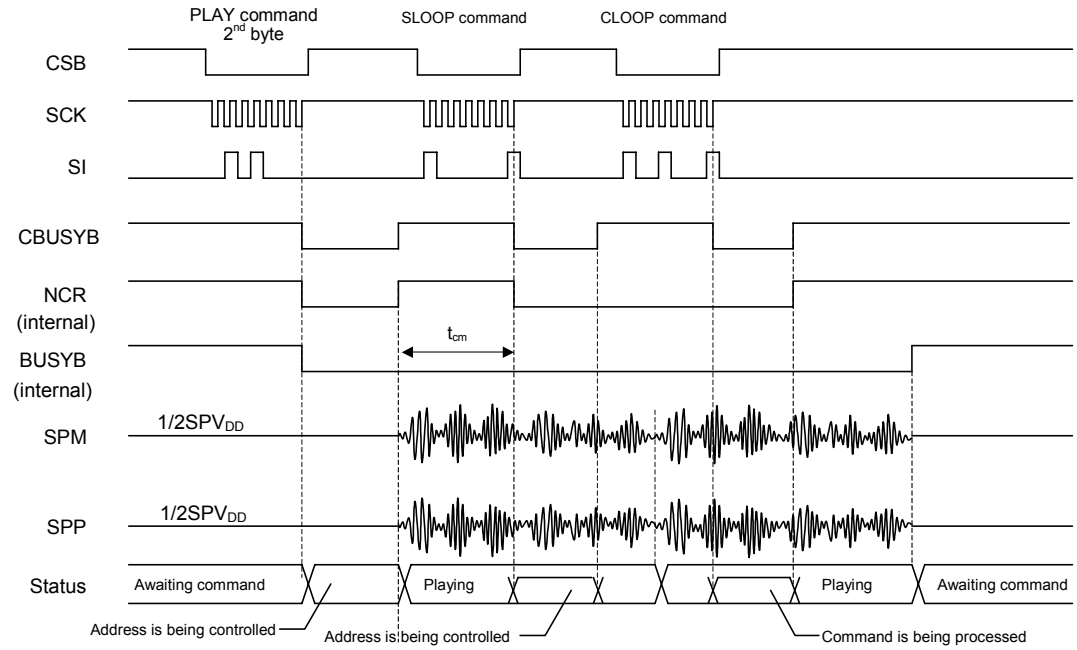
When the playback starts after the PLAY command is input and the address control of phrase-1 is over, the CBUSYB and NCR signals go to "H" level. Input the MUON command after this CBUSYB signal changes to "H" level. After the MUON command input, the NCR signal remains at "L" level until the end of phrase-1 playback. This status is the waiting for the phrase-1 playback to be finished.
When the phrase-1 playback is finished, the silence playback starts and the NCR signal goes to "H" level. Then, input the PLAY command again to playback phrase-1. Then, the NCR signal goes to "L" level again and the device enters a state of the waiting for the end of silence playback.
When the silence playback is finished and then the phrase-1 playback starts, the NCR signal goes to "H" level, and the device enters a status where it is possible to input the next PLAY or MUON command.
The BUSYB signal remains "L" level until the end of a series of playback.

10. SLOOP command

・command

1	0	0	0	CH3	CH2	CH1	CH0

The SLOOP command is used to set the repeat playback mode for each channel. This command can be set to each channel and also to multiple channels simultaneously. The channels are specified by setting CH0 to CH3 bits to "1" state respectively.
Use the CLOOP command to release repeat playback mode.
Since the SLOOP command is only valid during playback, be sure to input the SLOOP command while the NCR signal is "H" level after the PLAY command is input. The NCR signal is "L" level during repeat playback mode.
Once repeat playback mode is set, the current phrase is repeatedly played until the repeat playback setting is released by the CLOOP command or until playback is stopped by the STOP command. In the case of a phrase that was edited by the edit function, the edited phrase is repeatedly played.
The repeat playback mode is released if playback is stopped by the STOP command, therefore input the SLOOP command again if need to repeat playback again.
The following figure shows the SLOOP command input timing.



Effective Range of SLOOP Command Input

After the PLAY command is input, input the SLOOP command within the command input enable time (: t_{cm}) after NCR goes to "H". Then, the SLOOP command is available to repeat playback.

- Channel settings method

bit	Channel
CH0	Channel 1
CH1	Channel 2
CH2	Channel 3
CH3	Channel 4

11. CLOOP command

・command

1	0	0	1	CH3	CH2	CH1	CH0

The CLOOP command is used to release the repeat playback mode for each channel. This command can be set to each channel and also to multiple channels simultaneously. The channels are specified by setting CH0 to CH3 bits to "1" state respectively.
When the repeat playback mode is released, the NCR signal goes to "H" level.
It is possible to input this command regardless of the NCR signal status during playback, but a prescribed command interval time (:t_{INT}) is needed.

- Channel setting method

bit	Channel
CH0	Channel 1
CH1	Channel 2
CH2	Channel 3
CH3	Channel 4

12. CVOL command

・command

1	0	1	0	CH3	CH2	CH1	CH0	1st byte
0	0	0	CV4	CV3	CV2	CV1	CV0	2nd byte

The CVOL command uses 2 bytes. This command is used to adjust the playback volume of each channel. This command can be set to each channel and also to multiple channels simultaneously. The channels are specified by setting CH0 to CH3 bits to "1" state respectively.
It is possible to input this command regardless of the NCR status. This command is not available during power down, transition to the power-up state or transition to the power-down state.

This command can adjust volume by 32-levels as shown in the table below. The initial value is set to 0 dB after the reset is released. Also, the setting of this command is initialized after the reset is released or during power-up,

CV4-0	Volume	CV4-0	Volume
00	0dB (initial value)	10	-6.31
01	-0.28	11	-6.90
02	-0.58	12	-7.55
03	-0.88	13	-8.24
04	-1.20	14	-9.00
05	-1.53	15	-9.83
06	-1.87	16	-10.74
07	-2.22	17	-11.77
08	-2.59	18	-12.93
09	-2.98	19	-14.26
0A	-3.38	1A	-15.85
0B	-3.81	1B	-17.79
0C	-4.25	1C	-20.28
0D	-4.72	1D	-23.81
0E	-5.22	1E	-29.83
0F	-5.74	1F	OFF

- Channel setting method

bit	Channel
CH0	Channel 1
CH1	Channel 2
CH2	Channel 3
CH3	Channel 4

13. AVOL command

・command

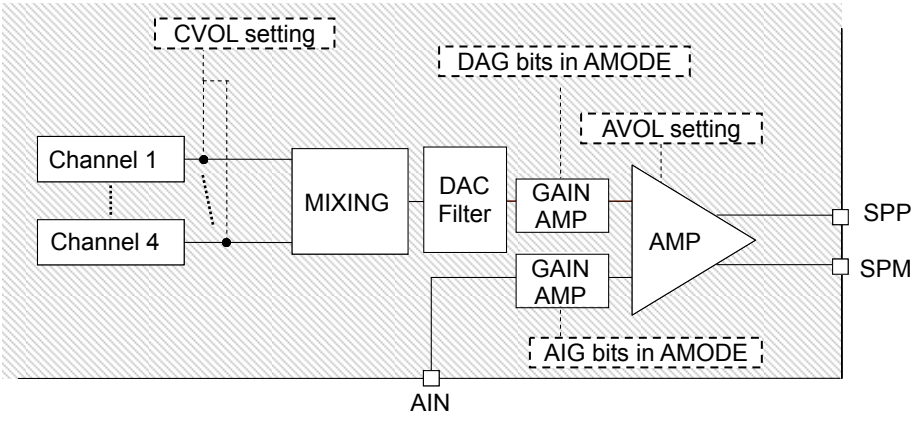
0	0	0	0	1	0	0	0	1st byte
0	0	AV5	AV4	AV3	AV2	AV1	AV0	2nd byte

The AVOL command uses 2 bytes. This command is used to adjust the playback volume. It is possible to input this command regardless of the NCR status. This command is not available during power down state, transition to power-up state or transition to power-down state.
This command can adjust volume by 50-levels as shown in the table below. The initial value is set to -4.0 dB after the reset is released. When the STOP command is input, the value set by the AVOL command is retained. When powered down, the value set by the AVOL command is initialized.

AV5-0	Volume (dB)	AV5-0	Volume (dB)	AV5-0	Volume (dB)	AV5-0	Volume (dB)
3F	+12.0	2F	+4.0	1F	-8.0	0F	-34.0
3E	+11.5	2E	+3.5	1E	-9.0	0E	OFF
3D	+11.0	2D	+3.0	1D	-10.0	0D	OFF
3C	+10.5	2C	+2.5	1C	-11.0	0C	OFF
3B	+10.0	2B	+2.0	1B	-12.0	0B	OFF
3A	+9.5	2A	+1.5	1A	-13.0	0A	OFF
39	+9.0	29	+1.0	19	-14.0	09	OFF
38	+8.5	28	+0.5	18	-16.0	08	OFF
37	+8.0	27	+0.0	17	-18.0	07	OFF
36	+7.5	26	-1.0	16	-20.0	06	OFF
35	+7.0	25	-2.0	15	-22.0	05	OFF
34	+6.5	24	-3.0	14	-24.0	04	OFF
33	+6.0	23	-4.0 (initial value)	13	-26.0	03	OFF
32	+5.5	22	-5.0	12	-28.0	02	OFF
31	+5.0	21	-6.0	11	-30.0	01	OFF
30	+4.5	20	-7.0	10	-32.0	00	OFF

To know the volume controls more

Three commands (: CVOL, AVOL and AMODE) can control volume. CVOL sets volume of each channel. AVOL sets volume of signal after mixing. And AMODE sets input gain of amplifier.



TERMINATION OF THE SG PIN

The SG pin is the signal ground for the built-in speaker amplifier. Connect a capacitor between this pin and the analog ground (: DGND) pin to prevent the trouble caused by noises.
Recommended capacitance value is shown below. However, it is important to evaluate and decide using the own board.
Also, start playback after each output voltage is stabilized.

Pin	Recommended capacitance value	Remarks
SG	0.1 μF ±20%	The time to stabilize voltage of the speaker outputs (:SPM and SPP) is longer, if use the larger capacitance.

TERMINATION OF THE V_{DDL} PIN

The V_{DDL} pin is the regulator output that is power supply for the internal logic circuitry. Connect a capacitor between this pin and the ground (: DGND) pin to prevent the trouble caused by noises and to hold power supply voltage steady.
The recommended capacitance value is shown below. However, it is important to evaluate and decide using the own board.
Also, start the next operation after each output voltage is stabilized.

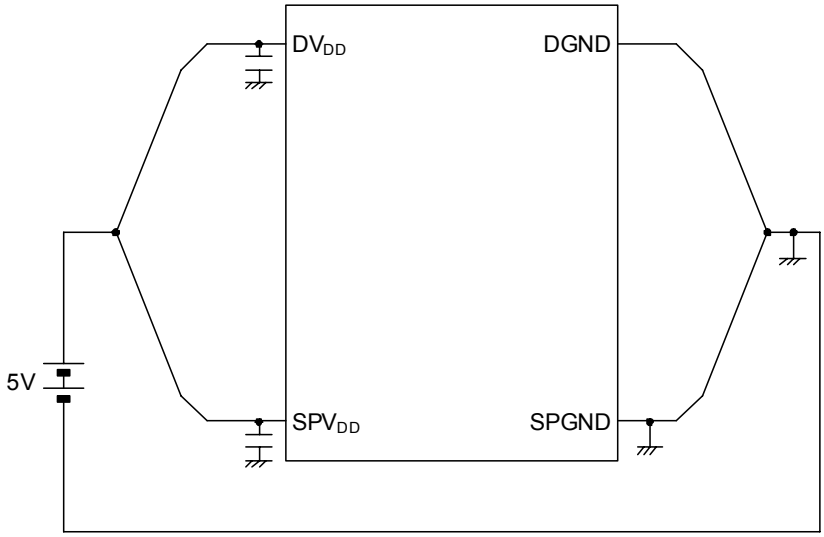
Pin	Recommended capacitance value	Remarks
V_{DDL}	10 μF ±20%	The time to stabilize voltage of each output is longer, if use the larger capacitance.

POWER SUPPLY WIRING

The power supplies of this LSI are divided into the following two:

- Power supply for logic circuitry (: DV_{DD})
- Power supply for speaker amplifier (: SPV_{DD})

As shown in the figure below, supply DV_{DD} and SPV_{DD} from the same power supply, and separate them into analog and logic power supplies in the wiring.



RECOMMENDED CERAMIC RESONATOR

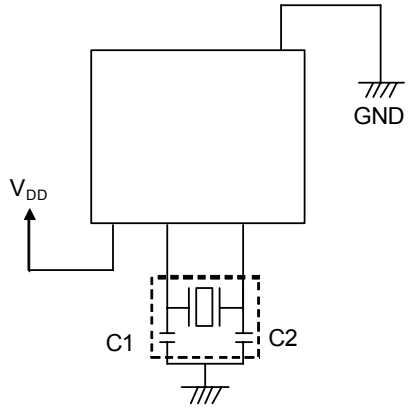
Recommended ceramic resonators for oscillation and conditions are shown below for reference.

KYOCERA Corporation

Freq [Hz]	Type	Conditions					
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Supply voltage Range [V]	Operating Temperature Range [°C]
4.096M	PBRC4.096MR50X000	15(built-in)		---	--	2.7 to3.3 4.5 to5.5	-20 to +85

Note: C1 and C2 are capacitors built-in resonator.

Circuit diagram

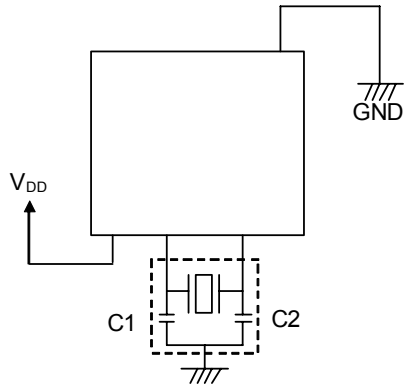


TDK Corporation

Freq [Hz]	Type	Conditions					
		C1 [pF]	C2 [pF]	Rf [Ohm]	C1 [pF]	Supply voltage Range [V]	Operating Temperature Range [°C]
4.000M	FCR4.0MXC5	30 (built-in)		---	---	2.7 to3.6	-40 to +85
	FCR4.0MXC5					4.5 to5.5	
4.096M	FCR4.09MXC5	30 (built-in)		---	---	2.7 to3.6	-40 to +85
	FCR4.09MXC5					4.5 to5.5	

Note: C1 and C2 are capacitors built-in resonator.

Circuit diagram

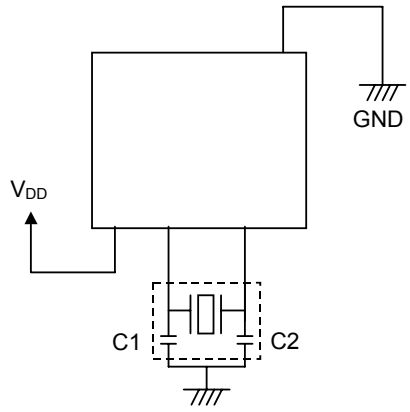


MURATA Corporation

Freq [Hz]	Type		Conditions					
			C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]	Supply voltage Range [V]	Operating Temperature Range [°C]
4.000M	SMD	CSTCR4M00G55-R0	39 (Built-in)		---	---	2.7 to 3.6	-40 to +85*
	Leaded	CSTLS4M00G56-B0	47 (Built-in)					
	SMD	CSTCR4M00G55-R0	39 (Built-in)				4.5 to 5.5	
	Leaded	CSTLS4M00G56-B0	47 (Built-in)					
4.096M	SMD	CSTCR4M09G55-R0	39 (Built-in)		---	---	2.7 to 3.6	
	Leaded	CSTLS4M09G56-B0	47 (Built-in)					
	SMD	CSTCR4M09G55-R0	39 (Built-in)				4.5 to 5.5	
	Leaded	CSTLS 4M09G56-B0	47 (Built-in)					

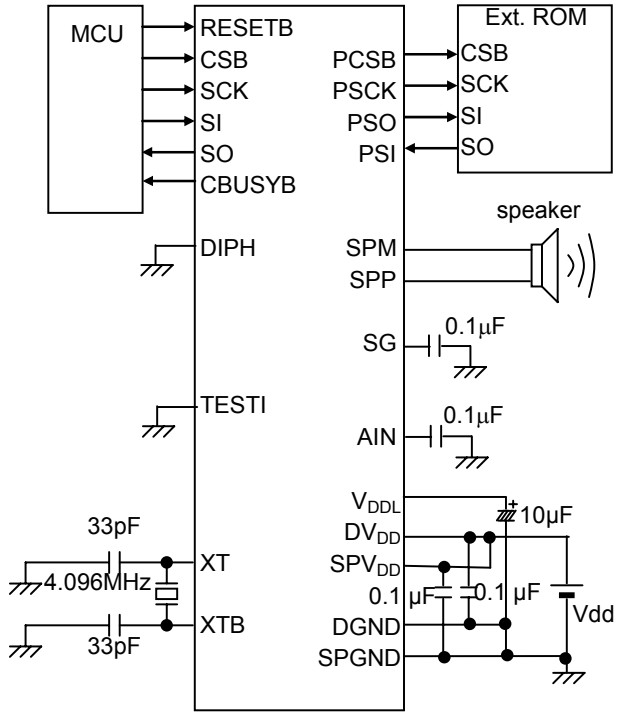
Note: C1 and C2 are capacitors built-in resonator.

Circuit diagram

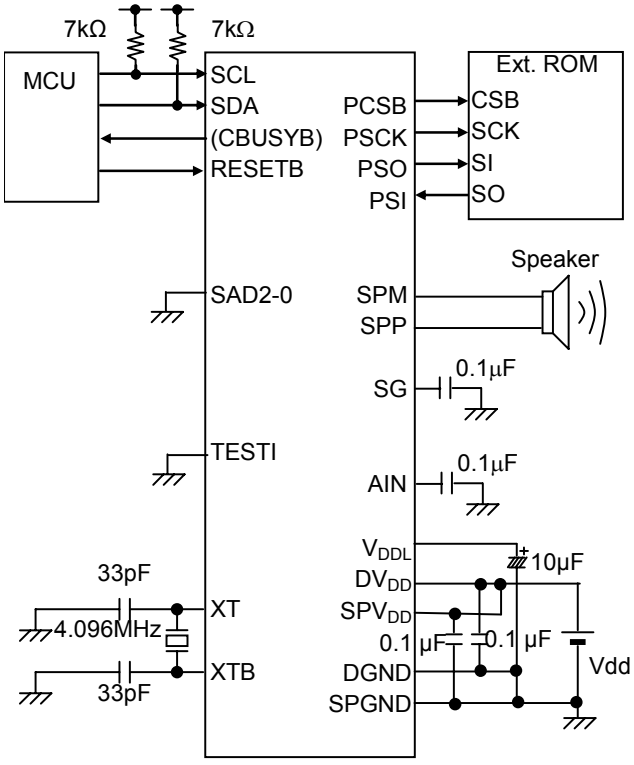


APPLICATION CIRCUIT

ML22420: DV_{DD}=SPV_{DD}= Vdd

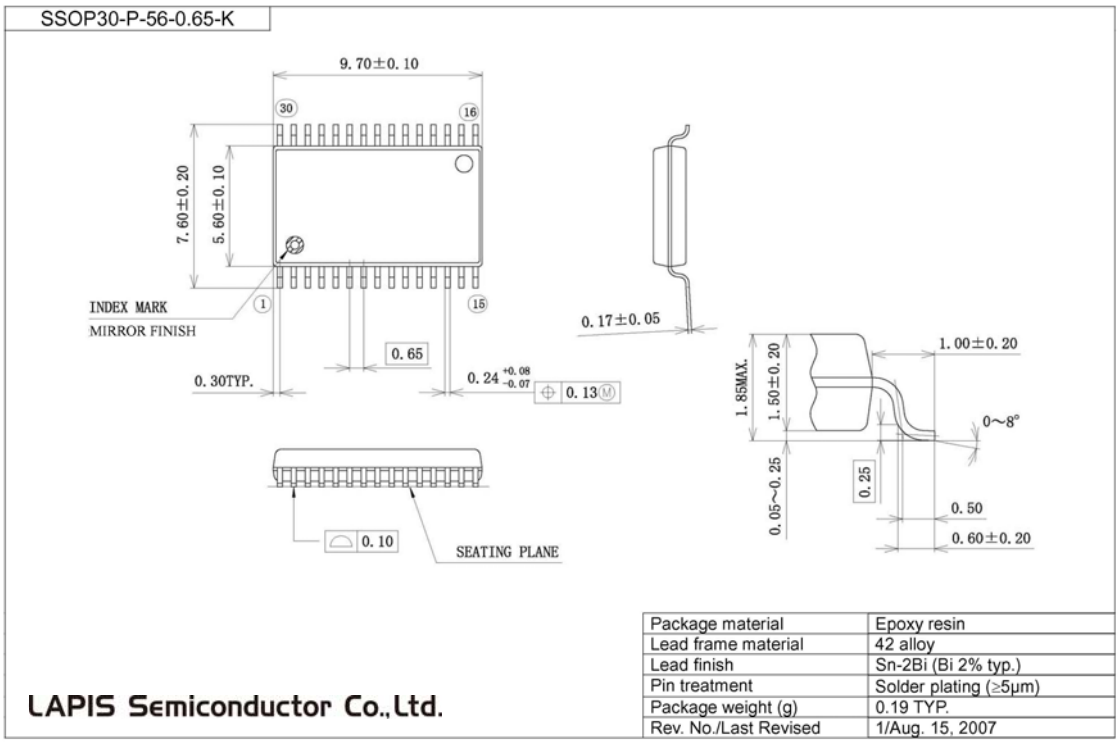


ML22460: DV_{DD}=SPV_{DD}= Vdd



PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2% typ.)
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	1/Aug. 15, 2007

Notes for Mounting the Surface Mount Type Package:

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL22420FULL-01	Sep. 17, 2008	–	–	Final edition 1
FEDL22420FULL-03	Mar. 25, 2009	17	11,19	Add Serial ROM interface timing information
		-	49	Correct ML22460 application circuit
		-	-	Remove all tCB2
		14	10	Correct Max value of LINE output voltage range
		11	11	Correct max value of tCB1
		49	49	Modify application circuit
		44	44	Correct value for AVOL
FEDL22420FULL-04	Aug.26,2009	1	1	Add Maximum External ROM capacity
		5	5	Modify PSO/PSI/PSCK/PCSB initial value
		49	49	Modify application circuit(ML22460)
FEDL22420FULL-05	Aug.25,2011	44	44	Modify AVOL volume table.

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