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LANSDALE Semiconductor, Inc.

ML145159
Serial-Input PLL Frequency Synthesizer with Analog Phase Detector

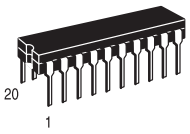
INTERFACES WITH DUAL–MODULUS PRESCALERS

Legacy Device: *Motorola MC145159-1*

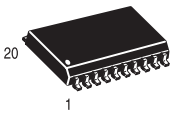
The ML145159 has a programmable 14–bit reference counter, as well as fully programmable divide–by–N/divide–by–A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

When combined with a loop filter and VCO, this device can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operations, a down mixer or a dual–modulus prescaler can be used between the VCO and the PLL.

- Operating Temperature Range: T_A – 40° to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- ÷ R Range = 3 to 16383
- ÷ N Range = 16 to 1023, P A Range = 0 to 127
- High–Gain Analog Phase Detector
- See Application Note AN969



P DIP 20 = RP
PLASTIC DIP
CASE 738



SOG 20W = -6P
SOG PACKAGE
CASE 751D

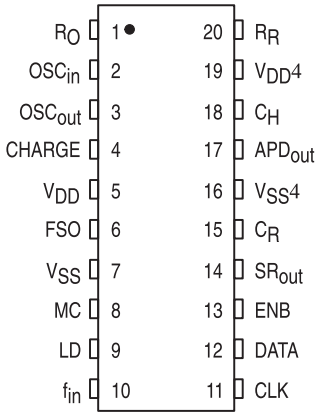
CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 20	MC145159P1	ML145159RP
SOG 20W	MC145159DW1	ML145159-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

PIN ASSIGNMENTS

PLASTIC DIP AND SOG PACKAGE



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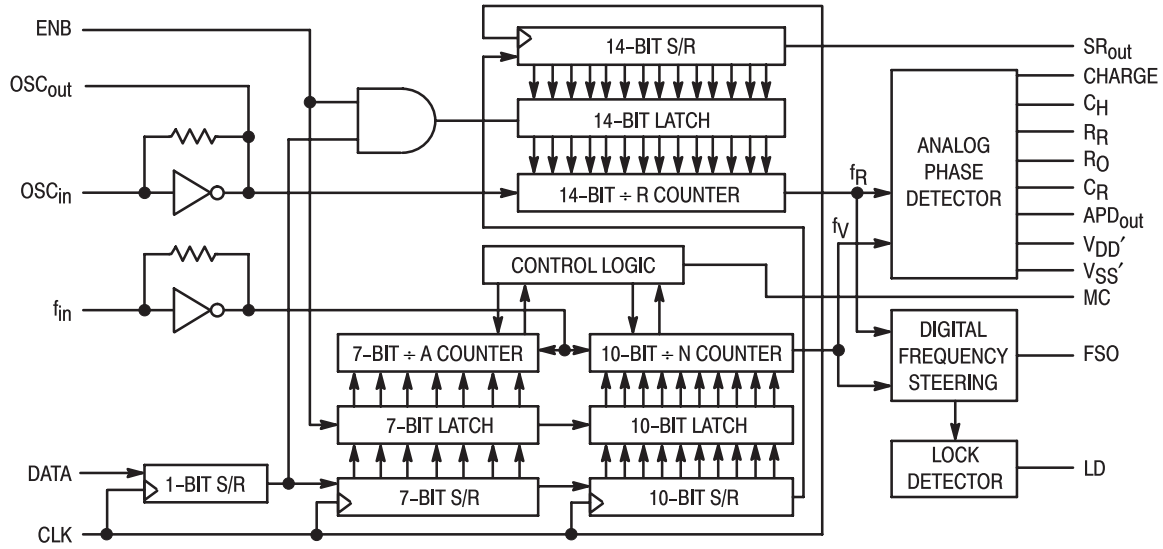
BLOCK DIAGRAM



* FSO is not and cannot be used as a digital phase detector output.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS} except I_{CR} and I_{APD} which are referenced to V_{SS}′)

Characteristic	Symbol	V_{DD}	– 40°C Min	– 40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Power Supply Voltage Range	V_{DD}	—	3	9	3	9	3	9	V
Output Voltage 0 Level V_{in} = 0 V or V_{DD} I_{out} = 0 μA	V_{OL}	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
(Except OSC_{out} and APD_{out}) 1 Level	V_{OH}	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	
Output Voltage 0 Level OSC_{out} V_{in} = 0 V or V_{DD}	V_{OL}	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
1 Level	V_{OH}	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
ΔVoltage, $V_{CH} - V_{APDout}$, $I_{APDout} \approx 0$ μA	ΔV	—	—	—	—	1.05	—	—	V
Input Voltage 0 Level V_{out} = 0.5 V or V_{DD} – 0.5 V (All Outputs Except OSC_{out})	V_{IL}	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
1 Level	V_{IH}	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
Input Voltage* — OSC_{in} V_O = 2.1 V or 0.9 V 0 Level V_O = 3.5 V or 1.5 V V_O = 6.3 V or 2.7 V	V_{IL}	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
1 Level V_O = 0.9 V or 2.1 V V_O = 1.5 V or 3.5 V V_O = 2.7 V or 6.3 V	V_{IH}	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
Output Current — MC V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	– 0.60 – 0.90 – 1.50	— — —	– 0.50 – 0.75 – 1.25	— — —	– 0.30 – 0.50 – 0.80	— — —	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	
Output Current, C_R, V_{CR} = 4.5 V, R_R = 240 k	I_{CR}	9	—	—	– 90	– 110	—	—	μA
Output Current, APD_{out} R_O = 240 k, V_{CH} = 0 V, V_{APDout} = 4.5 V	I_{APD}	9	—	—	170	350	—	—	μA
Output Current — Other Outputs V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	– 0.44 – 0.64 – 1.30	— — —	– 0.35 – 0.51 – 1.00	— — —	– 0.22 – 0.36 – 0.70	— — —	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	
Input Current — Data, CLK, ENB	I_{in}	9	—	± 0.3	—	± 0.1	—	± 1.0	μA
Input Current — f_{in}, OSC_{in}	I_{in}	9	± 2	± 50	± 2	± 25	± 2	± 22	μA
Input Capacitance	C_{in}	—	—	10	—	10	—	10	pF
Three–State Output Capacitance — FSO	C_{out}	—	—	10	—	10	—	10	pF
Quiescent Current V_{in} = 0 V or V_{DD} I_{out} = 0 μA	I_{DD}	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	μA
Three–State Leakage Current, V_{out} = 0 V or 9 V	I_{OZ}	9	—	± 0.3	—	± 0.1	—	± 3.0	μA

* DC coupled square wave.

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SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Characteristic	Figure No.	Symbol	V_{DD}	Min	Max	Unit
Output Rise Time — MC	4, 9	t_{TLH}	3 5 9	— — —	115 60 40	ns
Output Fall Time — MC	4, 9	t_{THL}	3 5 9	— — —	60 34 30	ns
Output Rise and Fall Time — LD and SR_{out}	4, 9	t_{TLH}, t_{THL}	3 5 9	— — —	140 80 60	ns
Propagation Delay Time — f_{in} to MC	5, 9	t_{PLH}, t_{PHL}	3 5 9	— — —	125 80 50	ns
Setup Times — Data to CLK	6	t_{su}	3 5 9	30 20 18	— — —	ns
CLK to ENB			3 5 9	70 32 25	— — —	
Hold Time — CLK to Data	6	t_h	3 5 9	12 12 15	— — —	ns
Recovery Time — ENB to CLK	6	t_{rec}	3 5 9	5 10 20	— — —	ns
Input Rise and Fall Times — CLK, OSC_{in}, f_{in}	7	t_r, t_f	3 5 9	— — —	5 2 0.5	µs
Input Pulse Width — ENB and CLK	8	t_w	3 5 9	40 35 25	— — —	ns

NOTE: Refer to the graphs and text in application note AN969 for maximum frequency information.

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PIN DESCRIPTIONS

INPUT PINS

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (PDIP, SOG – Pins 2, 3; SSOP – Pins 7, 8)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel–resonant crystal. Frequency–setting capacitors of appropriate value must be connected from OSC_{in} to V_{SS} and OSC_{out} toV_{SS}. OSC_{in} may also serve as input for an externally–generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels), DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

f_{in}
Frequency Input (PDIP, SOG – Pin 10, SSOP – Pin 15)

Input to the positive edge triggered divide–by–N and divide–by–A counters. f_{in} is typically derived from a dual–modulus prescaler and is AC coupled. This input has an inverter biased in the linear region to allow use with AC coupled signals as low as 500 mV peak–to–peak or direct coupled signals swinging from V_{DD} to V_{SS}.

DATA
Serial Data Input (PDIP, SOG – Pin 12, SSOP – Pin 17)

Counter and control information is shifted into this input. The last data bit entered goes into the one–bit control shift register. A logic 1 allows the reference counter information to be loaded into its 14–bit latch when ENB goes high. A logic 0 entered as the control bit disables the reference counter latch. The divide–by–A/divide–by–N counter latch is loaded, regardless of the contents of the control register, when ENB goes high. The data entry format is shown in Figure 1.

ENB
Transparent Latch Enable (PDIP, SOG – Pin 13, SSOP – Pin 18)

A logic high on this input allows data to be entered into the divide–by–A/divide–by–N latch and, if the control bit is high, into the reference counter latch. Counter programming is unaffected when ENB is low. ENB should be kept normally low and pulsed high to transfer data to the latches.

CLK
Shift Register Clock (PDIP, SOG – Pin 11, SSOP – Pin 16)

A low–to–high transition on this input shifts data from the serial data input into the shift registers.

COMPONENT PINS

C_R
Ramp Capacitor (PDIP, SOG – Pin 15, SSOP – Pin 20)

The capacitor connected from this pin to V_{SS}' is charged linearly, at a rate determined by R_R. The voltage on this capacitor is proportional to the phase difference of the frequencies present at the internal phase detector inputs. A polystyrene or mylar capacitor is recommended.

R_R
Ramp Current Bias Resistor (PDIP, SOG – Pin 20, SSOP – Pin 5)

A resistor connected from this pin to V_{SS}' determines the rate at which the ramp capacitor is charged, thereby affecting the phase detector gain (see Figure 2).

C_H
Hold Capacitor (PDIP, SOG – Pin 18, SSOP – Pin 3)

The charge stored on the ramp capacitor is transferred to the capacitor connected from this pin to either V_{DD}' or V_{SS}'. The ratio of C_R to C_H should be large enough to have no effect on the phase detector gain ($C_R > 10\ C_H$). A low–leakage capacitor should be used.

R_O
Output Bias Current Resistor (PDIP, SOG – Pin 1, SSOP – Pin 6)

A resistor connected from this pin to V_{SS}' biases the output N–Channel transistor, thereby setting a current sink on the analog phase detector output. This resistor adjusts the APD_{out} bias current (see Figure 3).

OUTPUT PINS

APD_{out}
Analog Phase Detector Output (PDIP, SOG – Pin 17, SSOP – Pin 2)

This output produces a voltage that controls an external VCO. The voltage range of this output (V_{DD} = + 9 V) is from below + 0.5 V to + 8 V or more. The source impedance of this output is the equivalent of a source follower with an externally variable source resistor. The source resistor depends upon the output bias current controlled by the output bias current resistor, R_O. The bias current is adjustable from 0.01 mA to 0.5 mA. The output voltage is not more than 1.05 V below the sampled point on the ramp. With a constant sample of the ramp voltage at 9 V and the hold capacitor of 50 pF, the instantaneous output ripple is about 5 mV peak–to–peak.

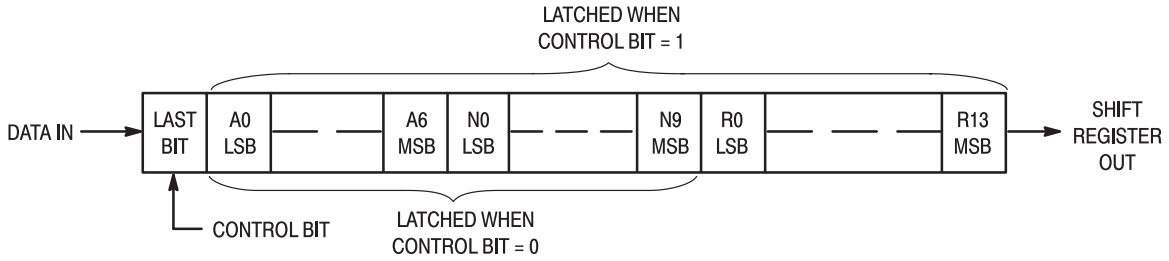

Figure 1. Data Entry Format

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CHARGE
Ramp Charge Indicator (PDIP, SOG – Pin 4, SSOP – Pin 9)

This output is high from the time f_R goes high to the time f_V goes high (f_R and f_V are the frequencies at the phase detector inputs). This high voltage indicates that the ramp capacitor, C_R, is being charged.

FSO
Three–State Frequency Steering Output (PDIP, SOG –Pin 6, SSOP – Pin 11)

If the counted down input frequency on f_{in} is higher than the counted down reference frequency of OSC_{in}, this output goes low. If the counted down VCO frequency is lower than that of the counted down OSC_{in}, this output goes high.

The repetition rate of the frequency steering output pulses is approximately equal to the difference of the frequencies of the two counted down inputs from the VCO and OSC_{in}. See Application Note AN969 for further information.

LD
Lock Detector Indicator (PDIP, SOG – Pin 9, SSOP – Pin 14)

This output is high during lock and goes low to indicate a non–lock condition. The frequency and duration of the non–lock pulses will be the same as either polarity of the frequency steering output.

MC
Dual Modulus Prescaler Control (PDIP, SOG – Pin 8, SSOP – Pin 13)

The modulus control level is low at the beginning of a count cycle and remains low until the divide–by–A counter has counted down from its programmed value. At that time, the modulus control goes high and remains high until the divide–by–N counter has counted the rest of the way down from its programmed value (N – A additional counts since both divide–by–N and divide–by–A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value of NT = N • P + A, where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels, N is the number programmed into the divide–by–N counter, and A is the number programmed into the divide–by–A counter.

SRout
Shift Register Output (PDIP, SOG – Pin 14, SSOP – Pin 19)

This pin is the non–inverted output of the last stage of the 32–bit serial data shift register. It is not latched by the ENB line. If unused, SR_{out} should be floated.

POWER SUPPLY

V_{DD}
Positive Power Supply (PDIP, SOG – Pin 5, SSOP – Pin 10)

Positive power supply input for all sections of the device except the analog phase detector. V_{DD} and V_{DD}' should be powered up at the same time to avoid damage to the ML145159. V_{DD} must be tied to the same potential asV_{DD}'.

V_{SS}
Negative Power Supply (PDIP, SOG – Pin 7, SSOP – Pin 12)

Circuit ground for all sections of the ML145159 except the analog phase detector. V_{SS} must be tied to the same potential as V_{SS}'.

V_{SS}'
Analog Phase Detector Circuit Ground (PDIP, SOG – Pin 16, SSOP – Pin 1)

Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

V_{DD}'
Analog Power Supply (PDIP, SOG – Pin 19, SSOP – Pin 4)

Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

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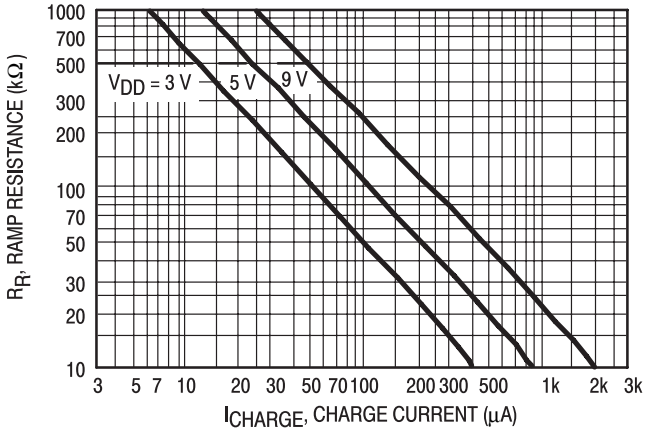


Figure 2. Charge Current vs Ramp Resistance

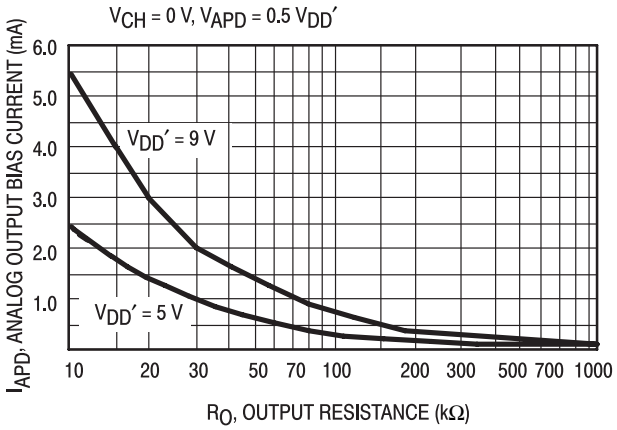


Figure 3. APD_{out} Bias Current vs Output Resistance

DESIGN EQUATION

$$K_\phi = \frac{I_{CHARGE}}{2\pi f_R C_R}$$

where

K_ϕ = phase detector gain, I_{CHARGE} is from Figure 2
f_R = reference frequency
C_R = ramp capacitor (in farads)

SWITCHING WAVEFORMS

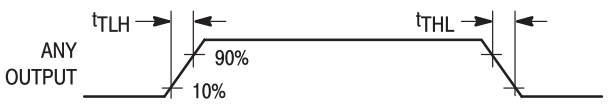


Figure 4.

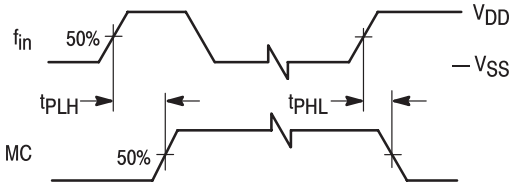


Figure 5.

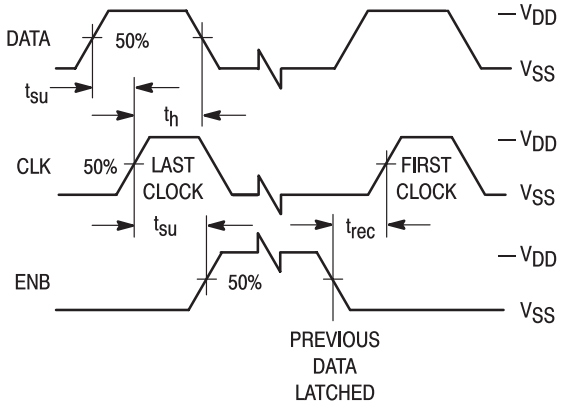


Figure 6.

Figure 7.

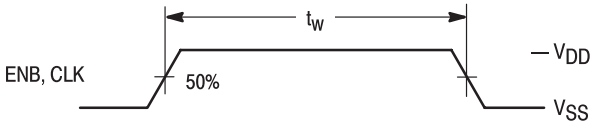
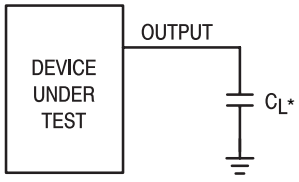


Figure 8.



* Includes all probe and fixture capacitance.

Figure 9. Test Circuit

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DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Lansdale's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or DC coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or AC coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the ML12061 MECL device. The reference signal from the MECL device is AC coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), DC coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.

For V_{DD} = 5 V, the crystal should be specified for a loading capacitance, CL, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. Assuming R1 = 0 Ω. the shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

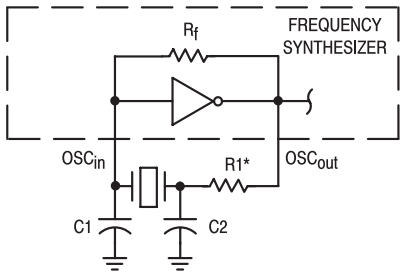
C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C1 and C2 = external capacitors (see Figure 10)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on–frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSCout pins to minimize distortion, stray capacitance, stray inductance, and start–up stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The maximum drive level specified by the crystal manufacturer represents the maximum stress that a crystal can withstand without damaging or excessive shift in operating frequency. R1 in Figure 10 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

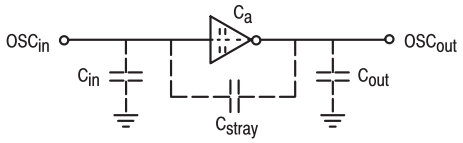
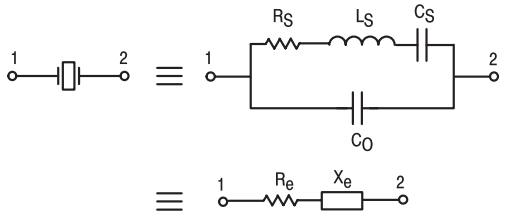


Figure 11. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

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Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Lansdale cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN–24, Statek Corp.

Technical Note TN–7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

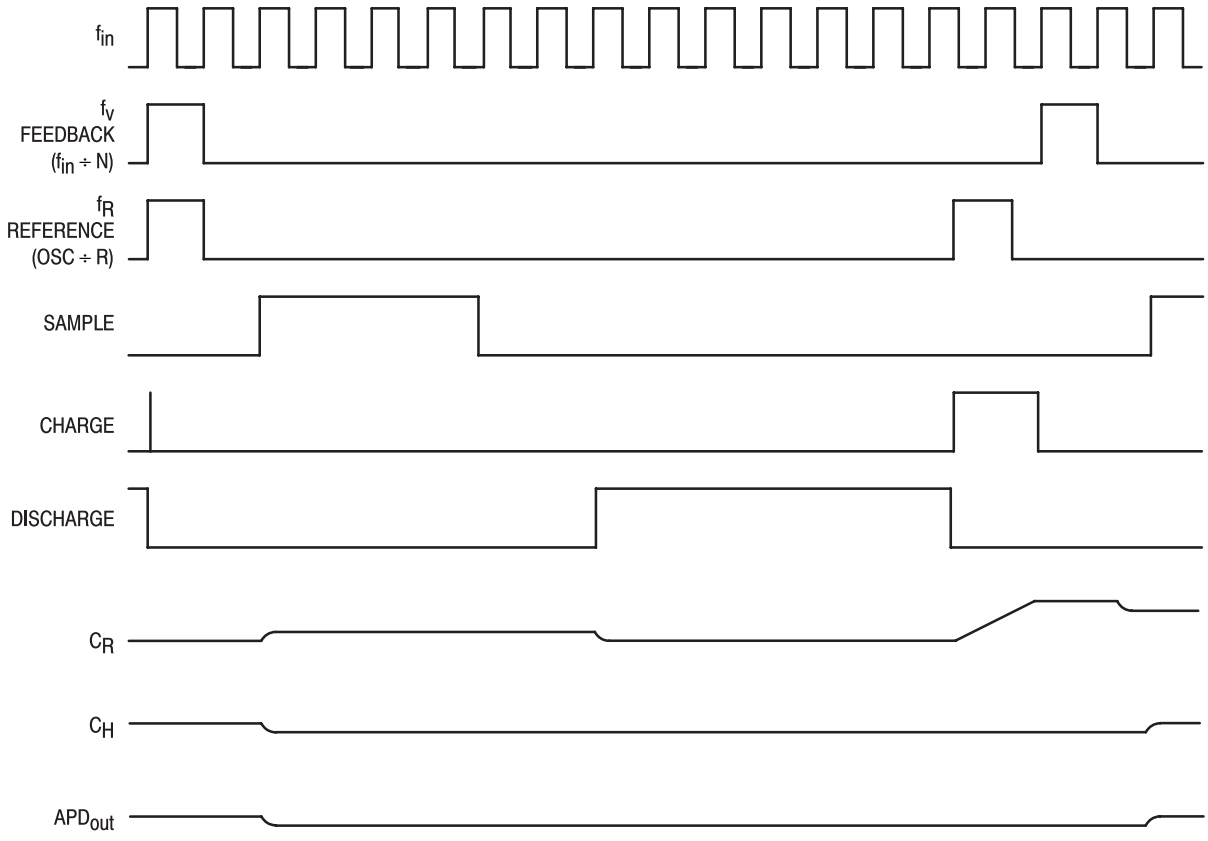

Figure 13. Timing Diagram for Minimum Divide Value (N = 16)

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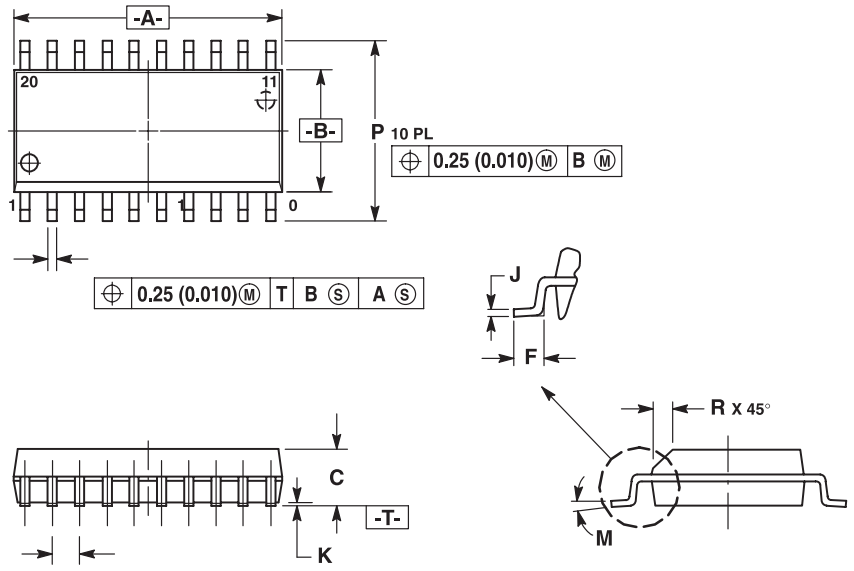
OUTLINE DIMENSIONS

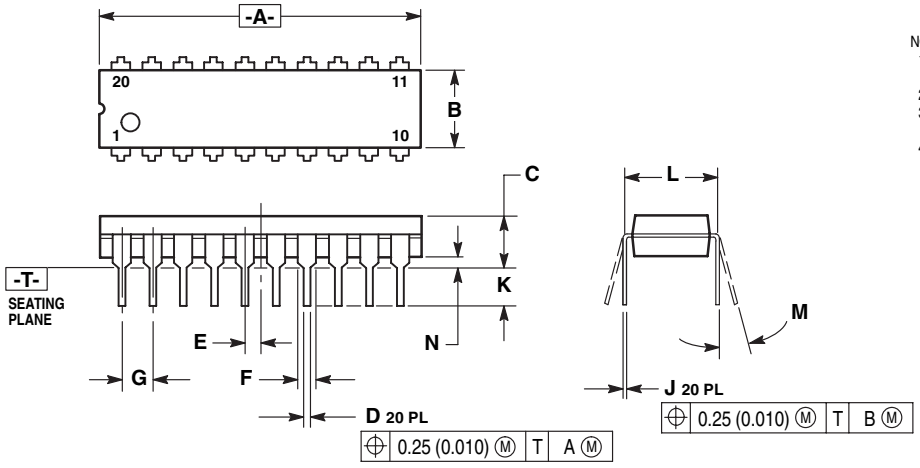
SOG = -6P
(MC145159-6P)
CASE 751D-04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONA AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL, IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.020	0.035
M	0°	7°	0°	7°
P	10.05	10.56	.0395	0.415
R	0.25	0.75	0.010	0.029

PLASTIC DIP 20 = RP
(MC145159RP)
CASE 738-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS		
DIM	MIN		MIN	MAX	MAX
A	1.010	1.070	25.66	27.17	
B	0.240	0.260	6.10	6.60	
C	0.150	0.180	3.81	4.57	
D	0.015	0.022	0.39	0.55	
E	0.050 BSC		1.27 BSC		
F	0.050	0.070	1.27	1.77	
G	0.100 BSC		2.54 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.140	2.80	3.55	
L	0.300 BSC		7.62 BSC		
M	0°	15°	0°	15°	
N	0.020	0.040	0.51	1.01	

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